Document Number: AFT09S282N
Rev. 0, 10/2012

RoHS

RF Power LDMOS Transistor

N-Channel Enhancement-Mode Lateral MOSFET

This 80 watt RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 720 to 960 MHz.

- Typical Single-Carrier W-CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 1400 mA, P_{out} = 80 Watts Avg., Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF.

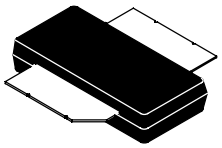
Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
920 MHz	20.0	35.9	6.3	-38.0	-14
940 MHz	20.1	36.2	6.2	-37.6	-18
960 MHz	20.0	36.1	6.1	-37.5	-17

Features

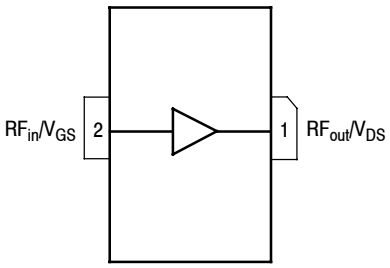
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications
- In Tape and Reel. R3 Suffix = 250 Units, 32 mm Tape Width, 13 inch Reel.

AFT09S282NR3

720-960 MHz, 80 W AVG., 28 V



OM-780-2
PLASTIC



(Top View)

Figure 1. Pin Connections

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	-0.5, +70	Vdc
Gate-Source Voltage	V_{GS}	-6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature Range	T_C	-40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	-40 to +225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 80 W CW, 28 Vdc, I_{DQ} = 1500 mA, 960 MHz Case Temperature 91°C, 282 W CW, 28 Vdc, I_{DQ} = 1500 mA, 960 MHz	$R_{\theta JC}$	 0.31 0.27	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	2
Machine Model (per EIA/JESD22-A115)	B
Charge Device Model (per JESD22-C101)	IV

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 70 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 370 μAdc)	$V_{GS(th)}$	1.0	1.5	2.0	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 1400 mA, Measured in Functional Test)	$V_{GS(Q)}$	1.7	2.2	2.7	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 3.6 Adc)	$V_{DS(on)}$	0.1	0.14	0.3	Vdc

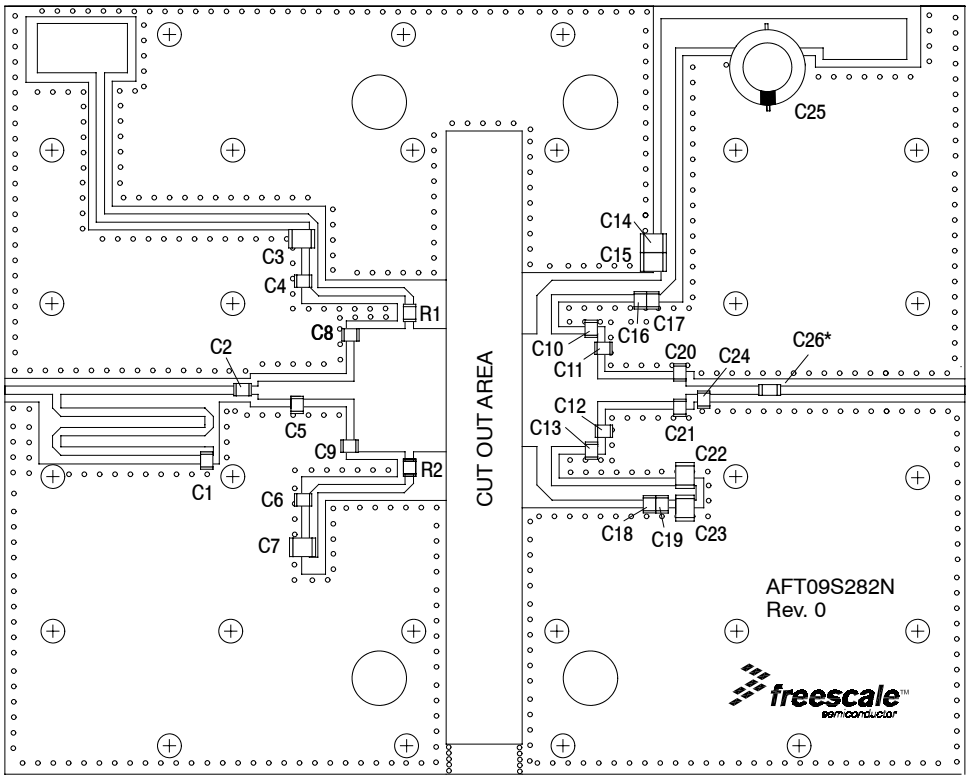
1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.

(continued)

Table 5. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, P_{out} = 80 W Avg., f = 960 MHz, Single-Carrier W-CDMA, IQ Magnitude Clipping, Input Signal PAR = 7.5 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	19.0	20.0	22.0	dB
Drain Efficiency	η_D	33.5	36.1	—	%
Output Peak-to-Average Ratio @ 0.01% Probability on CCDF	PAR	5.6	6.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	-37.5	-36.0	dBc
Input Return Loss	IRL	—	-17	-10	dB
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQ} = 1400 mA, f = 940 MHz					
VSWR 10:1 at 32 Vdc, 416 W CW Output Power (3 dB Input Overdrive from 280 W CW Rated Power)		No Device Degradation			
Typical Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, 920-960 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	280	—	W
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	60	—	MHz
Gain Flatness in 40 MHz Bandwidth @ P_{out} = 80 W Avg.	G_F	—	0.1	—	dB
Gain Variation over Temperature (-30°C to +85°C)	ΔG	—	0.0156	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	ΔP1dB	—	0.006	—	dB/°C

1. Part internally matched both on input and output.



*C26 is mounted vertically.

Figure 2. AFT09S282NR3 Test Circuit Component Layout

Table 6. AFT09S282NR3 Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1	62 pF Chip Capacitor	ATC100B620JT500XT	ATC
C2, C5, C10, C13	4.7 pF Chip Capacitors	ATC600F4R7BT250XT	ATC
C3, C7, C14, C15, C22, C23	10 μF Chip Capacitors	GRM32ER71H106KA12L	Murata
C4, C6, C16, C17, C18, C19	47 pF Chip Capacitors	ATC600F470JT250XT	ATC
C8, C9, C11, C24	3.9 pF Chip Capacitors	ATC600F3R9BT250XT	ATC
C12, C20, C21	2.4 pF Chip Capacitors	ATC600F2R4BT250XT	ATC
C25	470 μF, 63 V Electrolytic Capacitor	MCGPR63V477M13X26-RH	Multicomp
C26	36 pF Chip Capacitor	ATC100B360JT500XT	ATC
R1, R2	6.04 Ω, 1/4 W Chip Resistor	CRCW12066R04FKEA	Vishay
PCB	0.020″, ε_r = 3.5	RO4350	Rogers

TYPICAL CHARACTERISTICS

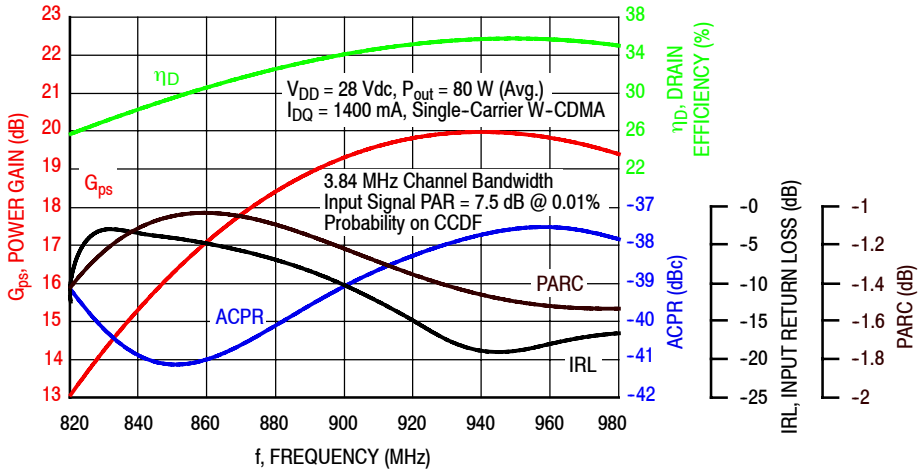


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 80 Watts Avg.

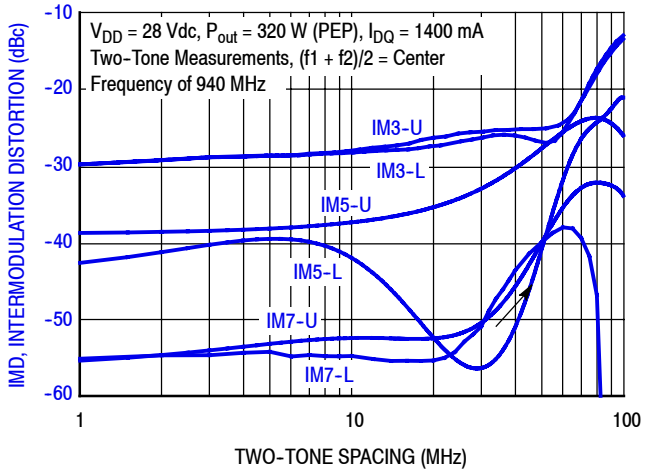


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

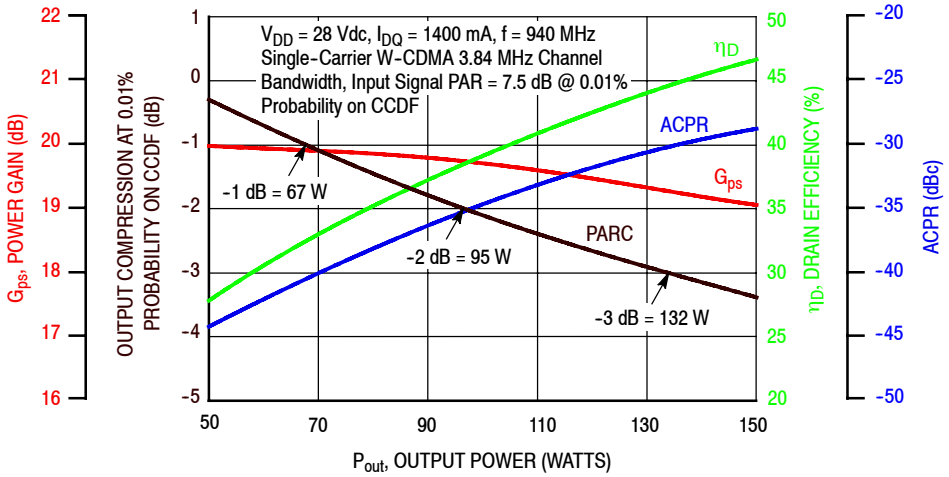


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS

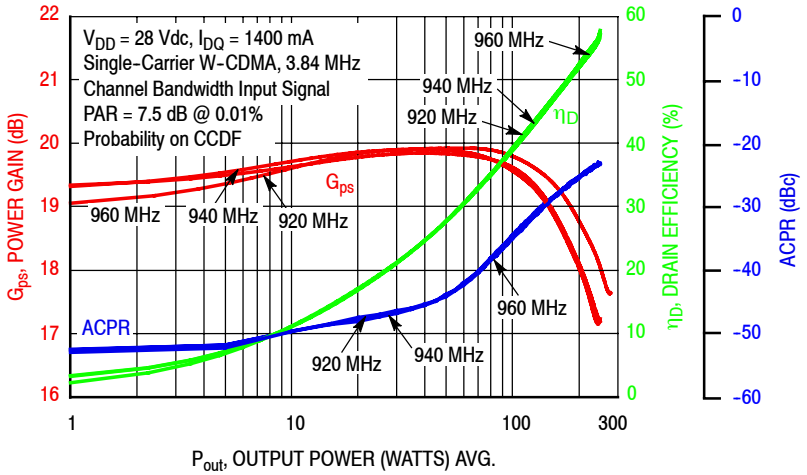


Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

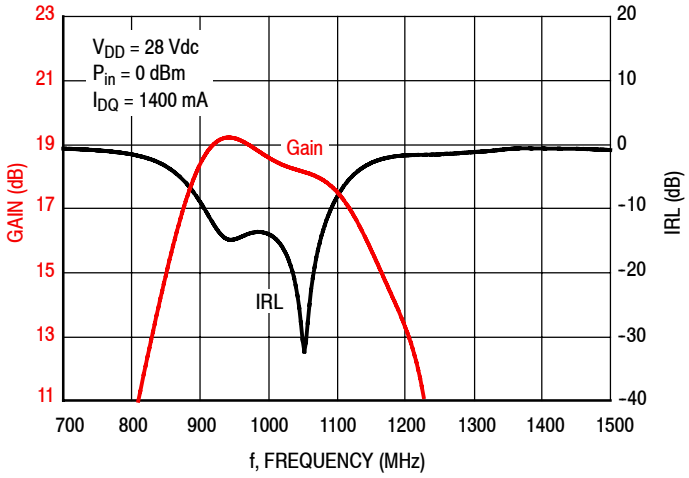


Figure 7. Broadband Frequency Response

V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Max Linear Gain (dB)	Max Output Power							
					P1dB				P3dB			
					(dBm)	(W)	η_D (%)	AM/PM (°)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	1.83 - j3.18	1.66 + j3.17	4.55 - j3.27	18.7	56.0	396	53.5	-8.0	56.9	494	58.2	-12
940	2.01 - j3.27	2.03 + j3.31	4.97 - j2.86	18.7	55.9	391	54.4	-7.7	56.9	490	57.6	-11
960	2.64 - j3.34	2.55 + j3.45	5.77 - j1.78	18.4	55.9	391	53.9	-7.9	56.9	488	57.8	-12

(1) Load impedance for optimum P1dB power.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

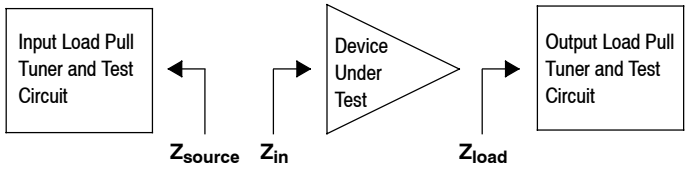


Figure 8. Load Pull Performance — Maximum P1dB Tuning

V_{DD} = 28 Vdc, I_{DQ} = 1400 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Z_{load} (1) (Ω)	Max Linear Gain (dB)	Max Drain Efficiency							
					P1dB				P3dB			
					(dBm)	(W)	η_D (%)	AM/PM (°)	(dBm)	(W)	η_D (%)	AM/PM (°)
920	1.83 - j3.18	1.70 + j3.02	1.49 - j1.61	22.0	53.5	225	66.2	-15	54.3	267	69.6	-22
940	2.01 - j3.27	2.12 + j3.16	1.48 - j1.80	22.0	53.3	215	66.6	-16	54.0	248	70.1	-24
960	2.64 - j3.34	2.66 + j3.26	1.76 - j1.79	21.7	53.6	230	67.4	-15	54.3	269	70.6	-22

(1) Load impedance for optimum P1dB efficiency.

Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

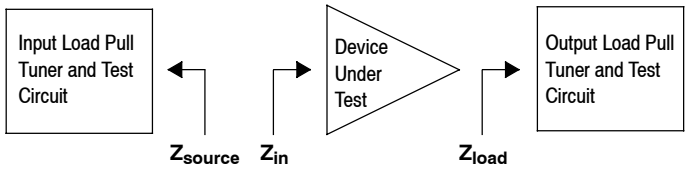


Figure 9. Load Pull Performance — Maximum Drain Efficiency Tuning

P1dB - TYPICAL LOAD PULL CONTOURS — 940 MHz

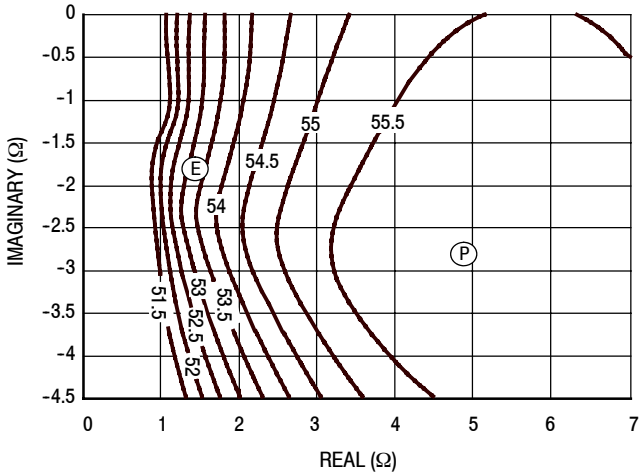


Figure 10. P1dB Load Pull Output Power Contours (dBm)

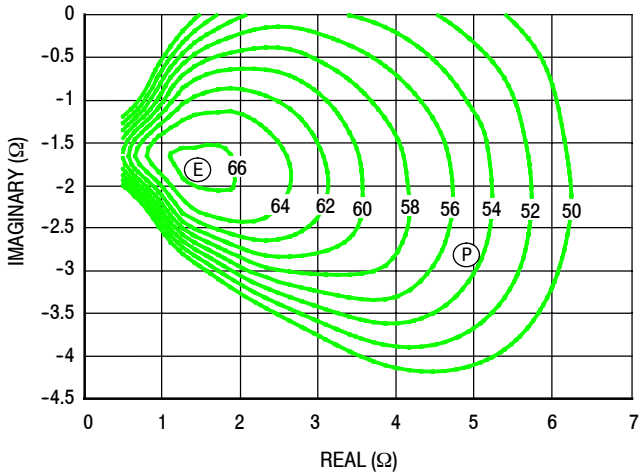


Figure 11. P1dB Load Pull Efficiency Contours (%)

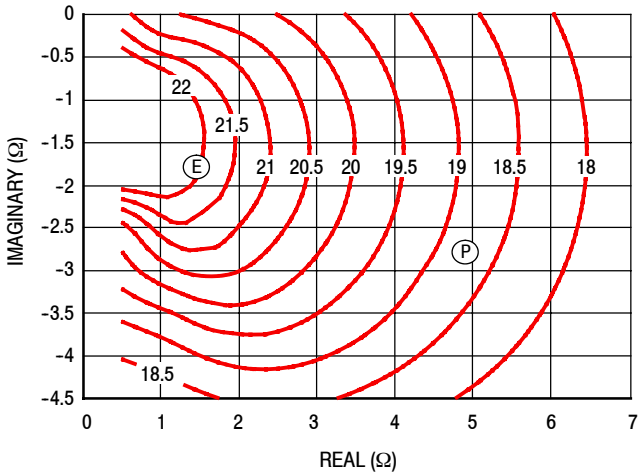


Figure 12. P1dB Load Pull Gain Contours (dB)

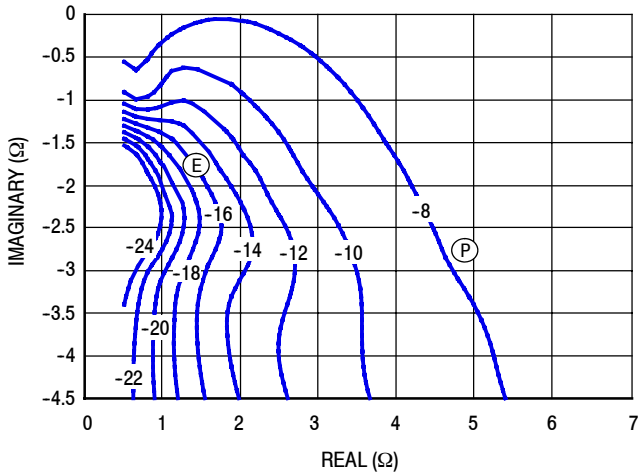


Figure 13. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Power Gain

Drain Efficiency

Linearity

Output Power

P3dB - TYPICAL LOAD PULL CONTOURS — 940 MHz

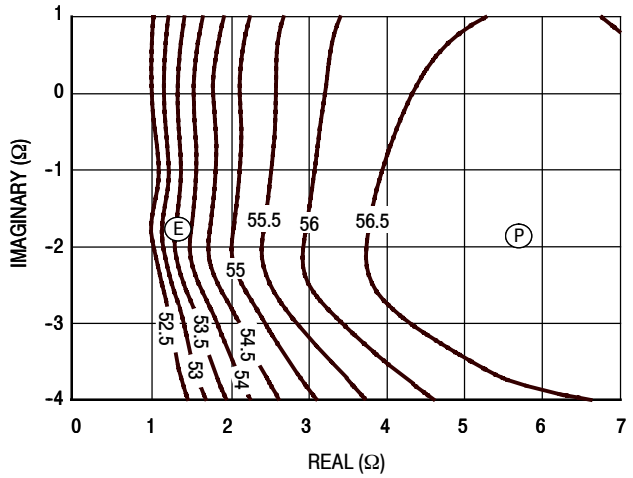


Figure 14. P3dB Load Pull Output Power Contours (dBm)

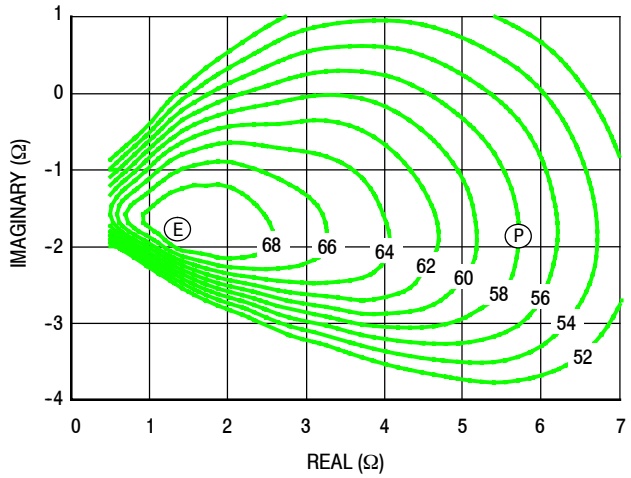


Figure 15. P3dB Load Pull Efficiency Contours (%)

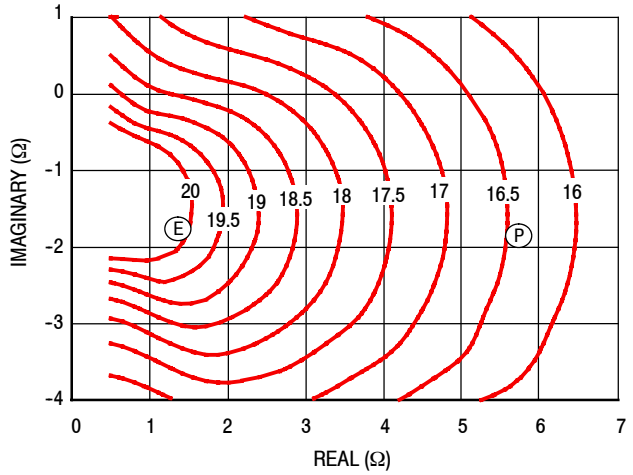


Figure 16. P3dB Load Pull Gain Contours (dB)

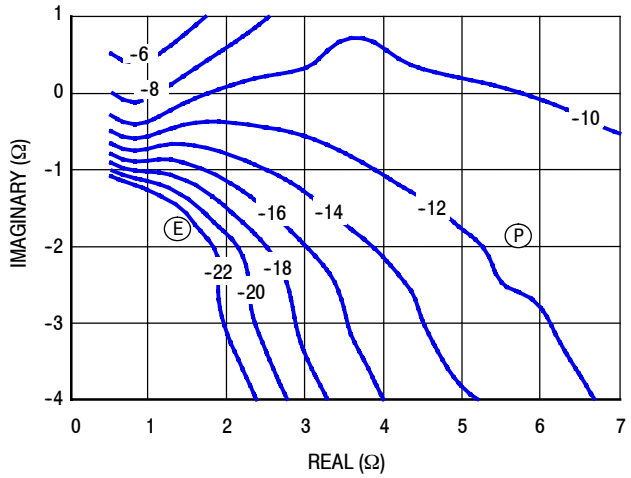


Figure 17. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

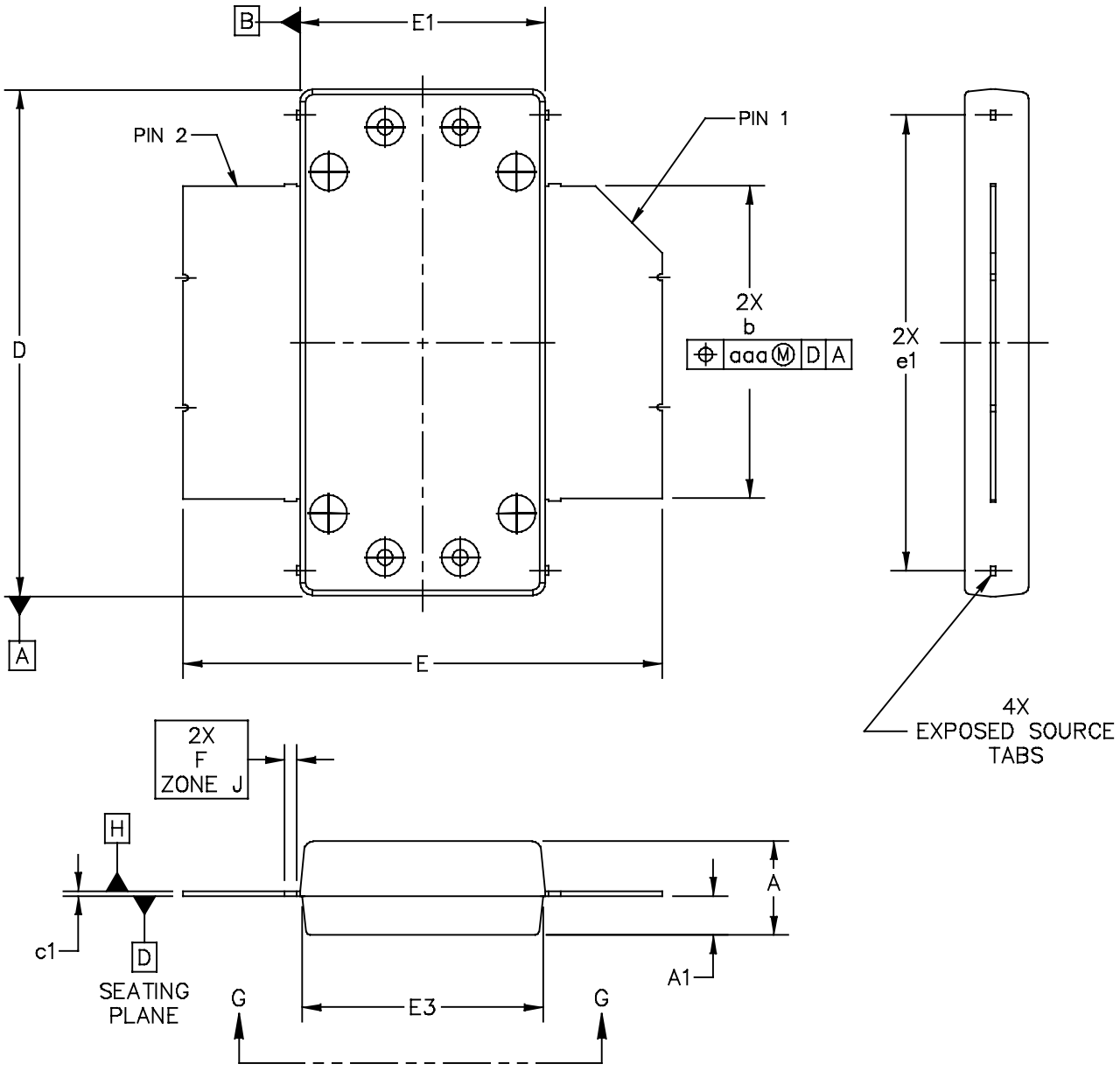
Power Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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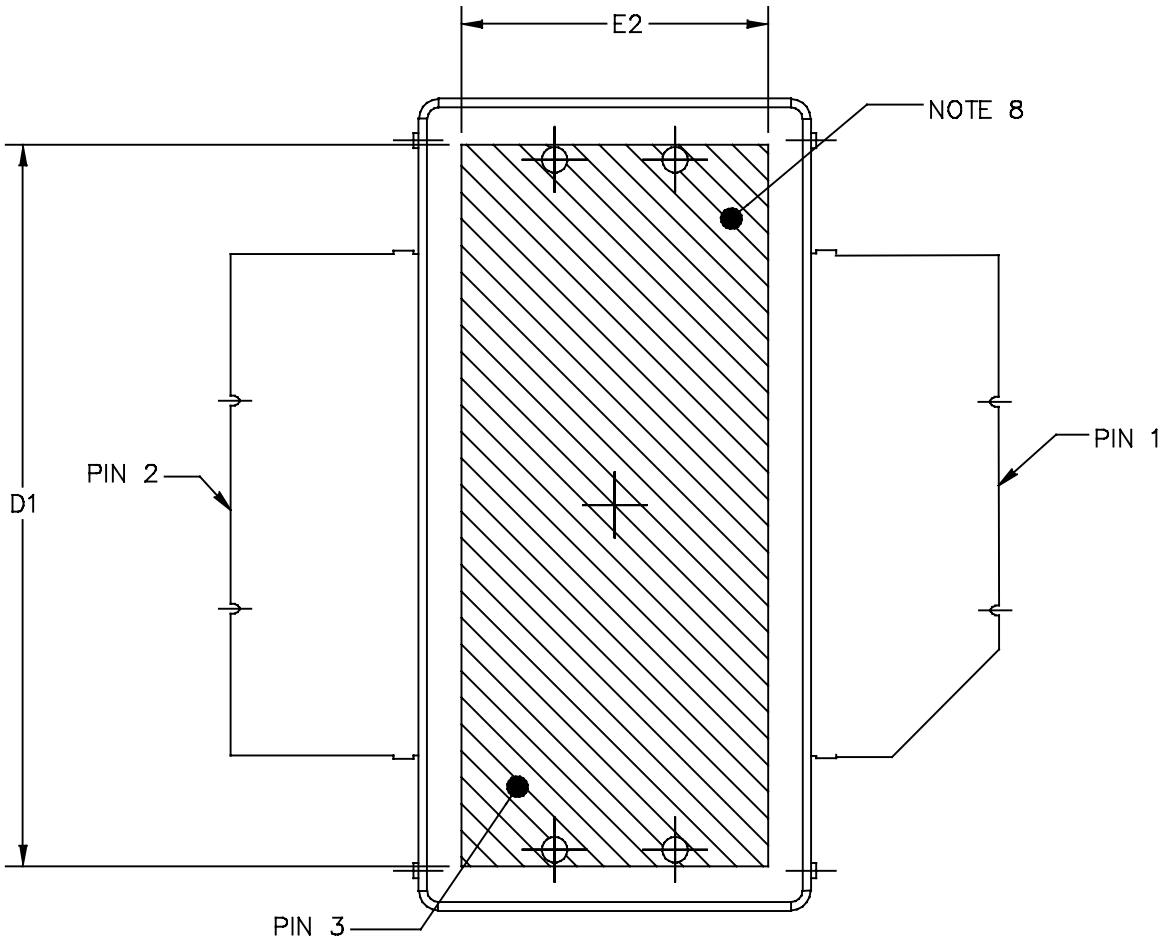
	CASE NUMBER: 2021-03	22 OCT 2009
	STANDARD: NON-JEDEC	



BOTTOM VIEW
VIEW G–G

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	CASE NUMBER: 2021–03	22 OCT 2009
	STANDARD: NON–JEDEC	

NOTES:
1. CONTROLLING DIMENSION: INCH

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DATUM PLANE –H– IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.

4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –H–.

5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

6. DATUMS –A– AND –B– TO BE DETERMINED AT DATUM PLANE –H–.

7. DIMENSION A1 APPLIES WITHIN ZONE "J" ONLY

8. HATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG. THE DIMENSIONS D1 AND E2 REPRESENT THE VALUES BETWEEN THE TWO OPPOSITE POINTS ALONG THE EDGES OF EXPOSED AREA OF HEAT SLUG.

STYLE 1:
PIN 1 – DRAIN
PIN 2 – GATE
PIN 3 – SOURCE

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
A	0.148	.152	3.76	3.86	b	.497	.503	12.62	12.78
A1	.059	.065	1.50	1.65	c1	.007	.011	0.18	0.28
D	.808	.812	20.52	20.62	e1	.721	.729	18.31	18.52
D1	.720	----	18.29	----					
E	.762	.770	19.36	19.56	aaa	.004		0.10	
E1	.390	.394	9.91	10.01					
E2	.306	----	7.77	----					
E3	.383	.387	9.73	9.83					
F	.025 BSC		0.635 BSC						

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TITLE:	DOCUMENT NO: 98ASA10831D	REV: B
OM780–2 STRAIGHT LEAD	CASE NUMBER: 2021–03	22 OCT 2009
	STANDARD: NON–JEDEC	

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Oct. 2012	• Initial Release of Data Sheet

How to Reach Us:

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Rev. 0, 10/2012