ZL30260–ZL30263

1-APLL, 6- or 10-Output Any-to-Any Clock Multiplier and Frequency Synthesizer

Product Brief

September 2016

Features

- **4 Flexible Input Clocks**
  - One crystal/CMOS input
  - Two differential/CMOS inputs
  - One single-ended/CMOS input
  - Any input frequency from 9.72MHz to 1.25GHz (300MHz max for CMOS)
  - Activity monitors, automatic or manual switching
  - Glitchless clock switching by pin or register
- **6 or 10 Any-Frequency, Any-Format Outputs**
  - Any output frequency from 1Hz to 1045MHz
  - High-resolution frac-N APLL with 0ppm error
  - The APLL has a fractional divider and an integer divider to make two independent frequency families
  - Output jitter from the integer divider as low as 0.17ps RMS (12kHz-20MHz)
  - Output jitter from fractional dividers is typically < 1ps RMS, many frequencies <0.5ps RMS
  - Each output has an independent divider
  - Each output configurable as LVDS, LVPECL, HCSL, 2xCMOS or HSTL
  - In 2xCMOS mode, the P and N pins can be different frequencies (e.g. 125MHz and 25MHz)
  - Multiple output supply voltage banks with CMOS output voltages from 1.5V to 3.3V
  - Precise output alignment circuitry and per-output phase adjustment

Ordering Information

ZL30260	ext. EEPROM	6 Outputs	8x8mm QFN
ZL30261	int. EEPROM	6 Outputs	8x8mm QFN
ZL30262	ext. EEPROM	10 Outputs	8x8mm QFN
ZL30263	int. EEPROM	10 Outputs	8x8mm QFN

Matte Tin

-40°C to +85°C

  - Per-output enable/disable and glitchless start/stop (stop high or low)
- **General Features**
  - Automatic self-configuration at power-up from external (ZL30260 or 2) or internal (ZL30261 or 3) EEPROM; up to 8 configurations pin-selectable
  - External feedback for zero-delay applications
  - Numerically controlled oscillator mode
  - Spread-spectrum modulation mode
  - Easy-to-configure design requires no external VCXO or loop filter components
  - SPI or I^2C processor Interface
  - Core supply voltage options: 2.5V only, 3.3V only, 1.8V+2.5V or 1.8V+3.3V
  - Space-saving 8x8mm QFN56 (0.5mm pitch)
  - Easy-to-use evaluation/programming software

Applications

- Frequency conversion and frequency synthesis in a wide variety of equipment types

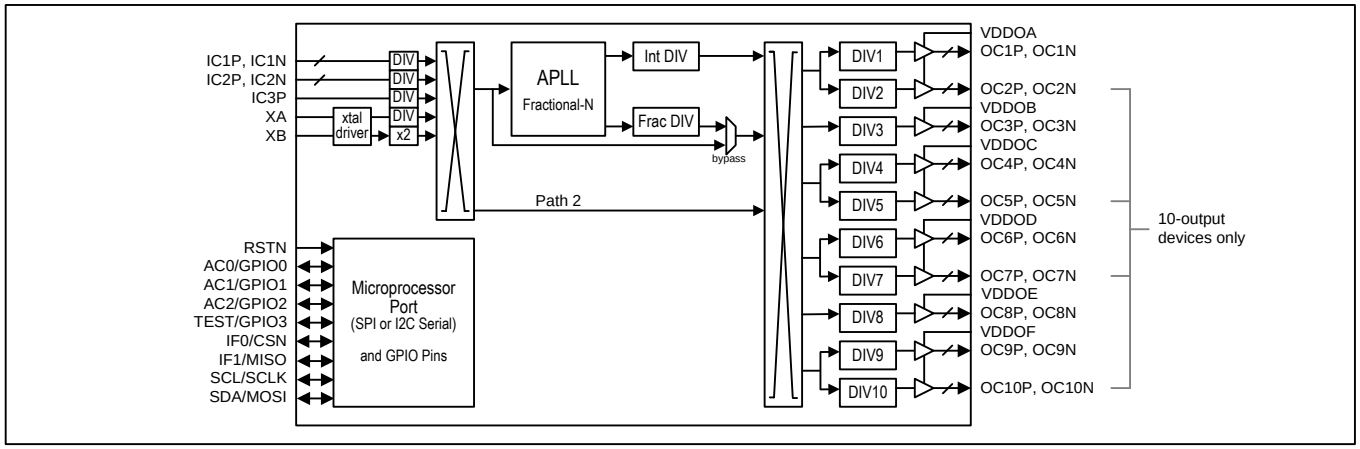


Figure 1 - Functional Block Diagram

1. Application Example

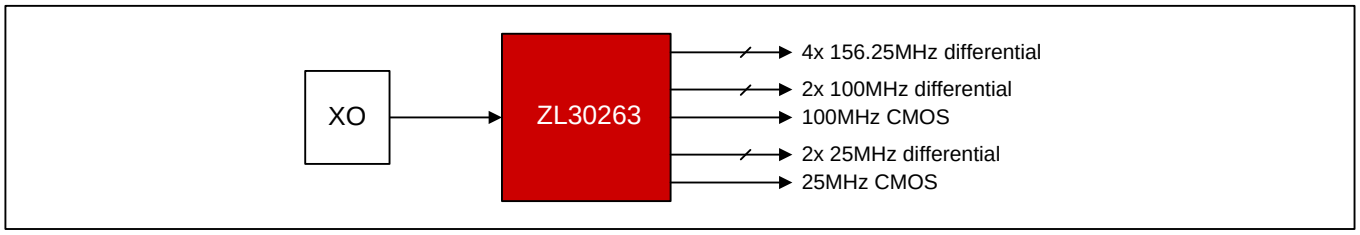


Figure 2 – PCIe and Ethernet Clocks for Server Application

2. Detailed Features

2.1 Input Clock Features

- Four input clocks: one crystal/CMOS, two differential/CMOS, one single-ended/CMOS
- Input clocks can be any frequency from 9.72MHz to 1250MHz (differential) or 300MHz (single-ended)
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN, wireless
- Activity monitor and glitchless input switching

2.2 APLL Features

- Very-high-resolution fractional (i.e. non-integer) frequency multiplication
- Any-to-any frequency conversion with 0ppm error
- Two APLL output dividers: one integer divider (4 to 15 plus half divides 4.5 to 7.5) and one fractional
- Easy-to-configure, completely encapsulated design requires no external VCXO or loop filter
- Bypass mode supports system testing

2.3 Output Clock Features

- Six (ZL30260 or ZL30261) or ten (ZL30262 or ZL30263) low-jitter output clocks
- Each output can be one differential output or two CMOS outputs
- Output clocks can be any frequency from 1Hz to 1035MHz (250MHz max for HCSL, CMOS and HSTL)
- Output jitter from integer multiply and integer dividers as low as 0.17ps RMS (12kHz to 20MHz)
- Output jitter from fractional dividers is typically <1ps RMS, many frequencies <0.5ps RMS (12kHz to 20MHz)
- In CMOS mode, the OCxP and OCxN pins can be different divisors (Example 1: OC3P 125MHz, OC3N 25MHz; Example 2: OC3P 25MHz, OC3N 1Hz/1PPS)
- Outputs directly interface (DC coupled) with LVDS, LVPECL, HSTL, HCSL and CMOS components
- Supported telecom frequencies include PDH, SDH, Synchronous Ethernet, OTN
- Can produce clock frequencies for microprocessors, ASICs, FPGAs and other components
- Can produce PCIe clocks (PCIe generation 1, 2 and 3)
- Sophisticated output-to-output phase alignment
- Per-output phase adjustment
- Per-output enable/disable
- Per-output glitchless start/stop (stop high or low)

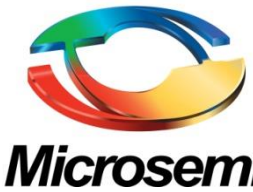
2.4 General Features

- SPI or I^2C serial microprocessor interface
- Automatic self-configuration at power-up; pin control to specify one of 8 stored configurations
  ZL30260 and ZL30262: preset configurations in ROM or user configurations in external EEPROM
  ZL30261 and ZL30263: user configurations in internal EEPROM
- Numerically controlled oscillator (NCO) mode allows system software to steer DPLL frequency with resolution better than 0.01ppb
- Spread-spectrum modulation mode (meets PCI Express requirements)
- Zero-delay buffer configuration using an external feedback path
- Four general-purpose I/O pins each with many possible status and control options

- Reference can be fundamental-mode crystal, low-cost XO or clock signal from elsewhere in the system

2.5 Evaluation Software

- Simple, intuitive Windows-based graphical user interface
- Supports all device features and register fields
- Makes lab evaluation of the ZL30260/1/2/3 quick and easy
- Generates configuration scripts to be stored in external (ZL30260,2) or internal (ZL30261,3) EEPROM
- Generates full or partial configuration scripts to be run on a system processor
- Works with or without an evaluation board



Microsemi Corporate Headquarters
One Enterprise
Aliso Viejo, CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

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