PIC16(L)F18856/18876

PIC16(L)F18856/18876 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F18856/18876 family devices that you have received conform functionally to the current Device Data Sheet (DS40001824**A**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F18856/18876 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision **(A2)**.

Data Sheet clarifications and corrections start on page 4, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F18856/18876 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID (Silicon Revision)(2)
		A2
PIC16F18856	3070h	2002h
PIC16LF18856	3072h	2002h
PIC16F18876	3071h	2002h
PIC16LF18876	3073h	2002h

Note 1: The Revision ID and Device ID are located in the Configuration memory at addresses 8005h and 8006h, respectively.

2: Refer to the *"PIC16(L)F188XX Memory Programming Specification"* (DS40001753) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item No.	Issue Summary	Affected Revision(1)
				A2
Analog-to-Digital Converter with Computation (ADC2)	ADC Conversion	1.1	When using ADRC as ADCC clock source there is a delay of one instruction cycle to set the ADGO bit.	X
NVMREG Access	NVMREG Access	2.1	Self-writes on LF devices below 2.2V at -40°C may not work.	X
EEPROM	Indirect Read	3.1	Indirect read of EEPROM with FSR returns unexpected value.	X
ECCP	Compare Mode	4.1	Toggle mode may output multiple pulses when source clock has a prescaler other than 1:1.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision **(A2)**.

1. Module: Analog-to-Digital Converter (ADC)

1.1 ADC Conversion

When using ADCRC as the ADC as the clock source for ADCC, there is a delay of one instruction cycle between the user setting the ADGO bit and being able to read it set. This can lead to a false conversion complete scenario (i.e., ADGO being cleared), depending if the user code has a bit clear test (BTFSC) instruction on the ADGO bit, immediately after setting the ADGO bit. See code example below.

e.g.

```
BSF ADCON0, ADGO      ; Start conversion
BTFSC ADCON0, ADGO    ; Is conversion done?
GOTO $-1              ; No, test again
```

The BTFSC will pass the very first time in this situation

Work around

Add a NOP instruction after setting the ADGO bit and before testing the bit for completion of conversion. See code example below.

e.g.

```
BSF ADCON0, ADGO      ; Start conversion
NOP
BTFSC ADCON0, ADGO    ; Is conversion done?
GOTO $-1; No, test again
```

Affected Silicon Revisions

A2							
X							

2. Module: Nonvolatile Memory Control

2.1 NVMREG Access

When performing self-writes through NVMREG access on PIC16LF18857/18877 devices with V_{DD} below 2.2V and temperature of -40°C, the writes may not work. This applies to both PFM and EEPROM writes.

Work around

None.

Affected Silicon Revisions

A2							
X							

3. Module: EEPROM

3.1 Indirect Read

Performing FSR reads of Data EEPROM addresses other than the lowest address (FSR=7000h) will return unexpected values.

Work around

Set NVMADRH:L to the desired address (F000h through F0FFh) and retrieve the EEPROM value from the NVMDATL register by setting the NVMREGS and RD bits in the NVMCON1 register.

Affected Silicon Revisions

A2							
X							

4. Module: ECCP

4.1 Compare Mode

The ECCP Compare Toggle modes (CCPxCON<3:0> bits = 0010 or 0001) output multiple pulses instead of a single toggle pulse when its source clock has a prescaler other than 1:1.

Work around

Use CCP Compare mode with pulse output (CCPxCON<3:0> bits = 1011) to clock a CLC configured as a J-K flip-flop in Toggle mode.

Affected Silicon Revisions

A2							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001824**A**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Analog-to-Digital Converter with Computation (ADC2)

In Register 23-3: ADCON2, bit 7: ADPSIS has incorrect descriptions for its bit selections. The correct description is below:

REGISTER 23-3: ADCON2: ADC CONTROL REGISTER 2

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W/HC-0	R/W-0/0	R/W-0/0	R/W-0/0
ADPSIS	ADCRS<2:0>**(2)**			ADACLR	ADMD<2:0>**(1)**		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **ADPSIS**: **ADC Previous Sample Input Select bits**

`1` = **ADFLTR is transfered to ADPREV at start-of-conversion**

`0` = **ADRES is transfered to ADPREV at start-of-conversion**

bit 6-4 ADCRS<2:0>: ADC Accumulated Calculation Right Shift Select bits

`111` = Reserved

`110` = Reserved

`101` through `000`:

If ADMD = `100`:

Low-pass filter time constant is 2^{ADCRS}, filter gain is 1:1

If ADMD = `001`, `010` or `011`:

The accumulated value is right-shifted by ADCRS (divided by 2^{ADCRS})**(2)**

Otherwise:

Bits are ignored

bit 3 ADACLR: ADC Accumulator Clear Command bit

`1` = Initial clear of ADACC, ADAOV, and the sample counter. Bit is cleared by hardware.

`0` = Clearing action is complete (or not started)

bit 2-0 ADMD<2:0>: ADC Operating Mode Selection bits**(1)**

`111` = Reserved

-
-
-

`101` = Reserved

`100` = Low-pass Filter mode

`011` = Burst Average mode

`010` = Average mode

`001` = Accumulate mode

`000` = Basic (Legacy) mode

Note 1: See Table 23-3 for Full-mode descriptions.

2: All results of divisions using the ADCRS bits are truncated, not rounded.

2. Module: Complementary Waveform Generator (CWG)

In Register 20-9: CWGxISM, IS<3:0> has incorrect descriptions for its bit selections. The correct description is below:

bit 7-4 **Unimplemented:** Read as '0'

bit 3-0 **IS<3:0>:** CWGx Input Selection bits

1111 = LC4_out
1110 = LC3_out
1101 = LC2_out
1100 = LC1_out
1011 = DSM_out
1010 = C2OUT_sync
1001 = C1OUT_sync
1000 = NCO1_out
0111 = PWM7_out
0110 = PWM6_out
0101 = CCP5_out
0100 = CCP4_out
0011 = CCP3_out
0010 = CCP2_out
0001 = CCP1_out
0000 = CWGxIN PPS

3. Module: Signal Measurement Timer (SMT)

The description for the Counter mode of the SMT given in 32.6.9 contains incorrect information, given the setup described earlier in the chapter. The corrected text is as follows:

This mode increments the timer on each pulse of the SMTx_signal input. This mode is asynchronous to the SMT clock and uses the SMTx_signal as a time source. The SMTxCPW register will be updated with the current SMTxTMR value on the **falling** edge of the SMTxWIN input.

4. Module: Signal Measurement Timer (SMT)

Several timing diagrams in the Signal Measurement Timer chapter (namely Figures 32-14, 32-15, and 32-18) contain inaccuracies. The correct versions of these timing diagrams are below.

FIGURE 32-14: TIME OF FLIGHT MODE REPEAT ACQUISITION TIMING DIAGRAM

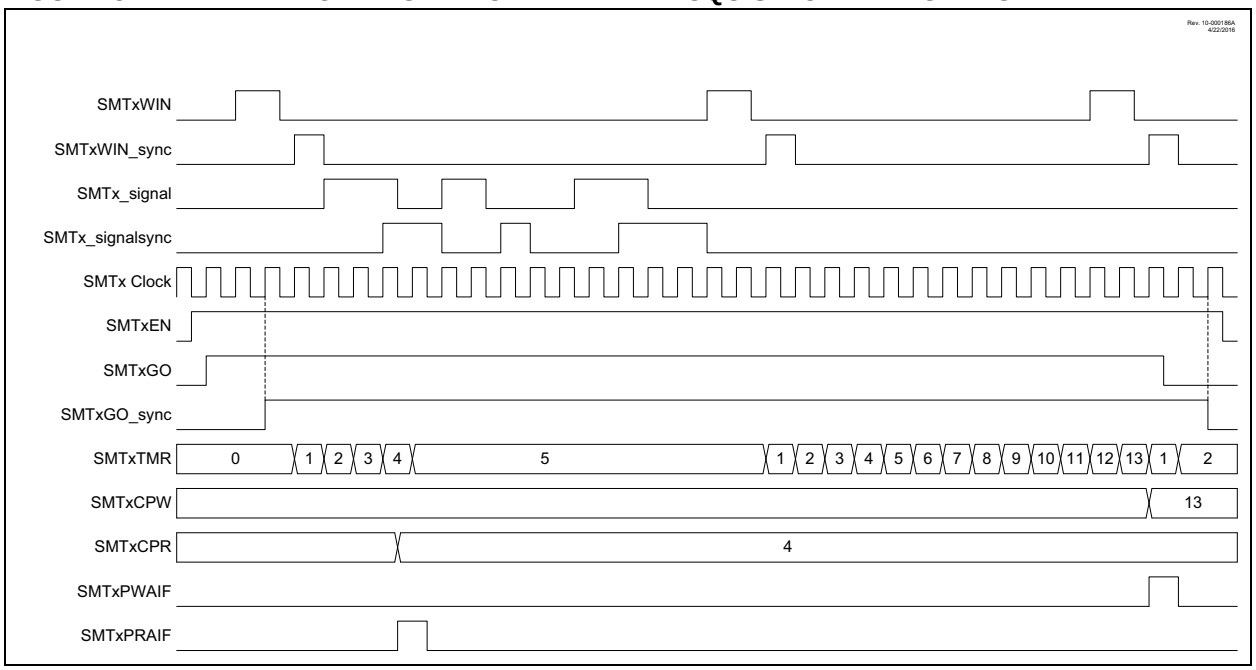


FIGURE 32-15: TIME OF FLIGHT MODE SINGLE ACQUISITION TIMING DIAGRAM

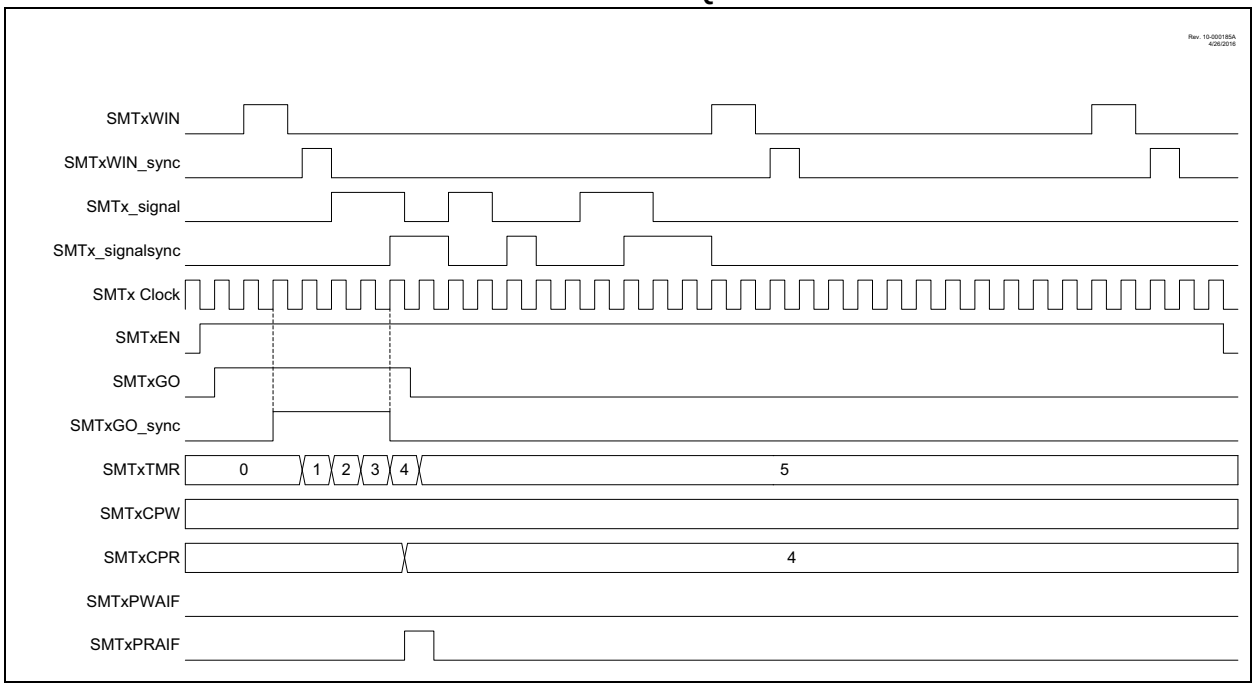
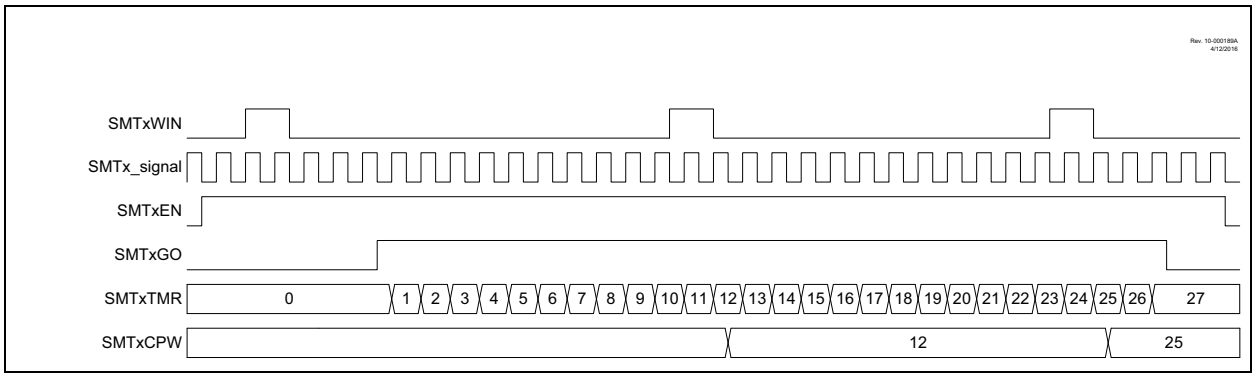


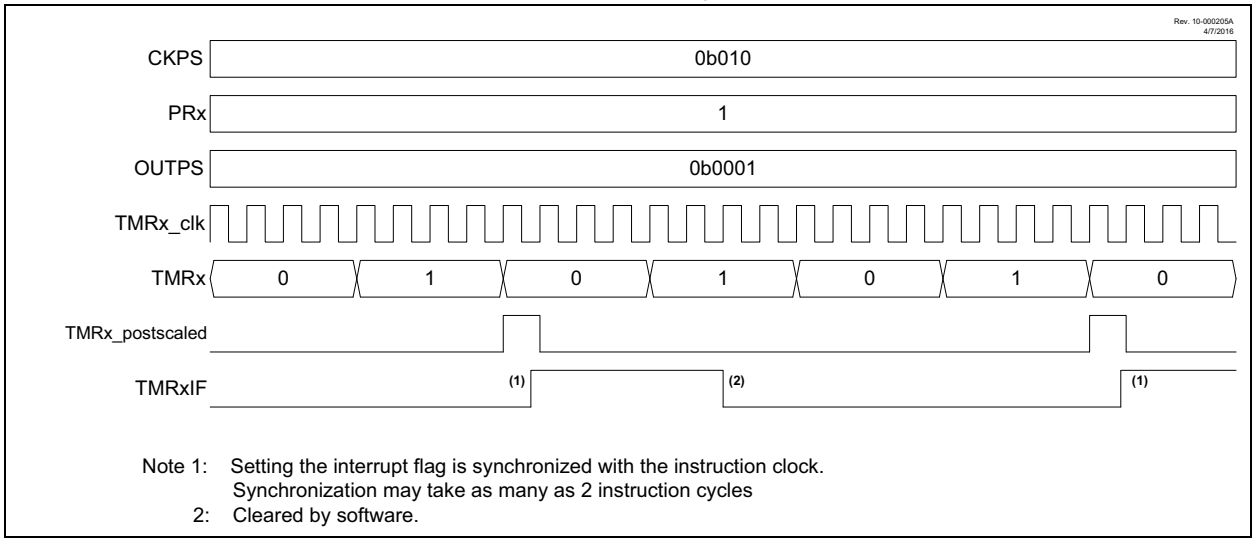
FIGURE 32-18: COUNTER MODE TIMING DIAGRAM



5. Module: Timer2/4/6

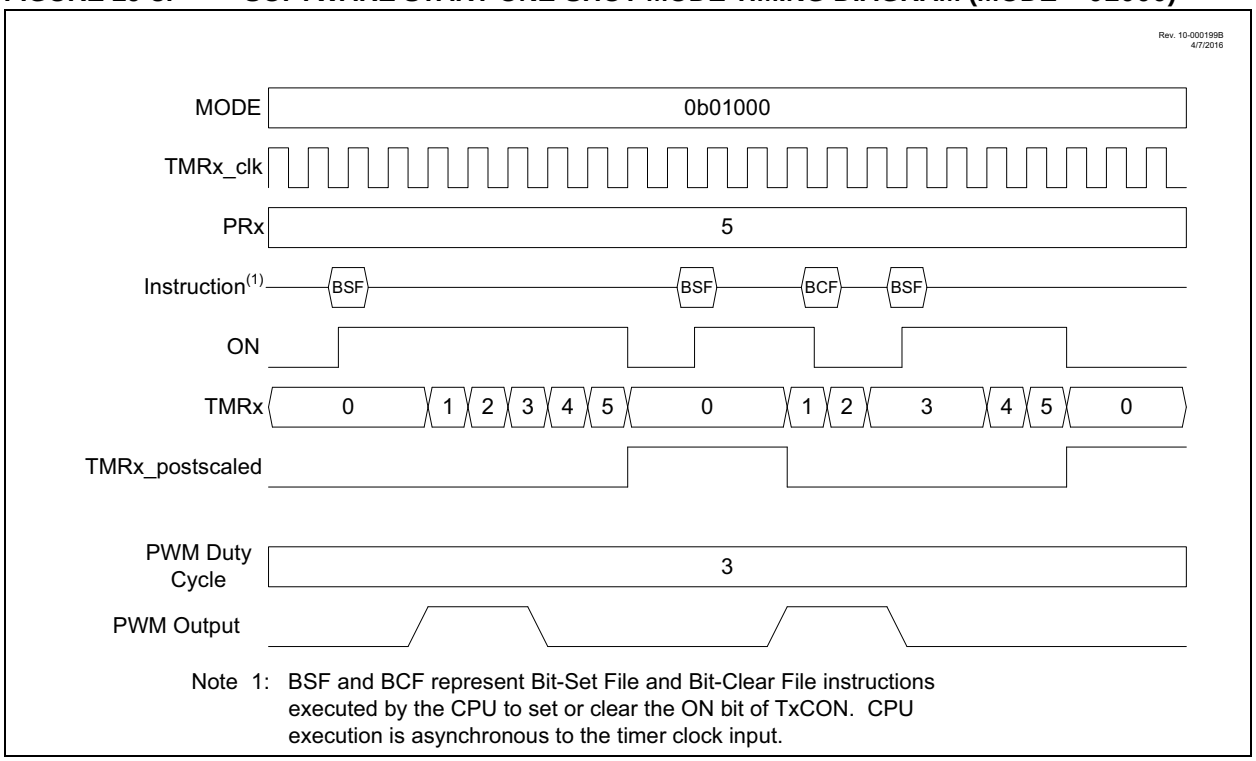
Several timing diagrams in the Timer2/4/6 chapter (namely Figure 29-3, as well as Figures 29-8 through 29-13) contain inaccuracies. The correct timing diagrams are shown below.

FIGURE 29-3: TIMER2 PRESCALER POSTSCALER, AND INTERRUPT TIMING DIAGRAM



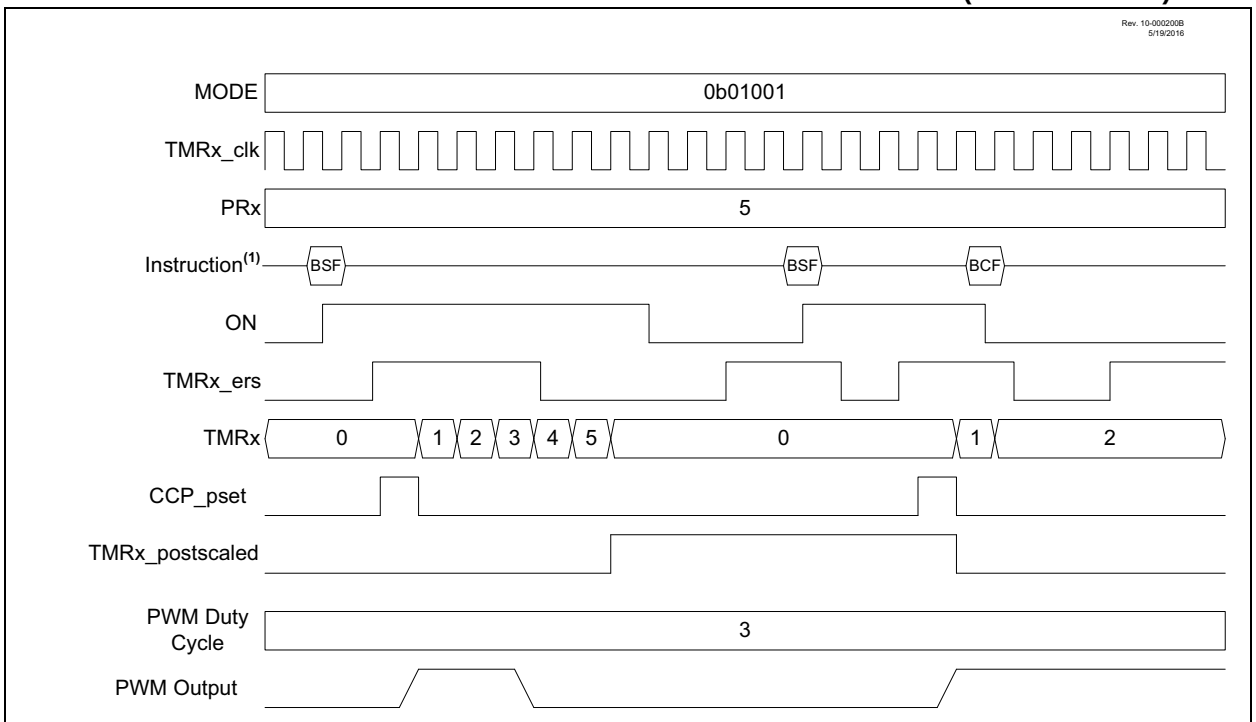
Note 1: Setting the interrupt flag is synchronized with the instruction clock. Synchronization may take as many as 2 instruction cycles
2: Cleared by software.

FIGURE 29-8: SOFTWARE START ONE-SHOT MODE TIMING DIAGRAM (MODE = 01000)



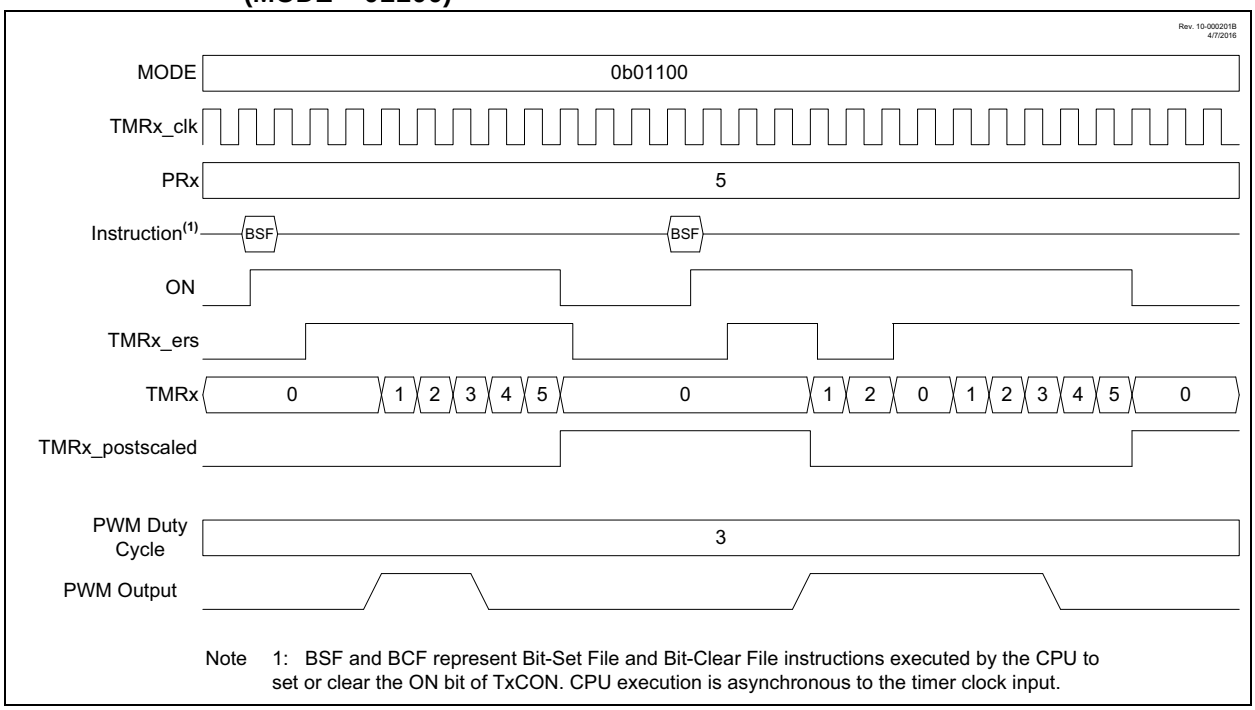
Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

FIGURE 29-9: EDGE-TRIGGERED ONE-SHOT MODE TIMING DIAGRAM (MODE = 01001)



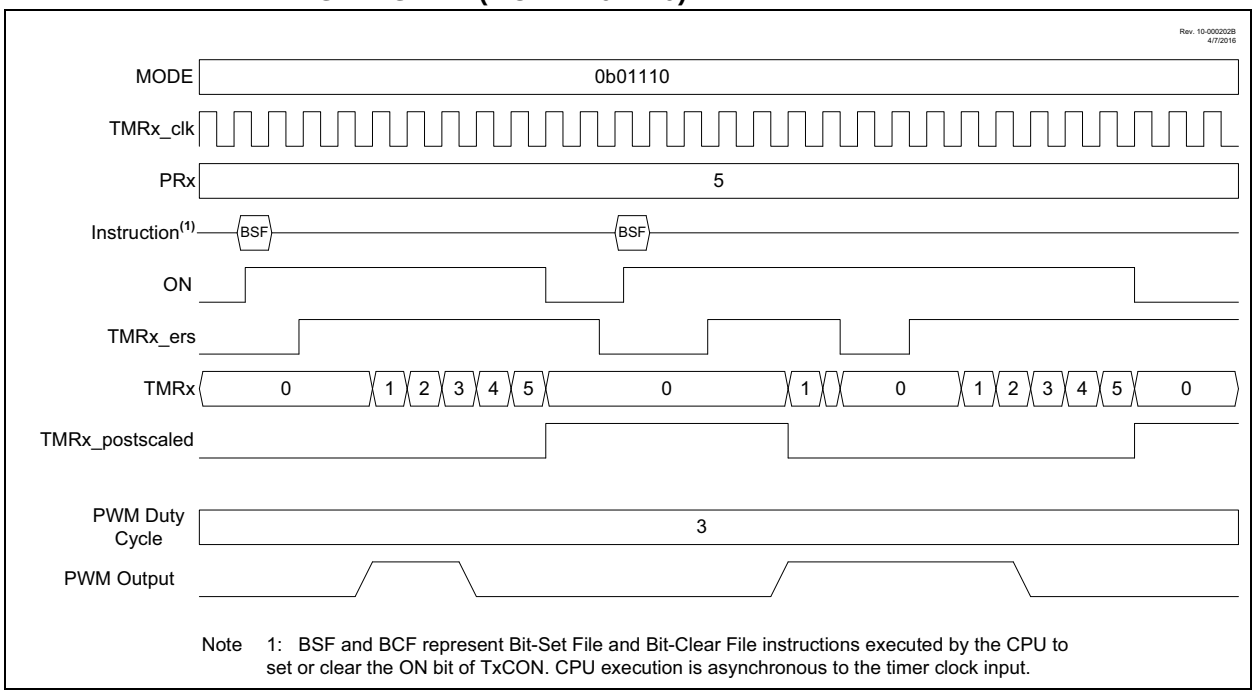
Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

FIGURE 29-10: EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE TIMING DIAGRAM (MODE = 01100)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

FIGURE 29-11: LOW LEVEL RESET, EDGE-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE TIMING DIAGRAM (MODE = 01110)



Note 1: BSF and BCF represent Bit-Set File and Bit-Clear File instructions executed by the CPU to set or clear the ON bit of TxCON. CPU execution is asynchronous to the timer clock input.

FIGURE 29-12: RISING EDGE-TRIGGERED MONOSTABLE MODE TIMING DIAGRAM (MODE = 10001)

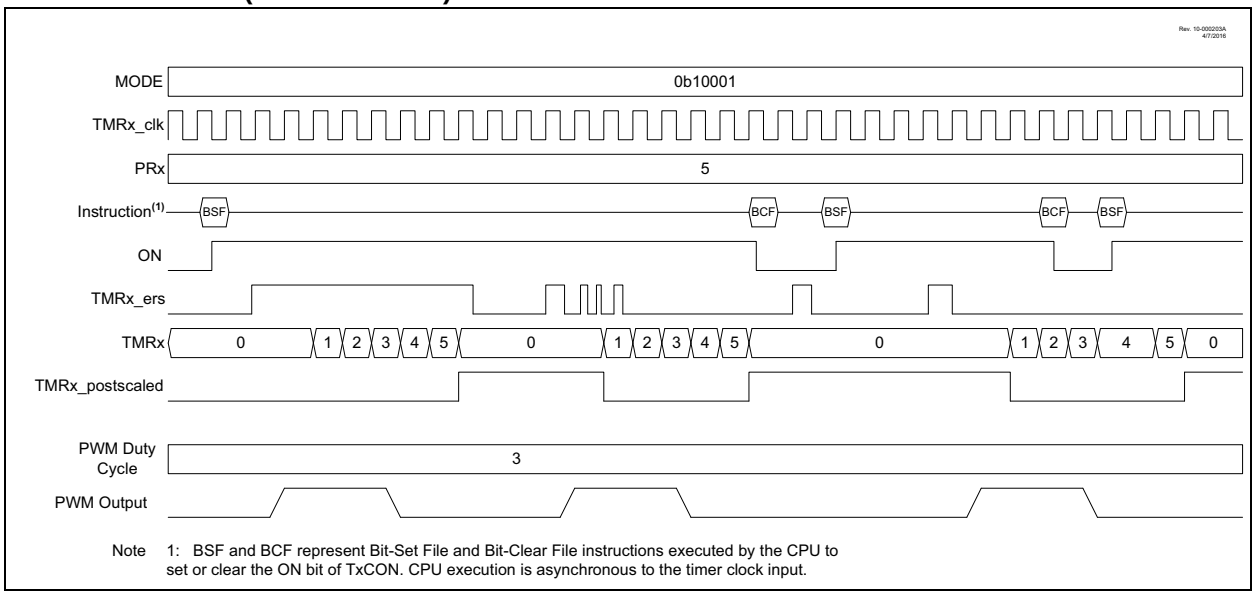
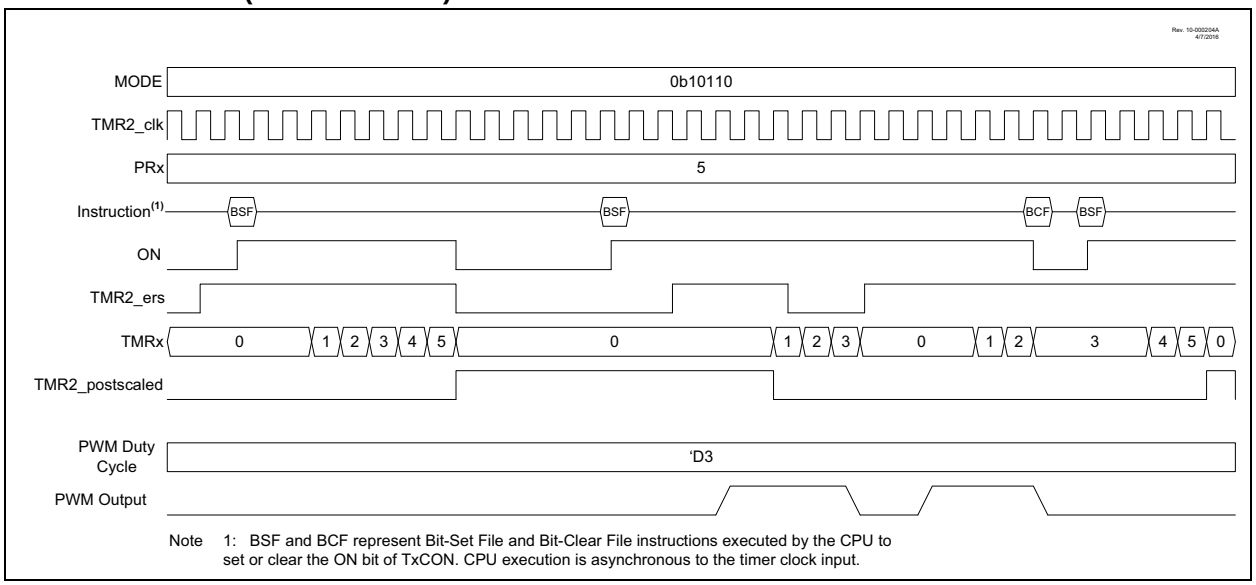


FIGURE 29-13: LEVEL-TRIGGERED HARDWARE LIMIT ONE-SHOT MODE TIMING DIAGRAM (MODE = 10110)



6. Module: Nonvolatile Memory (NVM) Control

Tables 10-2 and 10-3 contain several inaccuracies and should be as follows:

TABLE 10-2: NVM ORGANIZATION AND ACCESS INFORMATION

Master Values			NVMREG Access			FSR Access	
Memory Function	**Program Counter (PC), ICSP™ Address**	**Memory Type**	**NVMREGS bit (NVMCON1)**	**NVMADR <14:0>**	**Allowed Operations**	**FSR Address**	**FSR Programming Address**
Reset Vector	0000h	PFM	0	0000h	Read Write	8000h	Read-Only
User Memory	0001h		0	0001h		8001h	
	0003h			0003h		8003h	
INT Vector	0004h		0	0004h		8004h	
User Memory	0005h		0	0005h		8005h	
	07FFh			07FFh		FFFFh	
User ID	8000h	PFM	1	0000h	Read	No Access	
	8003h			0003h	Write		
Reserved	8004h	—	–	0004h	—		
Rev ID	8005h	PFM	1	0005h	**Read-Only**		
Device ID	8006h		1	0006h			
CONFIG1	8007h		1	0007h	**Read Write**		
CONFIG2	8008h		1	0008h			
CONFIG3	8009h		1	0009h			
CONFIG4	800Ah		1	000Ah			
CONFIG5	800Bh		1	000Bh	Read Write		
User Memory	F000h	EEPROM	1	**F000h**		**7000h**	Read-Only
	F0FFh			**F0FFh**		**70FFh**	

7. Module: Analog-to-Digital Converter with Computation (ADC^2)

Section 23.5.2 “Basic Mode” is inconsistent with Table 23-3 and contains inaccuracies. The correct text of this section should read:

Basic mode (ADMD = 000) disables all additional computation features. In this mode, no accumulation occurs. Double sampling, Continuous mode, all CVD features, **and threshold error detection** are still available, but no features involving the digital filter/average features are used.

8. Module: Analog-to-Digital Converter with Computation (ADC^2)

Section 23.5.3 “Accumulate Mode” is inconsistent with Table 23-3 and contains inaccuracies. The correct text of this section should read:

In Accumulate mode (ADMD = 001), the ADC conversion result is **added to the ADACC registers**. The Formatting mode does not affect the right-justification of the ADACC value. Upon each sample, ADCNT is incremented, indicating the number of samples accumulated. After each sample and accumulation, **the ADFLTR register is updated with the value of ADACC right shifted by the ADCRS value, a threshold comparison is performed** (see Section 23.5.7 “Threshold Comparison”), and the ADTIF interrupt may trigger.

9. Module: Timer0

In Register 27-2: T0CON1, T0CS<2:0> has incorrect descriptions for its bit selections. The correct description is below:

111 = **Reserved**

110 = **LC1_out**

101 = **SOSC**

100 = LFINTOSC

011 = HFINTOSC

010 = FOSC/4

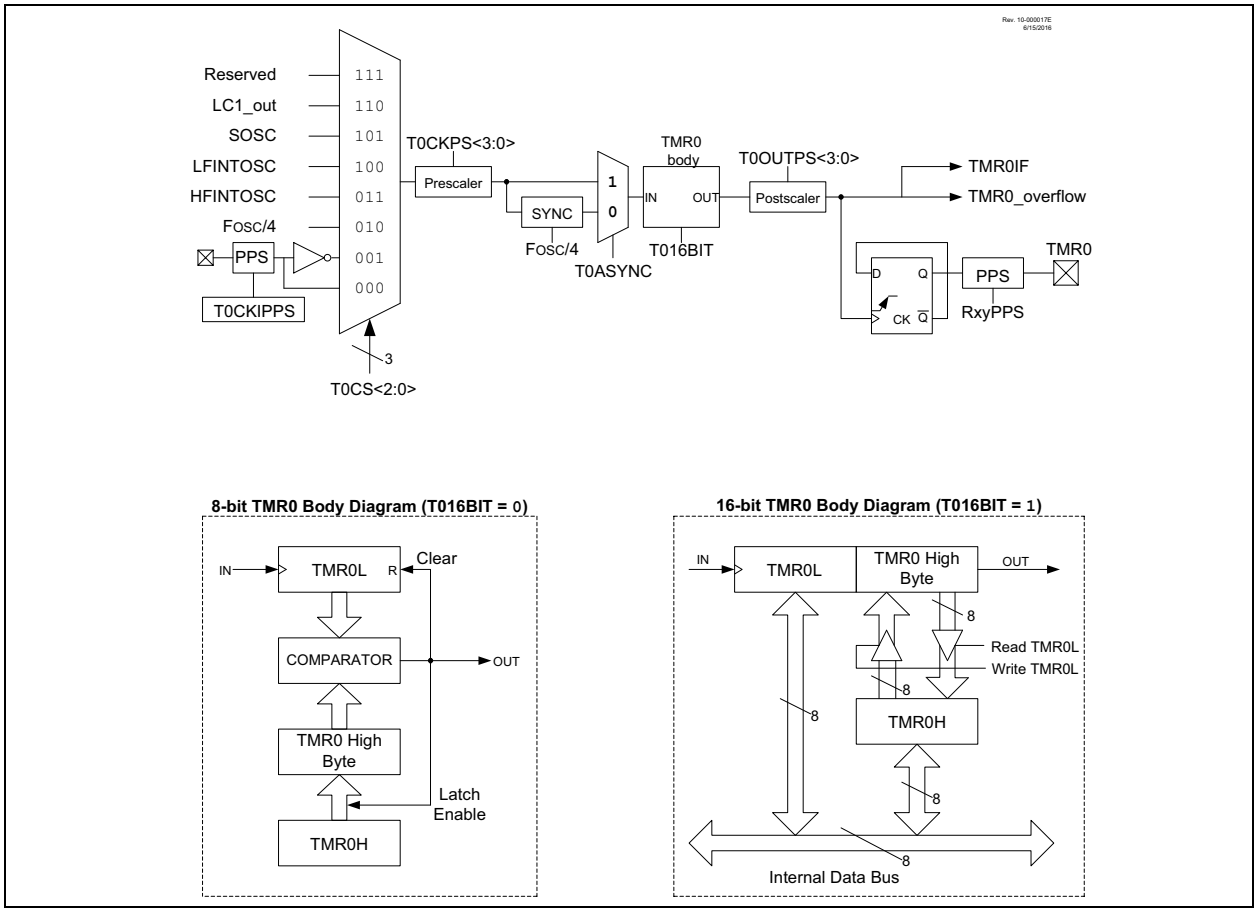
011 = T0CKIPPS (Inverted)

000 = T0CKIPPS (True)

10. Module: Timer0

Figure 27-1: Block Diagram of Timer0 is inaccurate; the correct diagram is below:

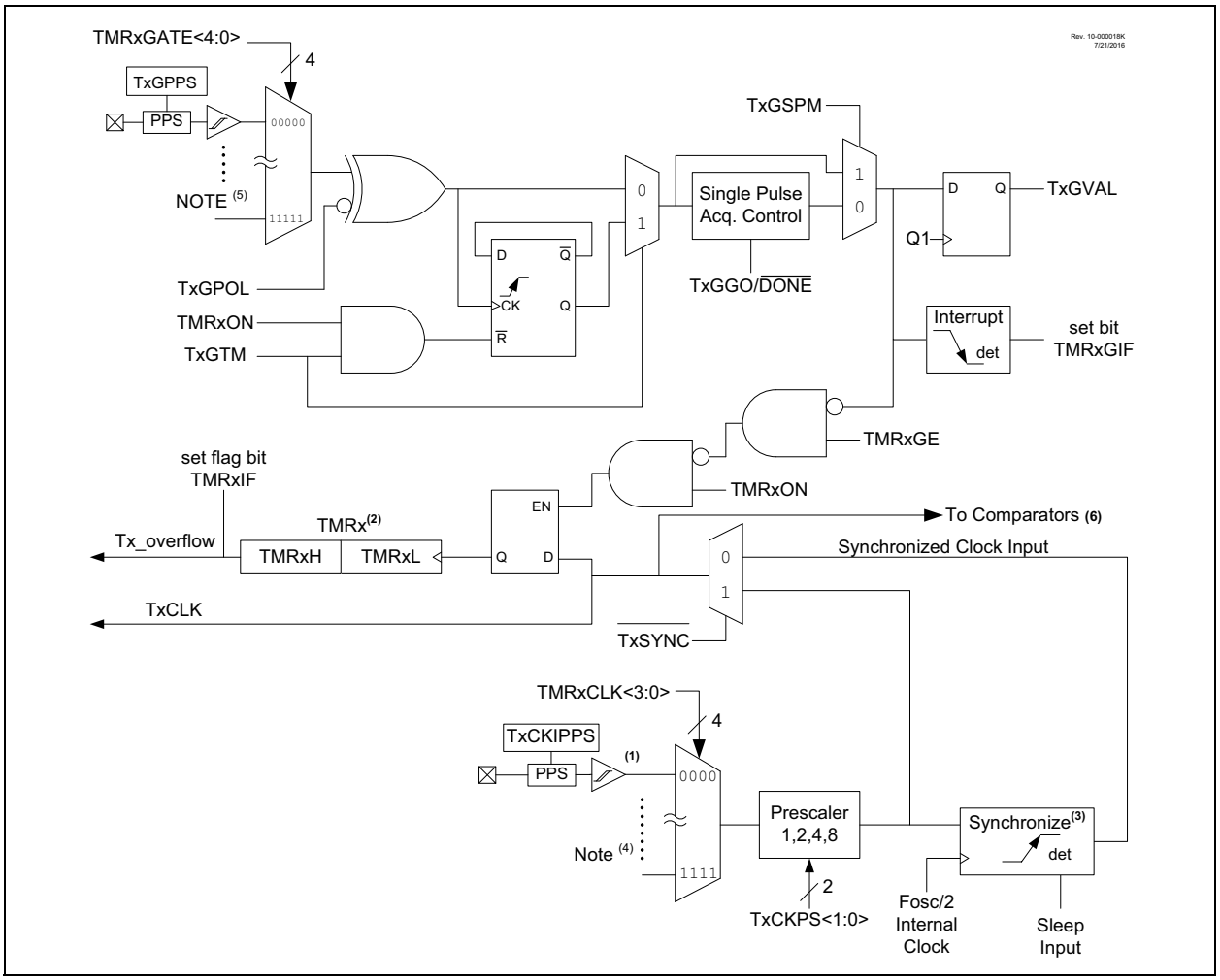
FIGURE 27-1: BLOCK DIAGRAM OF TIMER0



11. Module: Timer1

Figure 28-1 is incorrect. The correct diagram is below:

FIGURE 28-1: TIMER1



12. Module: Timer1

Bit RD16 of TXCON: Timer1/3/5 Control Register has an incorrect bit description. The correct description is below:

bit1 RD16: Timer1 16-Bit Read Enable

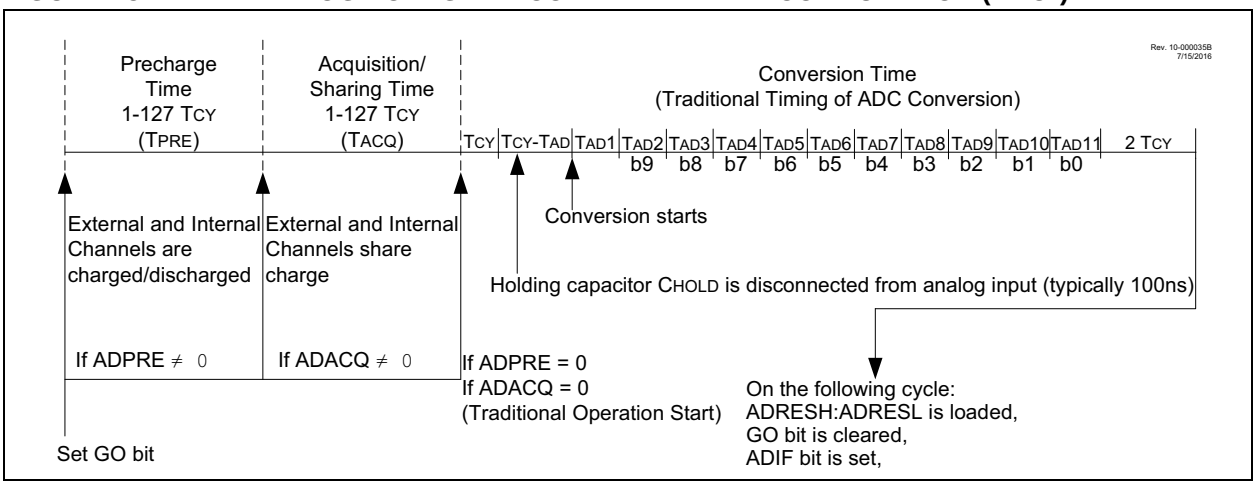
1 = All 16 bits of Timer1 can be read simultaneously (TMR1H is buffered)

0 = 16-bit reads of Timer1 are disabled (TMR1H not buffered)

13. Module: Analog to Digital Converter with Computation (ADC^2)

Figure 23-2: Analog-to-Digital Converter with Computation (ADC^2) is inaccurately described in the data sheet for the ADCC. It should be as follows:

FIGURE 23-2: ANALOG-TO-DIGITAL CONVERTER WITH COMPUTATION (ADC^2)



14. Module: Electrical Specifications

The typical value for specification D207 in Table 37-3: Power-Down Current (IPD) is incorrect. The correct value is 28, as shown below in bold.

TABLE 37-3: TABLE 37-3: POWER-DOWN CURRENT (IPD)

PIC16LF18856/76				Standard Operating Conditions (unless otherwise stated)					
PIC16F18856/76				Standard Operating Conditions (unless otherwise stated) VREGPM = 1					
Param. No.	Symbol	Device Characteristics	Min.	Typ.†	Max. +85°C	Max. +125°C	Units	Conditions	
								VDD	Note
D207	IPD_CMP	Comparator	—	25	38	40	µA	3.0V	
D207	IPD_CMP	Comparator	—	**28**	40	50	µA	3.0V	

15. Module: Electrical Specifications

The typical value for the specification AD22 in Table 37-13: Analog-to-Digital Converter (ADC) Conversion Timing Specifications is incorrect. The correct value is 11+3TCY, as shown below in bold.

TABLE 37-13: ANALOG-TO-DIGITAL CONVERTER (ADC) CONVERSION TIMING SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
AD22	TCNV	Conversion Time	—	**11+3TCY**	—	TAD	Set of GO/$\overline{\text{DONE}}$ bit to Clear of GO/$\overline{\text{DONE}}$ bit

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (8/2016)

Initial release of this document.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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ISBN: 978-1-5224-0901-4

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06/23/16