

FEATURES

Noise figure: 1.6 dB typical
Small signal gain: 19 dB typical
Output P1dB: 16 dBm typical
Single-supply voltage: 3.5 V at 90 mA typical
Output IP3: 27 dBm typical
50 Ω matched input/output
Self biased with optional bias control for quiescent drain control (I_{DQ}) reduction with no radio frequency (RF) applied
Die size: 1.33 mm \times 1.08 mm \times 0.102 mm

APPLICATIONS

Point to point radios
Point to multipoint radios
Military and space
Test instrumentation

GENERAL DESCRIPTION

The **HMC903-Die** is a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), low noise amplifier (LNA), which is self biased with the optional bias control for I_{DQ} reduction. It operates between 6 GHz and 18 GHz. This LNA provides 19 dB of small signal gain, 1.6 dB noise figure, and an output third-order intercept (IP3) of 27 dBm, requiring only 90 mA of supply current from a 3.5 V supply. The output power for a 1 dB compression (P1dB) of 16 dBm enables the LNA to function as a local oscillator (LO) driver for balanced, I/Q, or image rejection mixers. The **HMC903-Die** also features inputs/outputs that are dc blocked and internally matched to 50 Ω for ease of integration into multichip modules (MCMs). All data is taken with the **HMC903-Die** in a 50 Ω test fixture connected via 0.025 mm (1 mil) diameter with bonds of 0.31 mm (12 mil) length.

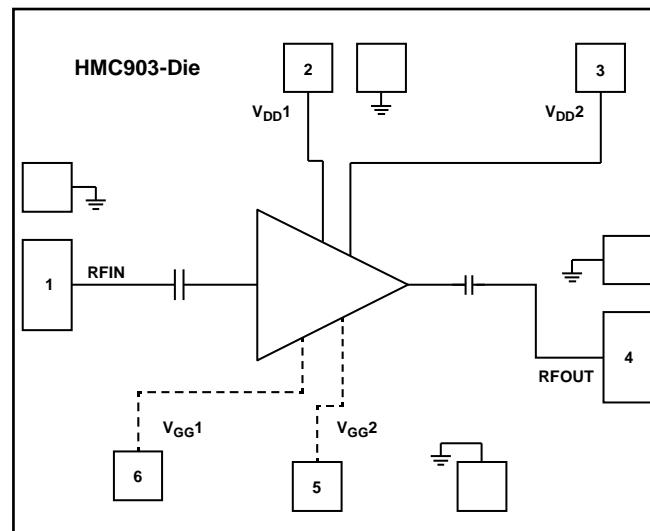
FUNCTIONAL BLOCK DIAGRAM


Figure 1.

Rev. A

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REVISION HISTORY

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

3/2017—Rev. 01.0712 to Rev. A

Updated Format Universal
 Changes to Features Section 1
 Changes to Table 1 3
 Added Electrostatic Discharge (ESD) Sensitivity, Human Body
 Model (HBM) Parameter, Table 2 4
 Changes to Table 3 5

Added Theory of Operation Section and Figure 19; Renumbered
 Sequentially 8
 Added Applications Information Section 9
 Changes to Figure 20 and Figure 21 10
 Added Typical Application Circuits Section and Figure 22 and
 Figure 23 11
 Updated Outline Dimensions 13
 Changes to Ordering Guide 13

SPECIFICATIONS**ELECTRICAL SPECIFICATIONS**

$T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 3.5\text{ V}$, $I_{DQ} = 90\text{ mA}$. $V_{GG1} = V_{GG2} = \text{open}$ for normal, self biased operation.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		6		18	GHz	
GAIN		17	19		dB	
Gain Variation over Temperature			0.013		dB/°C	
RETURN LOSS						
Input			11		dB	
Output			13		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB		16		dBm	
Saturated Output Power	P_{SAT}		18		dBm	
Output Third-Order Intercept	IP3		27		dBm	
NOISE FIGURE	NF		1.6	2.1	dB	
SUPPLY CURRENT	I_{DQ}		90		mA	$V_{DD} = 3.5\text{ V}$, $V_{GG1} = V_{GG2} = \text{open}$

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Drain Bias Voltage	4.5 V
RF Input Power	10 dBm
Gate Bias Voltages	
V _{GG1}	–0.8 V to +0.2 V
V _{GG2}	–0.8 V to +0.2 V
Channel Temperature	175°C
Continuous Power Dissipation, P _{DISS} (T = 85°C, Derate 6.9 mW/°C Above 85°C)	0.62 W
Thermal Resistance (Channel to Die Bottom)	144.8°C/W
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–55°C to +85°C
Electrostatic Discharge (ESD) Sensitivity, Human Body Model (HBM)	Class 0, passed 150 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

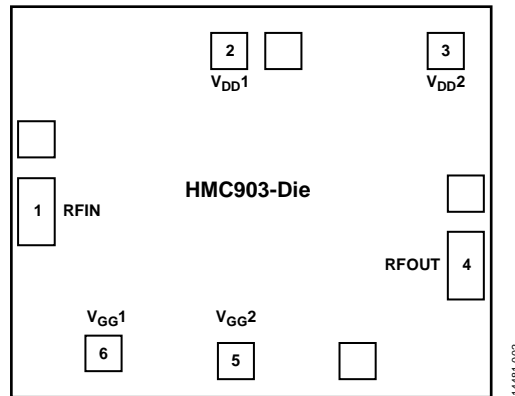


Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RFIN	Radio Frequency Input. This pad is matched to 50 Ω. See Figure 3 for the interface schematic.
2, 3	V _{DD1} , V _{DD2}	Power Supply Voltages. Power supply voltage for the amplifier. See Figure 24 and Figure 25 for required external components. See Figure 4 for the interface schematic.
4	RFOUT	Radio Frequency Output. This pad is matched to 50 Ω. See Figure 5 for the interface schematic.
5, 6	V _{GG1} , V _{GG2}	Gate Control Voltages. Optional gate control for amplifier. When left open, the amplifier is self biased. Applying a negative voltage reduces the current. See Figure 6 for the interface schematic.
Die Bottom	GND	Ground. Die bottom must be connected to RF/dc ground. See Figure 7 for the interface schematic.

INTERFACE SCHEMATICS

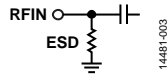


Figure 3. RFIN Interface Schematic

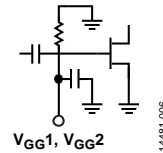


Figure 6. V_{GG1}, V_{GG2} Interface Schematic

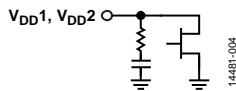


Figure 4. V_{DD1}, V_{DD2} Interface Schematic



Figure 7. GND Interface Schematic

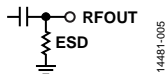


Figure 5. RFOUT Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

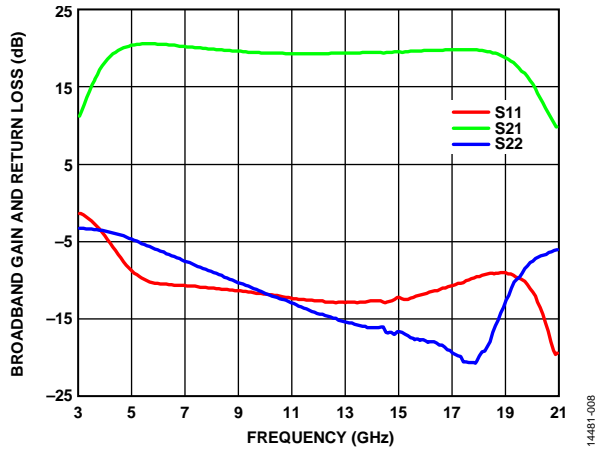


Figure 8. Broadband Gain and Return Loss vs. Frequency

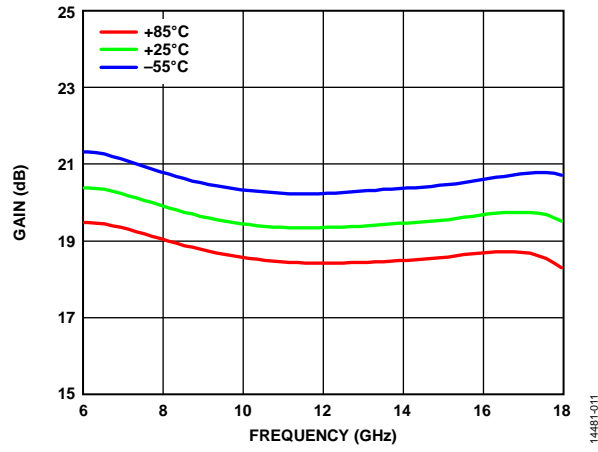


Figure 11. Gain vs. Frequency at Various Temperature

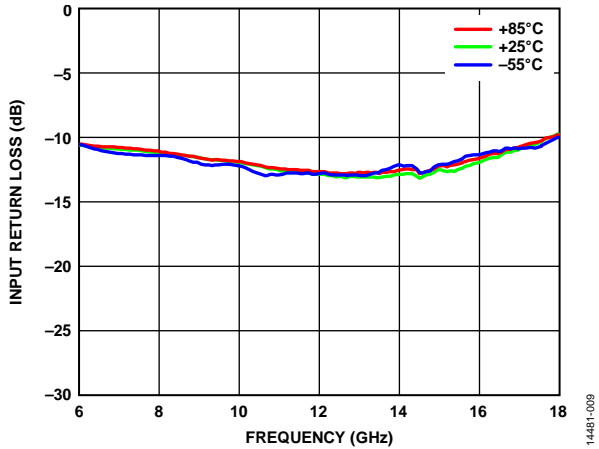


Figure 9. Input Return Loss vs. Frequency at Various Temperatures

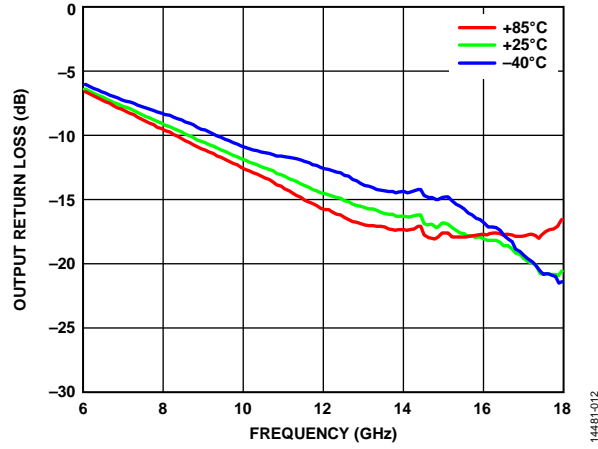


Figure 12. Output Return Loss vs. Frequency at Various Temperatures

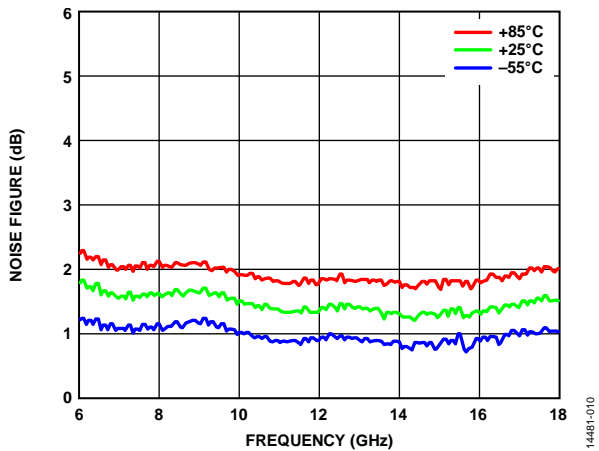


Figure 10. Noise Figure vs. Frequency at Various Temperatures

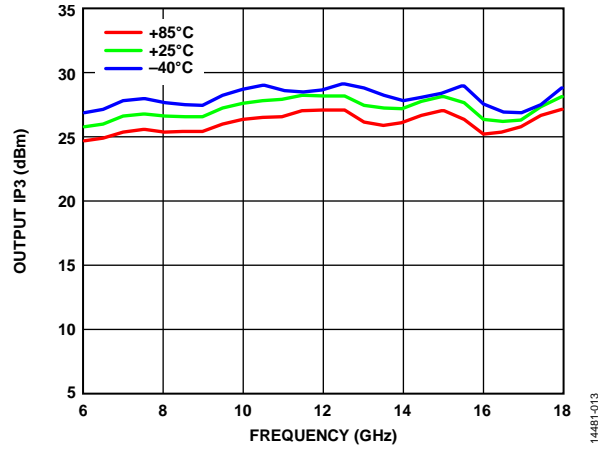


Figure 13. Output IP3 vs. Frequency at Various Temperatures

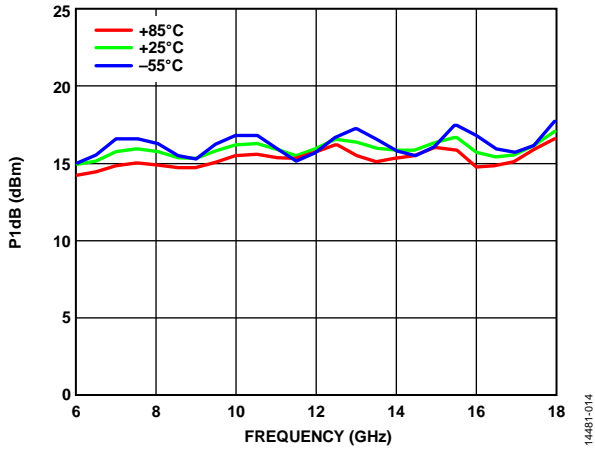


Figure 14. P1dB vs. Frequency at Various Temperatures

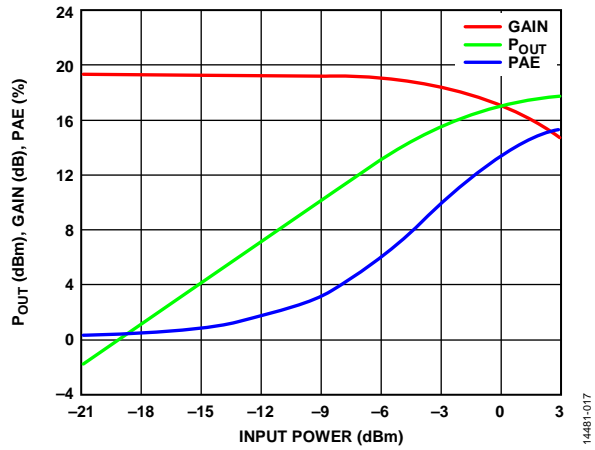


Figure 17. P_{OUT}, Gain, and Power Added Efficiency (PAE) vs. Input Power at 12 GHz

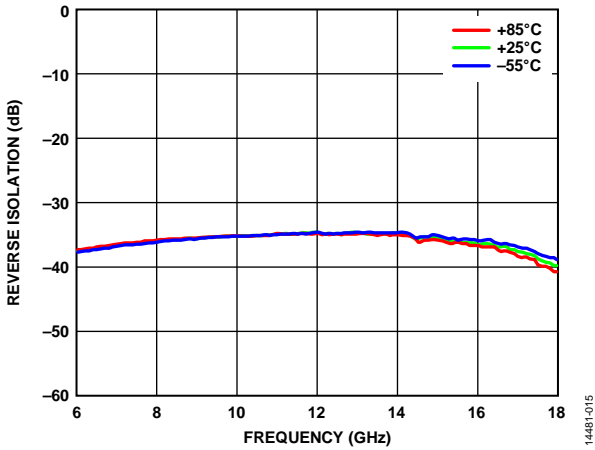


Figure 15. Reverse Isolation vs. Frequency at Various Temperatures

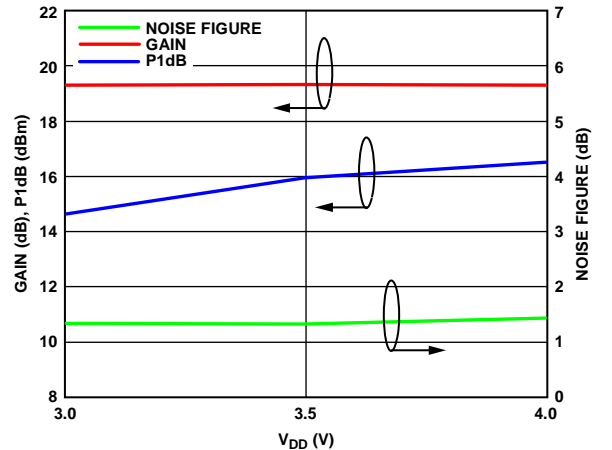


Figure 18. Gain, P1dB, and Noise Figure vs. Supply Voltage (V_{DD}) at 12 GHz

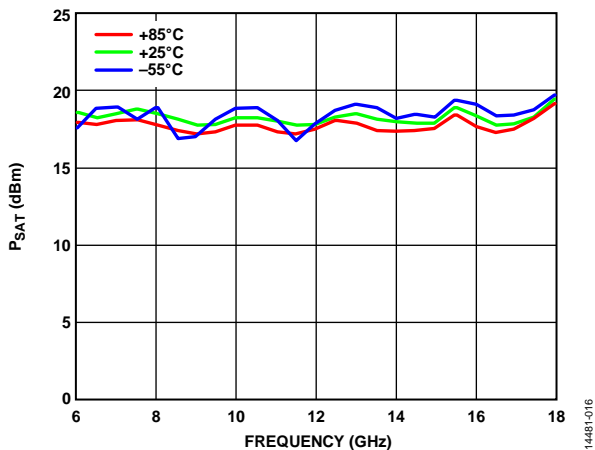


Figure 16. P_{SAT} vs. Frequency at Various Temperatures

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14481-017

14481-015

14481-018

14481-016

THEORY OF OPERATION

The [HMC903-Die](#) is a GaAs, pHEMT, MMIC, low noise amplifier. The [HMC903-Die](#) amplifier uses two gain stages in series. The basic schematic for the amplifier is shown in Figure 19, which forms a low noise amplifier operating from 6 GHz to 18 GHz with excellent noise figure performance.

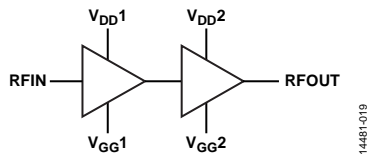


Figure 19. Basic Schematic for the [HMC903-Die](#)

The [HMC903-Die](#) has single-ended input and output ports with impedances nominally equal to 50 Ω over the 6 GHz to 18 GHz frequency range.

Consequently, the device can be directly inserted into a 50 Ω system with no required impedance matching circuitry; therefore, multiple [HMC903-Die](#) amplifiers can be cascaded back to back without the need for external matching circuitry.

The input and output impedances are sufficiently stable vs. variations in temperature and supply voltage that no impedance matching compensation is required.

It is critical to supply very low inductance ground connections to the exposed pad to ensure stable operation. To achieve optimal performance from the [HMC903-Die](#) and to prevent damage to the device, do not exceed the absolute maximum ratings.

APPLICATIONS INFORMATION

Figure 25 shows the basic connections for operating the [HMC903-Die](#) in self biased operation. Both the RFIN and the RFOUT ports have on-chip dc block capacitors, eliminating the need for external ac coupling capacitors.

The [HMC903-Die](#) has V_{GG1} and V_{GG2} optional gate bias pads. When these pads are left open, the amplifier runs in self biased operation with typical $I_{DQ} = 90$ mA when $V_{DD} = 3.5$ V. When using the optional V_{GG1} and V_{GG2} gate bias pads, use the recommended bias sequencing to prevent damage to the amplifier.

The recommended bias sequence during power-up is as follows:

1. Connect to GND.
2. Set V_{GG1} and V_{GG2} to -2 V.
3. Set V_{DD1} and V_{DD2} to $+3.5$ V.
4. Increase V_{GG1} and V_{GG2} to achieve a typical $I_{DQ} = 90$ mA.
5. Apply the RF signal.

The recommended bias sequence during power-down is as follows:

1. Turn off the RF signal.
2. Decrease V_{GG1} and V_{GG2} to -2 V to achieve a typical $I_{DQ} = 0$ mA.
3. Decrease V_{DD1} and V_{DD2} to 0 V.
4. Increase V_{GG1} and V_{GG2} to 0 V.

The bias conditions previously listed (V_{DD1} and $V_{DD2} = 3.5$ V and $I_{DQ} = 90$ mA) are the recommended operating points to achieve optimum performance. The data used in this data sheet is taken with the recommended bias conditions listed in the Electrical Specifications section. If the [HMC903-Die](#) is used with different bias conditions than what is recommended, a different performance than what is shown in the Typical Performance Characteristics section can result. Decreasing the V_{DD} level has a negligible effect on gain and NF performance, but reduces P1dB. This behavior is shown in Figure 18. For applications where the P1dB requirement is not stringent, the [HMC903-Die](#) can be down biased to reduce power consumption.

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

The **HMC903-Die** is attached directly to the ground plane eutectically or with conductive epoxy (see the General Handling section, the Mounting section, and the Wire Bonding section).

The 50 Ω microstrip transmission lines on 0.127 mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the **HMC903-Die** (see Figure 20).

When using 0.254 mm (10 mil) thick alumina thin film substrates, the die is raised 0.150 mm (6 mil) so the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102 mm (4 mil) thick die to a 0.150 mm (6 mil) thick molybdenum heat spreader (moly tab), which then attaches to the ground plane (see Figure 21).

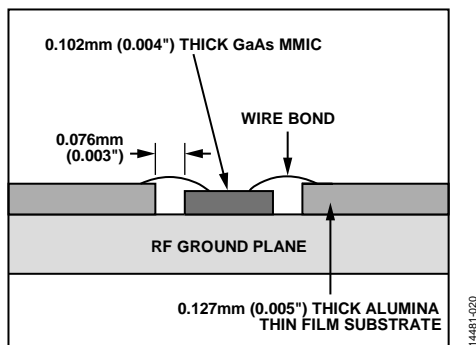


Figure 20. Routing RF Signal

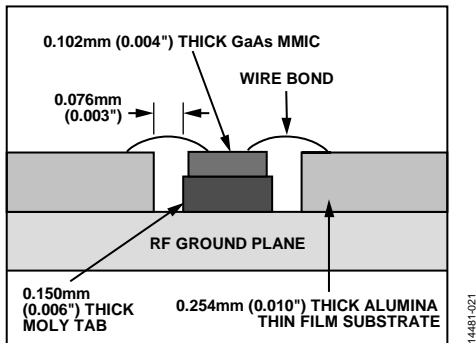


Figure 21. Routing RF Signal with Moly Tab

Microstrip substrates are placed as close to the die as possible to minimize bond wire length. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

HANDLING PRECAUTIONS

Follow the precautions detailed in the following sections to avoid permanent damage to the device.

Storage

All bare die are placed in either waffle or gel-based ESD protective containers and then sealed in an ESD protective bag for shipment. After opening the sealed ESD protective bag, store all die in a dry nitrogen environment.

Cleanliness

Handle the chips in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.

Static Sensitivity

Follow ESD precautions to protect against ESD strikes.

Transients

Suppress instrument and bias supply transients while bias is applied. Use the shielded signal and bias cables to minimize inductive pickup.

General Handling

Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the **HMC903-Die** has fragile air bridges and must not be touched with the vacuum collet, tweezers, or fingers.

Mounting

The **HMC903-Die** is back metallized and can be die mounted with gold tin (AuSn) eutectic preforms or with electrically conductive epoxy. The mounting surface must be clean and flat.

Eutectic Die Attach

An 80% gold/20% tin preform is recommended with a work surface temperature of 255°C and a tool temperature of 265°C. When hot 90% nitrogen/10% hydrogen gas is applied, the tool tip temperature is 290°C. Do not expose the chip to a temperature greater than 320°C for more than 20 sec. No more than 3 sec of scrubbing is required for attachment.

Epoxy Die Attach

Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the **HMC903-Die** after it is placed into position. Cure epoxy per the schedule of the manufacturer.

Wire Bonding

RF bonds made with two 1 mil wires are recommended. These bonds are thermosonically bonded with a force of 40 g to 60 g. DC bonds of 0.001 in (0.025 mm) diameter, thermosonically bonded, are recommended. Create ball bonds with a force of 40 g to 50 g and wedge bonds at 18 g to 22 g. Create bonds with a nominal stage temperature of 150°C. A minimum amount of ultrasonic energy is applied to achieve reliable bonds. All bonds are as short as possible, less than 12 mil (0.31 mm).

TYPICAL APPLICATION CIRCUITS

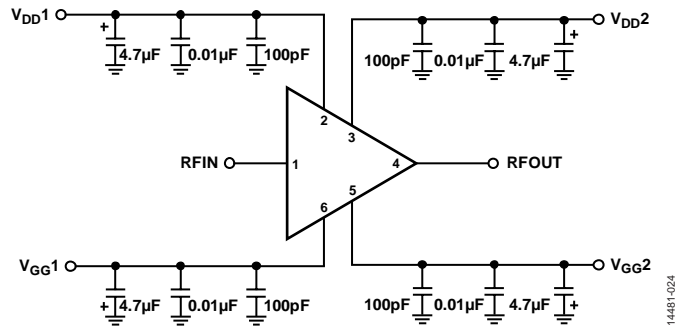


Figure 22. Typical Application Circuit with Gate Control Option

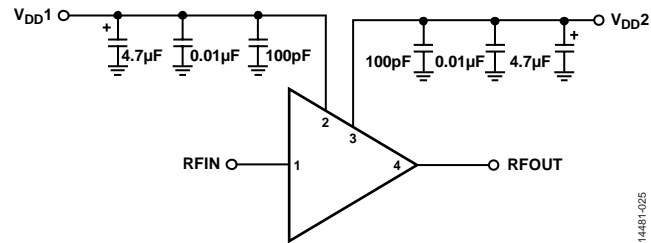


Figure 23. Typical Application Circuit with Self Biased Option

ASSEMBLY DIAGRAMS

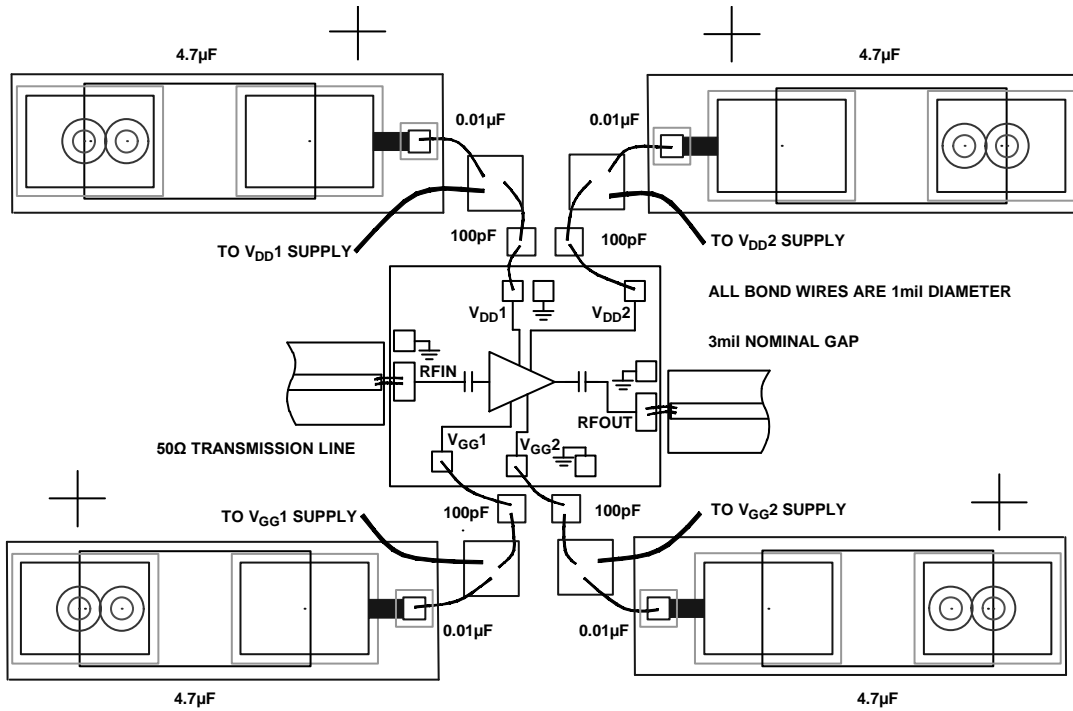


Figure 24. Assembly Diagram with Gate Control Option

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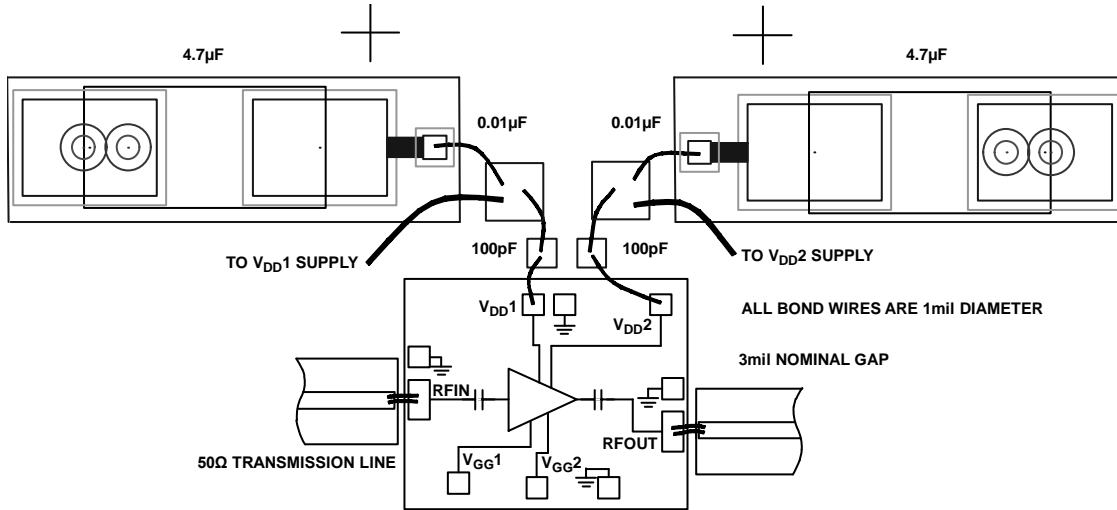
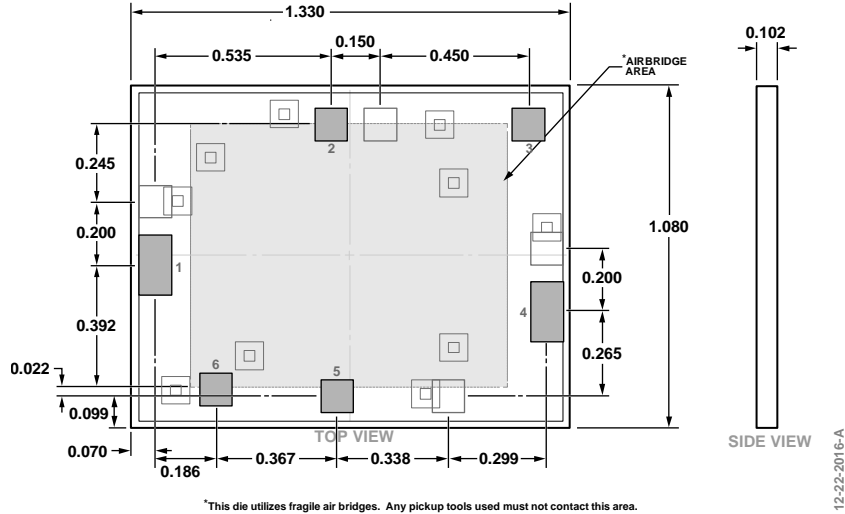


Figure 25. Assembly Diagram with Self Biased Option

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OUTLINE DIMENSIONS



*This die utilizes fragile air bridges. Any pickup tools used must not contact this area.

Figure 26. 6-Pad Bare Die [CHIP]
(C-6-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
HMC903	-55°C to +85°C	6-Pad Bare Die [CHIP]	C-6-10
HMC903-SX	-55°C to +85°C	6-Pad Bare Die [CHIP]	C-6-10

¹ The HMC903-SX is a sample order of two devices.