

PIC10F200/202/204/206 Rev. A Silicon/Data Sheet Errata

The PIC10F200/202/204/206 parts you have received conform functionally to the Device Data Sheet (DS41239D), except for the anomalies described below.

Microchip intends to address all issues listed here in future revisions of the **PIC10F200/202/204/206 silicon**. Where noted, issues apply to listed revision only.

1. Module: Port Pins

On the PIC10F204/206 silicon, Rev. A0, the data direction control latch for port pin GP2 is overridden when the comparator output is used internally. This applies when the following bit configuration is used:

T0CS = 1	OPTION<5>
$\overline{\text{CMPT0CS}} = 0$	CMCON0<4>
$\overline{\text{COUTEN}} = 1$	CMCON0<6>

Work around

This issue is fixed in Rev. A1 and later.

2. Module: Comparator

On the PIC10F204/206 silicon, Rev. A0, the internal voltage reference is disabled when a SLEEP instruction is executed.

Work around

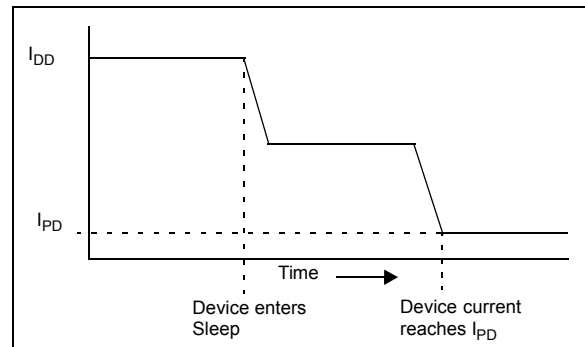
Do not issue a SLEEP instruction when using the internal 0.6V voltage reference. This issue is fixed in Rev. A1 and later.

3. Module: I_{PD} , Power-Down Base current

On the PIC10F200/202/204/206 silicon, revisions earlier than A3, the power-down base current may remain higher than the specification for a short time when entering Sleep.

The following graph illustrates the device current upon entering Sleep:

FIGURE 1:



The length of time between the device entering Sleep mode and the device current reaching I_{PD} increases as both temperature and voltage decrease.

Work around

This issue is fixed in Rev. A3 and later.

PIC10F200/202/204/206

4. Module: MPLAB® IDE, Revision 6.61 and Earlier

The MPLAB IDE 6.61 does not look for or set the Configuration Word in the hex file at the conventional logical location of 0xFFFF.

Work around

The CONFIG data must be assigned in two locations within the assembly code to ensure proper Configuration Word placement in the hex file. This is only required for MPLAB IDE version 6.61 and earlier.

EXAMPLE 1: CODE

```
Fixed Code
org      0xYYYY
data    _CP_OFF & _WDT_ON & etc.
__CONFIG _CP_OFF & _WDT_ON & etc.
Re-locatable Code
.config code 0xYYYY
data    data _CP_OFF & _WDT_ON & etc.
__CONFIG data _CP_OFF & _WDT_ON & etc.
```

TABLE 1: CONFIGURATION WORD ADDRESS

Device	YYYY
PIC10F200	01FF
PIC10F202	03FF
PIC10F204	01FF
PIC10F206	03FF

Note 1: YYYY is the address of the Configuration Word for the part.

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS41239D), the following clarifications and corrections should be noted.

1. Module: Special Features of the CPU

Register 9-1: Configuration Word, bit 11-5 and bit 1-0 should be (Read as '1') as shown in bold.

REGISTER 9-1: CONFIGURATION WORD FOR PIC10F200/202/204/206

—	—	—	—	—	—	—	MCLRE	$\overline{\text{CP}}$	WDTE	—	—
bit 11											bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 11-5 **Unimplemented:** Read as '1'

bit 4 **MCLRE:** GP3/ $\overline{\text{MCLR}}$ Pin Function Select bit

1 = GP3/ $\overline{\text{MCLR}}$ pin function is $\overline{\text{MCLR}}$

0 = GP3/ $\overline{\text{MCLR}}$ pin function is digital I/O, $\overline{\text{MCLR}}$ internally tied to VDD

bit 3 **$\overline{\text{CP}}$:** Code Protection bit

1 = Code protection off

0 = Code protection on

bit 2 **WDTE:** Watchdog Timer Enable bit

1 = WDT enabled

0 = WDT disabled

bit 1-0 **Reserved:** Read as '1'

APPENDIX A: REVISION HISTORY

Rev A Document (6/2004)

First revision of this document.

Rev B Document (6/2004)

Added Module 2, VREF is disabled in Sleep.

Rev C Document (9/2004)

Added Module 3, MPLAB IDE and the `_CONFIG` assembly directive.

Rev D Document (6/2006)

Added the following Modules to the “Clarifications/Corrections to the Data Sheet” section:

- Module 1, “Internal Oscillator”
- Module 2, “Voltage Reference”
- Module 3, “8-Lead 2x3 DFN (MC) Packaging”
- Module 4, “8-Lead 2x3 DFN (MC) Package – Top Marking”
- Module 5, “6-Lead SOT-23 (OT) Package – Top Marking”

Rev E Document (3/2007)

Revised Module 1 and Module 2 work arounds.

Clarification/Corrections to the Data Sheet:

Revised Module 3: Replaced DFN Package Drawing;

Added Module 6, “Timer0 Clock”;

Added Module 7, Special Features of the CPU, Register 9-1.

Rev F Document (5/2007)

Revised Module 3, Table 1, Note 1.

Clarification/Corrections to the Data Sheet:

Data Sheet was updated. The following was removed:

- Module 1, “Internal Oscillator”
- Module 2, “Voltage Reference”
- Module 3, “8-Lead 2x3 DFN (MC) Packaging”
- Module 4, “8-Lead 2x3 DFN (MC) Package – Top Marking”
- Module 5, “6-Lead SOT-23 (OT) Package – Top Marking”
- Module 6, “Timer0 Clock”;

Module 7, Special Features of the CPU, Register 9-1 is renumbered to Module 1.

Rev G Document (6/2007)

Moved Module 3 to Module 4.

Added Module 3: I_{PD} , Power-Down Base current

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