

The TDK4 is a high voltage, high current disc pack SCR employing a high di/dt gate structure. This gate design allows the SCR to be reliably operated at high di/dt and dv/dt conditions in various phase control applications.

#### FEATURES:

- Low On-State Voltage
- High di/dt Capability
- High dv/dt Capability
- Hermetic Ceramic Package
- Excellent Surge and I<sup>2</sup>t Ratings

#### APPLICATIONS:

- DC Power Supplies
- Motor Controls

#### ORDERING INFORMATION

Select the complete 12 digit Part Number using the table below.  
 EXAMPLE: TDK4363402DH is a 3600V-3400A SCR with 300ma IGT and 12 inch gate and cathode potential leads.

PART	Voltage Rating $V_{DRM}-V_{RRM}$	Voltage Code	Current Rating $I_{TAVG}$	Current Code	Turn-Off $T_q$	Gate $I_{GT}$	Leads
<b>TDK4</b>	3600	<b>36</b>	3400	<b>34</b>	<b>0</b>	<b>2</b>	
	3400	<b>34</b>					
	3200	<b>32</b>			400us	300ma	12"
	3000	<b>30</b>			(typ.)	(max)	

**Absolute Maximum Ratings<sup>†</sup>**

Characteristic	Symbol	Rating	Units
Repetitive Peak Voltage	$V_{DRM} - V_{RRM}$	3000 - 3600	Volts
Average On-State Current, $T_C=70^\circ\text{C}$	$I_{T(Avg.)}$	3430	A
RMS On-State Current, $T_C=70^\circ\text{C}$	$I_{T(RMS)}$	5388	A
Average On-State Current, $T_C=55^\circ\text{C}$	$I_{T(Avg.)}$	3745	A
RMS On-State Current, $T_C=55^\circ\text{C}$	$I_{T(RMS)}$	5883	A
Peak One Cycle Surge Current, 60Hz, $V_R=0V$	$I_{TSM}$	70,000	A
Peak One Cycle Surge Current, 50Hz, $V_R=0V$	$I_{TSM}$	65,600	A
Fuse Coordination $I^2t$ , 60Hz	$I^2t$	2.04E+07	A <sup>2</sup> s
Fuse Coordination $I^2t$ , 50Hz	$I^2t$	2.15E+07	A <sup>2</sup> s
Critical Rate-of-Rise of On-State Current	$di/dt$	100	A/us
Repetitive from .67•VDRM			
Critical Rate-of-Rise of On-State Current	$di/dt$	300	A/us
Non-Repetitive from .67•VDRM			
Peak Gate Power, 100us	$P_{GM}$	16	Watts
Average Gate Power	$P_{G(avg)}$	5	Watts
Operating Temperature	$T_j$	-40 to+125	°C
Storage Temperature	$T_{Stg.}$	-40 to+150	°C
Approximate Weight		6.1	lb
		2.77	Kg
Mounting Force		18,000 - 25,000	lbs
		80 - 110	KNewtons

<sup>†</sup> Ratings apply for operation at rated load force.

Information presented is based upon manufacturers testing and projected capabilities. This information is subject to change without notice. The manufacturer makes no claim as to suitability for use, reliability, capability or future availability of this product.

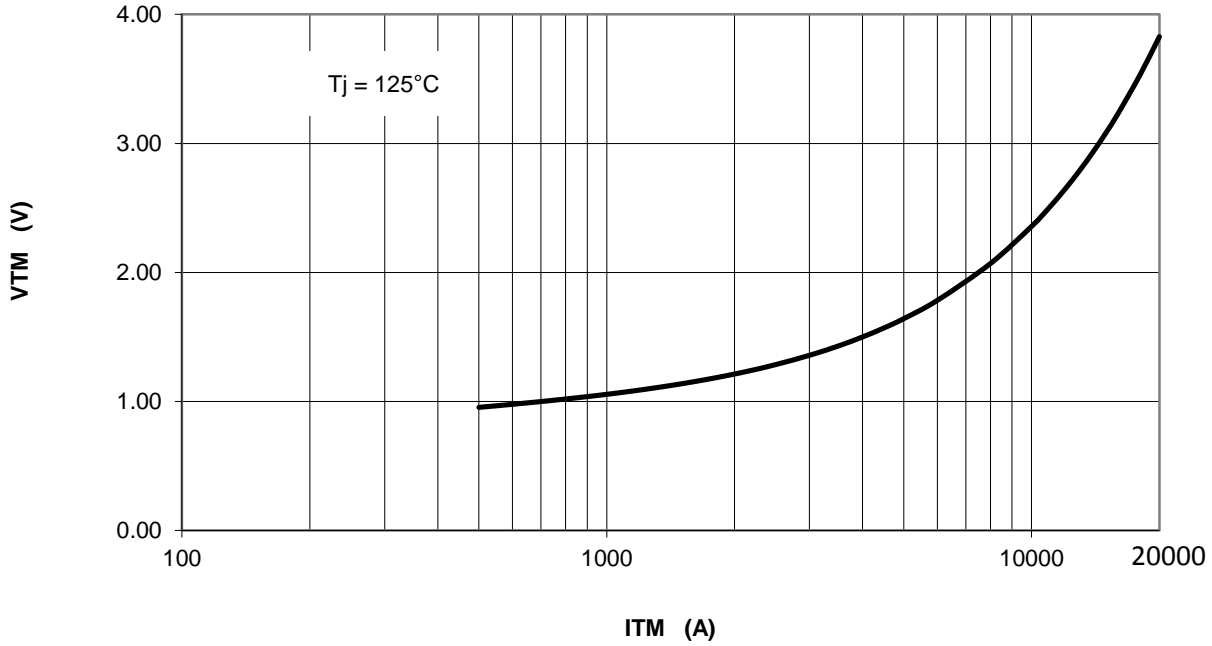
**Electrical Characteristics, T<sub>j</sub>=25°C unless otherwise specified**

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Repetitive Peak Forward						
Leakage Current	I <sub>DRM</sub>	T <sub>j</sub> =125°C, V <sub>DRM</sub> =Rated			300	ma
Repetitive Peak Reverse						
Leakage Current	I <sub>RDM</sub>	T <sub>j</sub> =125°C, V <sub>RDM</sub> =Rated			300	ma
Peak On-State Voltage	V <sub>TM</sub>	T <sub>j</sub> =125°C, I <sub>TM</sub> =4000A			1.50	V
V <sub>TM</sub> Model, Low Level	V <sub>0</sub>	T <sub>j</sub> =125°C			0.914	V
V <sub>TM</sub> = V <sub>0</sub> + r•I <sub>TM</sub>	r	15% I <sub>TM</sub> - π•I <sub>TM</sub>			0.145	mΩ
V <sub>TM</sub> Model, High Level	V <sub>0</sub>	T <sub>j</sub> =125°C			0.802	V
V <sub>TM</sub> = V <sub>0</sub> + r•I <sub>TM</sub>	r	π•I <sub>TM</sub> - I <sub>TSM</sub>			0.152	mΩ
V <sub>TM</sub> Model, 4-Term	A	T <sub>j</sub> =125°C			0.285	
V <sub>TM</sub> = A + B•Ln(I <sub>TM</sub> ) +	B	15%I <sub>TM</sub> - I <sub>TSM</sub>			0.120	
C•(I <sub>TM</sub> ) + D•(I <sub>TM</sub> ) <sup>1/2</sup>	C				1.69E-04	
	D				-0.00720	
Turn-On Delay Time	t <sub>d</sub>	V <sub>D</sub> = 0.5•V <sub>DRM</sub> Gate Drive: 40V - 20Ω			3	us
Turn-Off Time (typ)	t <sub>q</sub>	T <sub>j</sub> =125°C dv/dt = 20V/us to 80% V <sub>DRM</sub>		600		us
dv/dt <sub>(crit)</sub>	dv/dt	T <sub>j</sub> =125°C Exp. Waveform V <sub>D</sub> =67% Rated	1000			V/us
Gate Trigger Current	I <sub>GT</sub>	T <sub>j</sub> =25°C V <sub>D</sub> = 12V	40	100	300	ma
Gate Trigger Voltage	V <sub>GT</sub>		0.8	2.0	4.0	V
Peak Reverse Gate Voltage	V <sub>GRM</sub>				5	V

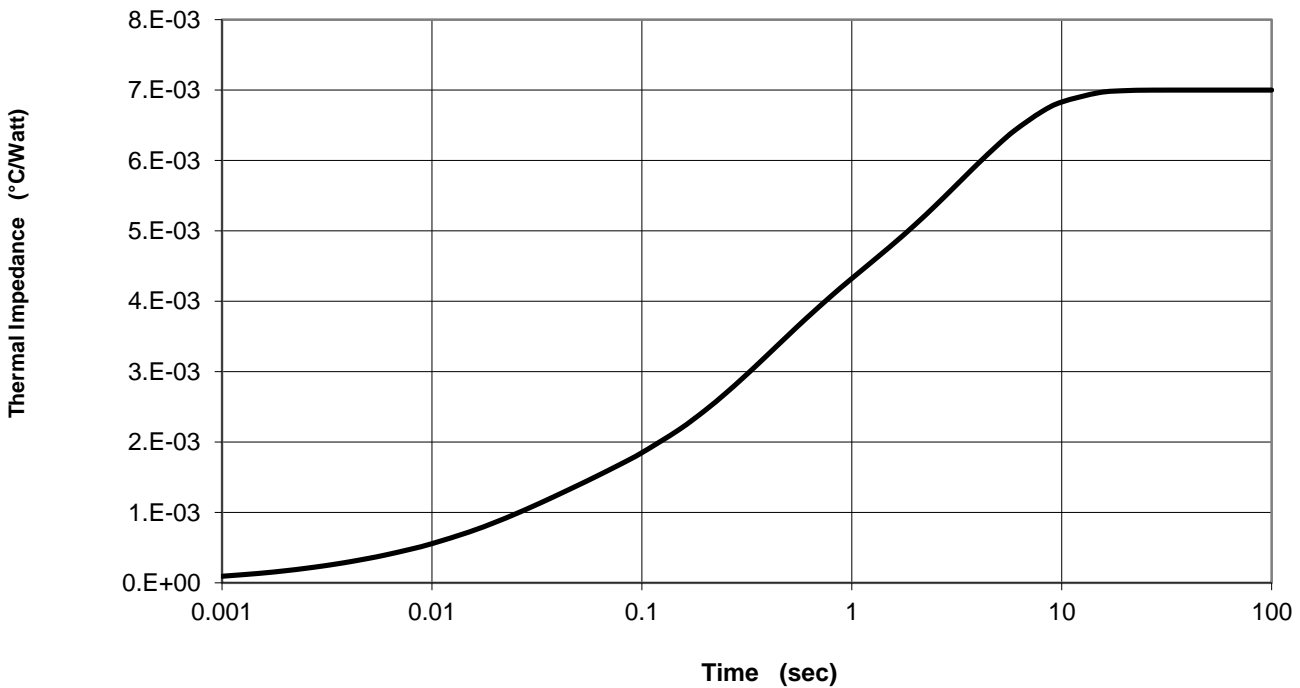
**Thermal Characteristics**

Characteristic	Symbol	Test Conditions	Rating			Units
			min	typ	max	
Thermal Resistance						
Junction to Case	Rθ <sub>jc</sub>	Double side cooled		0.0055	0.007	°C/Watt
Case to Sink	Rθ <sub>cs</sub>	Double side cooled		0.0015	0.002	°C/Watt
Thermal Impedance Model	Zθ <sub>jc</sub>	Double side cooled				
$Z_{\theta_{jc}}(t) = \Sigma(A(N) \cdot (1 - \exp(-t/\text{Tau}(N))))$						
where: N = 1                      2                      3                      4						
A(N) = 1.43E-04    9.38E-04    2.42E-03    3.50E-03						
Tau(N) = 2.62E-03    2.31E-02    3.05E-01    3.30E+00						

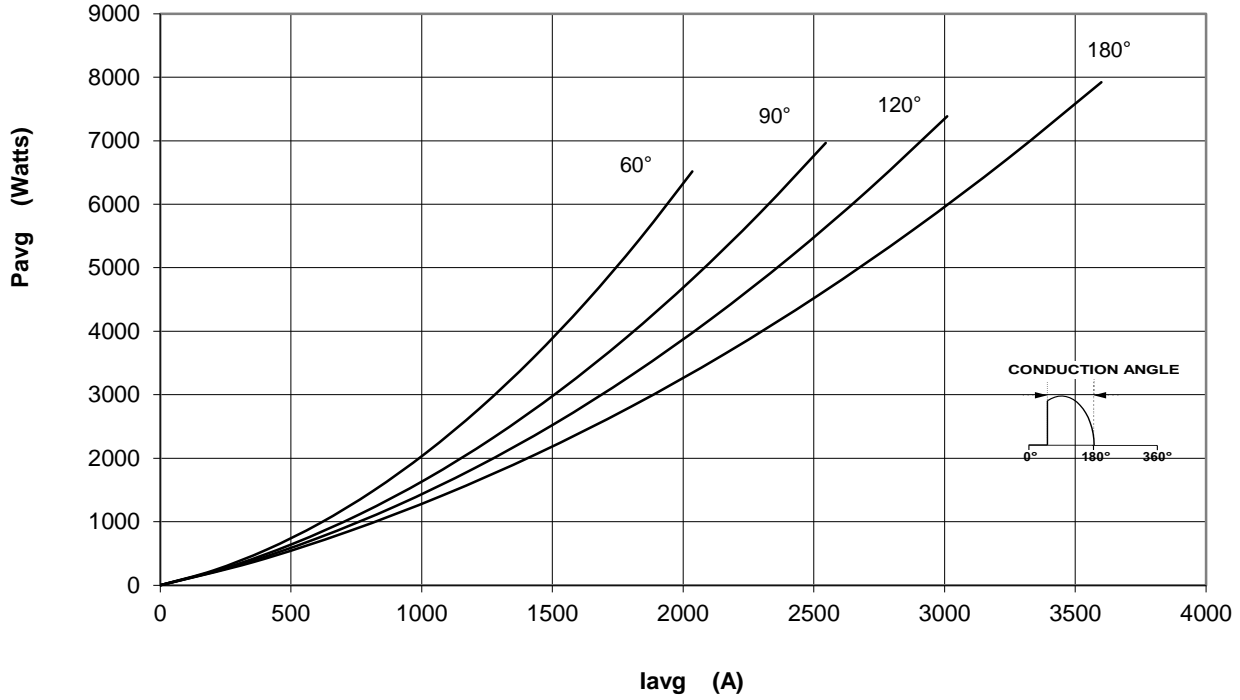
### Maximum On-State Voltage Drop



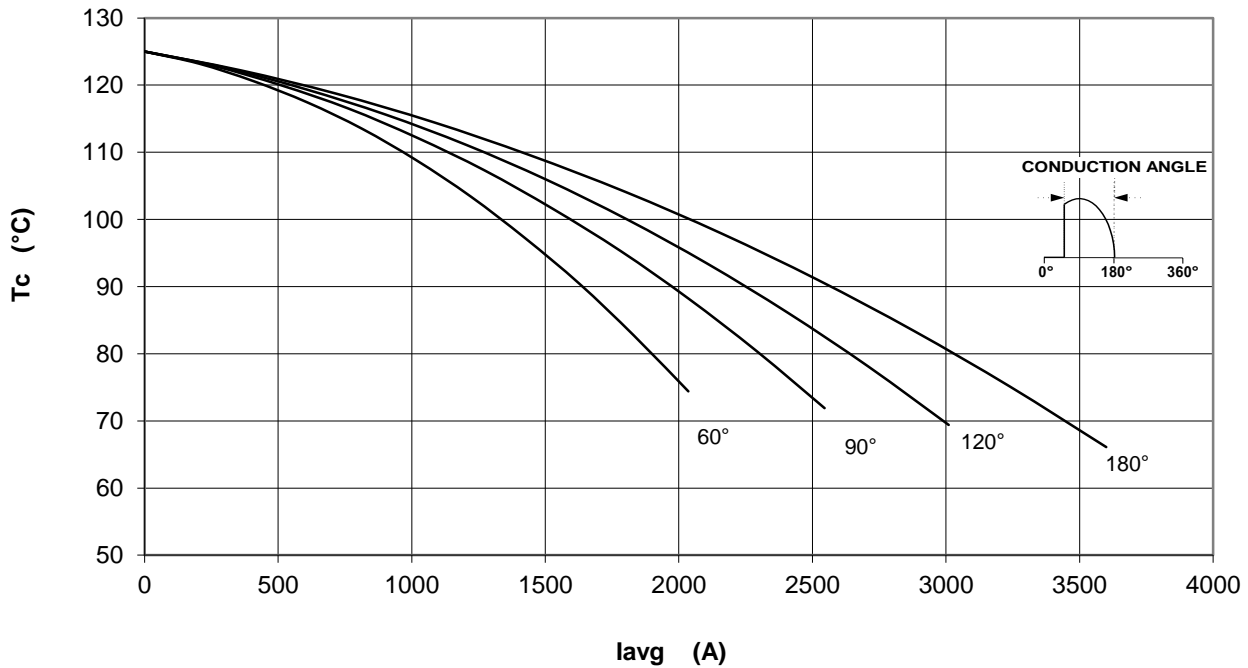
### MAXIMUM TRANSIENT THERMAL IMPEDANCE



**Maximum On-State Power Dissipation**  
 Sinusoidal Waveform

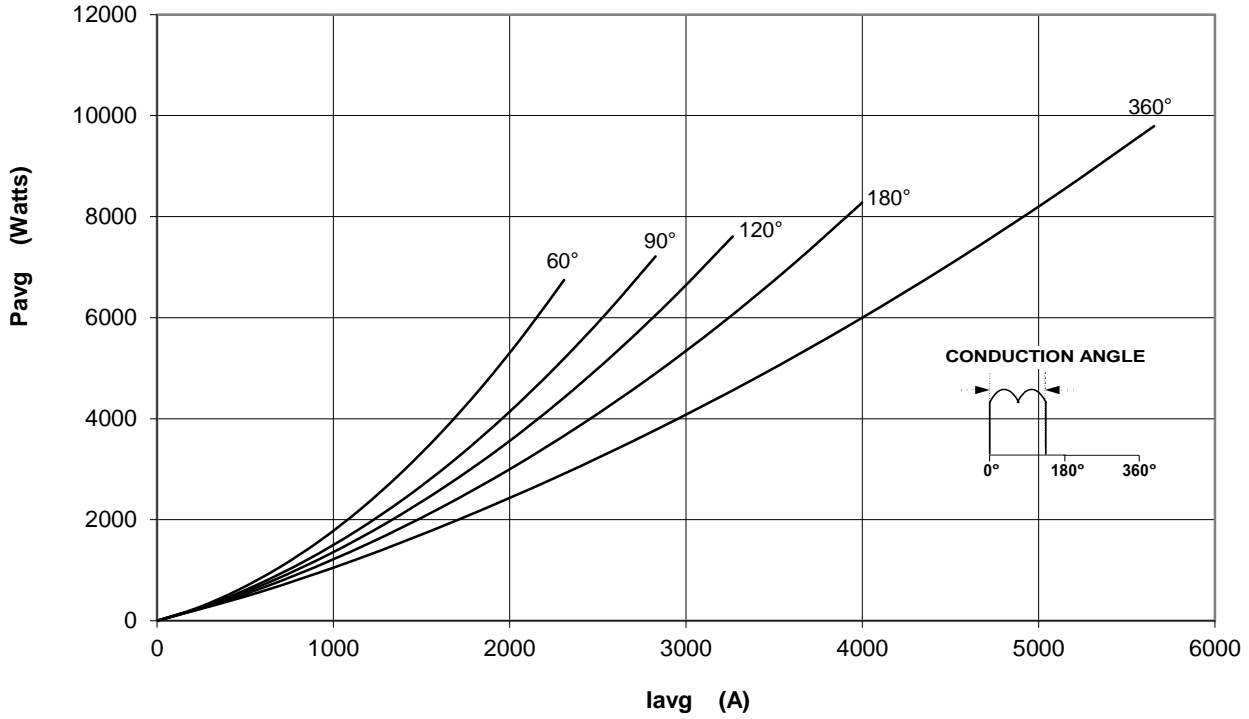


**Maximum Allowable Case Temperature**  
 Sinusoidal Waveform



### Maximum On-State Power Dissipation

Square Waveform



### Maximum Allowable Case Temperature

Square Waveform

