

Introduction

The L9301 is a SPI (Serial Peripheral Interface) that controls octal channel with 4 high/low and 4 low-side driver in order to drive inductive loads, it is powered with maximum power voltage 18Vdc, it is able to work in the temperature range (-40°C to 150°C). 8 loads can be driven in SPI or PWM mode, the other 4 can be driven only by SPI mode.

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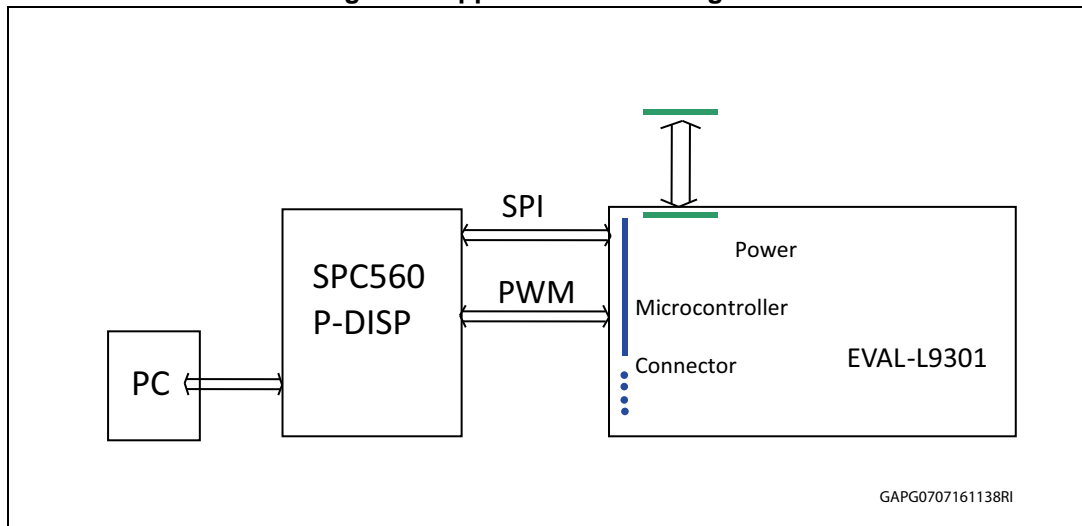
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1 Hardware description

The EVAL-L9301 board provides maximum flexibility, access to all pins to simplify the evaluation and debug phase.

1.1 Block diagram

Figure 1. Application block diagram



1.1.1 Microcontroller interface

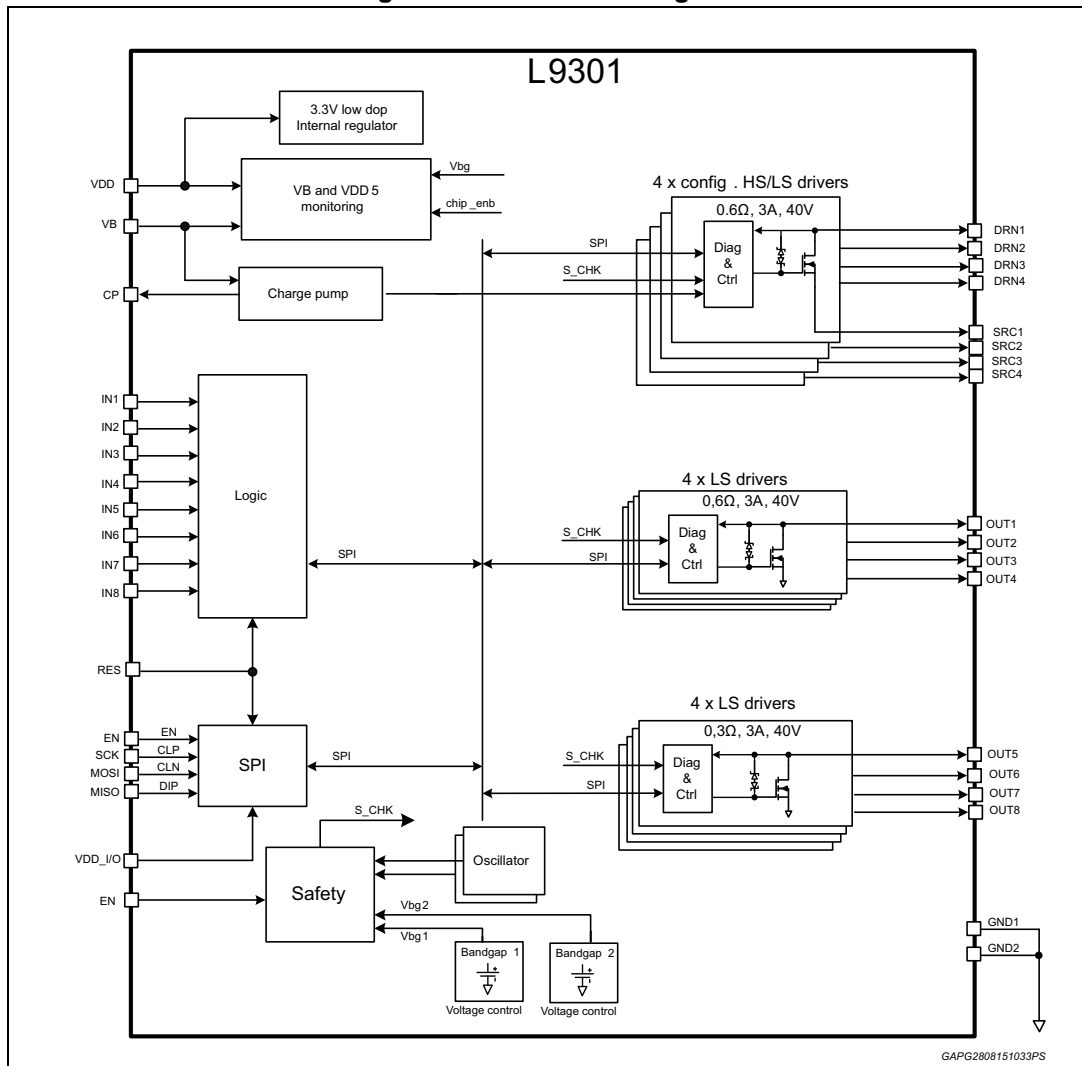
- Standard ADG connector 4x37.
- 8 PWM output [0, 5]V, duty [20, 80]%, frequency [2, 10]khz
- Configuration and Diagnostic of L9301 via SPI
- Possibility to directly connect the board to SPC560P-DISP.

Main features device are shown in the following, for data sheet device refer to L9301 data sheet (see [Section A.1.1: Document references](#)):

- Case PowerSSO36
- 8 integrated power MOS configurable as: 8 low-side ON-OFF with $R_{ON(max)}=0.3 \Omega$
- 4 high/low-side PWM with $R_{ON(max)}=0.6 \Omega$ and 4 low-side with $R_{ON(max)}=0.3 \Omega$
- Operating battery supply voltage 5 V to 18 V
- Operating Vdd supply voltage 4.75 V to 5.25 V
- Logic input TTL/CMOS compatible
- Voltage clamping 37 V typ.
- SPI interface for outputs control and diagnosis data communication
- 8 PWM inputs for 8 outputs
- Over temperature protection
- Open load, short to ground and short to battery diagnosis
- Overcurrent diagnosis

1.2 L9301 Block diagram

Figure 2. L9301 Block diagram



In [Figure 2](#) you can see the following areas.

On the left:

- SPI: 4 pin: Clock (Clk), Chip Select, MOSI e MISO;
- Logic: IN1-8 for 8 PWM;
- on the right:
- OUT1-8: the connections to loads;
- DRN1-4 and SRC1-4: 4 output MOS source and drain, used in several mode like recirculation diode.

L9301 device, as said, has 12 power MOS outputs: 4 outputs are configurable high/low-side drivers with $R_{onmax} = 0,6 \Omega$ (DRN1-4 and SRC1-4), 4 low-side drivers with $R_{onmax} = 0,6 \Omega$ (OUT1-4) and 4 low-side drivers with $R_{onmax} = 0,3 \Omega$ (OUT5-8). The DRN/SRC with OUT1-4 can be connected in parallel out of device in order to have 4 low-side drivers

with $R_{onmax} = 0,3 \Omega$. In this connection we are able to work with 8 low-side channels with resistance of $0,3 \Omega$.

It's possible to connect OUT1-8, driven in PWM, to drive an inductive load connected to VB (battery voltage) or to GND (ground), without using free-wheeling diode (paragraph 1.2), in this case $R_{onmax} = 0,6 \Omega$.

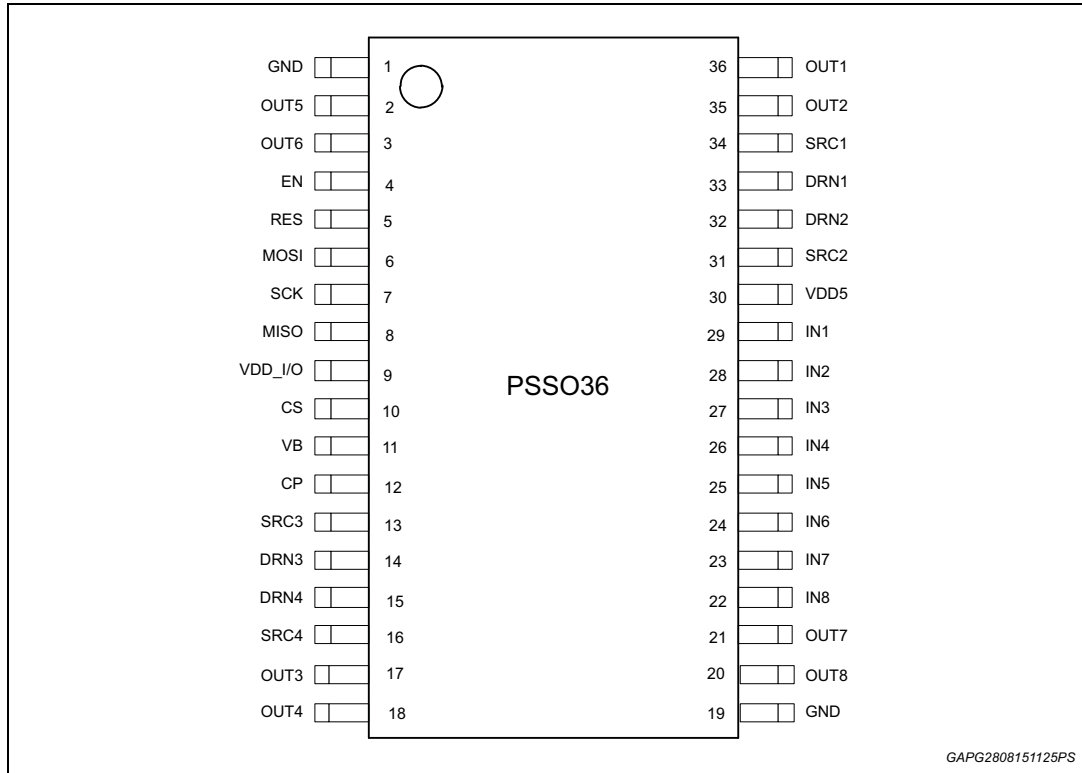
The device is configurable through SPI, choosing one of the 4 possible configurations, signal slew rate, overcurrent threshold, turn on/off channels and to have diagnosis.

1.3 Recirculation diode

In the off state driver the inductive load has to discharge the stored energy in on state using an external recirculation diode, otherwise, it's possible to assign this function to the internal MOS, used like recirculation diode.

2 L9301 pin-out and pin description

Figure 3. L9301 pin connection diagram



GAPG2808151125PS

Table 1. L9301 pin descriptions

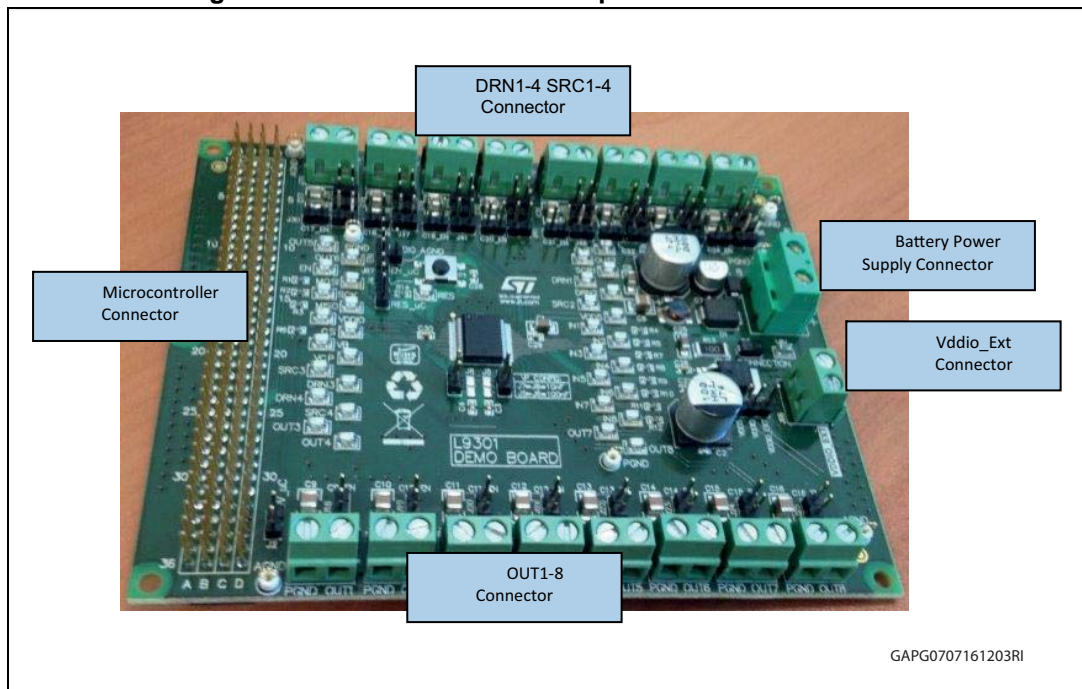
Pin	Symbol	Function
1	GND	Power ground of OUT 1, 2, 5, 6
2	OUT5	Output 5
3	OUT6	Output 6
4	EN	Enable
5	RES	Reset Input (active low)
6	MOSI	SPI data in
7	SCK	SPI serial clock input
8	MISO	SPI data out
9	VDD_I/O	Microcontroller logic interface voltage
10	CS	SPI chip select (active low)
11	VB	Battery supply voltage
12	CP	Charge pump
13	SRC3	Source pin for configurable driver #3
14	DRN3	Drain pin of configurable driver #3
15	DRN4	Drain pin of configurable driver #4
16	SRC4	Source pin of configurable driver #4
17	OUT3	Output 3
18	OUT4	Output 4

Table 1. L9301 pin descriptions (continued)

Pin	Symbol	Function
19	GDN	Power ground of 3, 4, 7, 8
20	OUT8	Output 8
21	OUT7	Output 7
22	IN8	Discrete input used to PWM output driver #8
23	IN7	Discrete input used to PWM output driver #7
24	IN6	Discrete input used to PWM output driver #6
25	IN5	Discrete input used to PWM output driver #5
26	IN4	Discrete input used to PWM output driver #4
27	IN3	Discrete input used to PWM output driver #3
28	IN2	Discrete input used to PWM output driver #2
29	IN1	Discrete input used to PWM output driver #1
30	VDD5	5 Volt supply input
31	SRC2	Source pin of configurable driver #2
32	DRN2	Drain pin of configurable driver #2
33	DRN1	Drain pin of configurable driver #1
34	SRC1	Source pin of configurable driver #1
35	OUT2	Output 2
36	OUT1	Output 1
EP	GND	Exposed pad: connected to GND

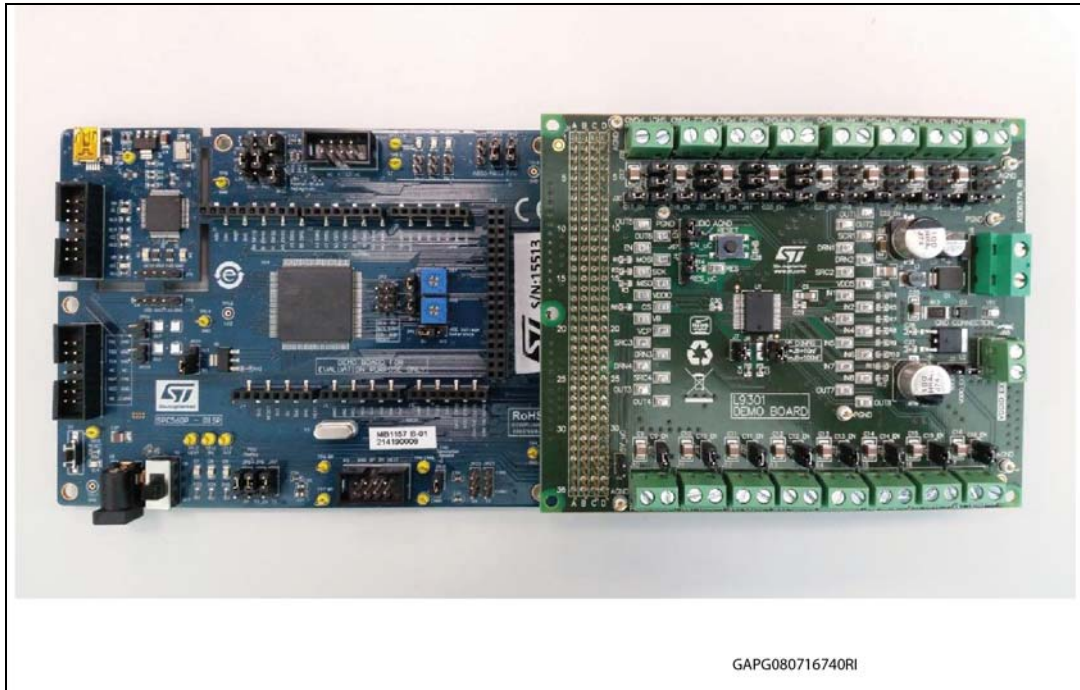
2.1 Evaluation board: main components and connectors

Figure 4. Motherboard main components and connectors



3 SPC560P-DISP + L9301 Eva board

Figure 5. Motherboard system



4 L9301 Demo Board Schematic

The demo board has been designed to be connected directly to SPC560P-DISP demo board, so the 'Header pin' is a 36X4 pin with the signals compatible with SPC560P-DISP Demo Board one:

Figure 6. L9301 Microcontroller connector

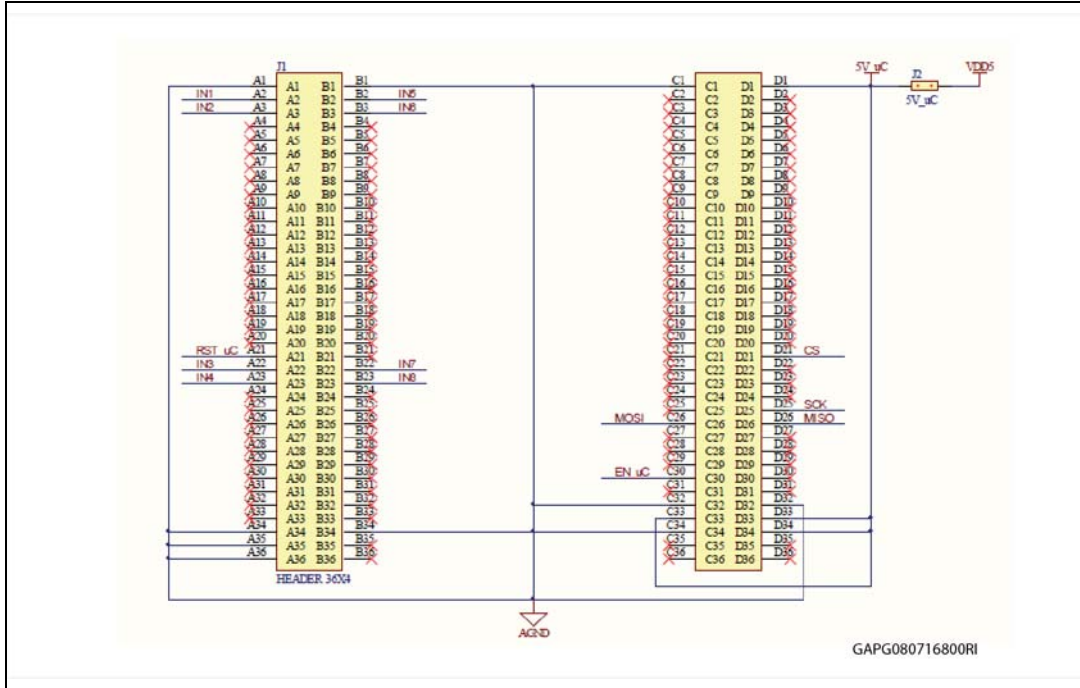


Table 2. Pin description 'HEADER 36X4'

Pin	Symbol	Function
A1	AGND	Board ground
A2	IN1	Discrete Input used to PWM output driver #1
A3	IN2	Discrete input used to PWM output driver #2
A21	RST Uc	Reset from Microcontroller
A22	IN3	Discrete Input used to PWM output driver #3
A23	IN4	Discrete Input used to PWM output driver #4
A34	AGND	Power Ground
A35	AGND	Power Ground
A36	AGND	Power Ground
B1	AGND	Power Ground
B2	IN5	Discrete Input used to PWM output driver #5
B3	IN6	Discrete Input used to PWM output driver #6
B22	IN7	Discrete Input used to PWM output driver #7

Table 2. Pin description 'HEADER 36X4' (continued)

Pin	Symbol	Function
B23	IN8	Discrete Input used to PWM output driver #8
B34	AGND	Power Ground
C1	AGND	Power Ground
C26	MOSI	SPI data in
C30	EN uC	Enable from Microcontroller
C32	AGND	Power Ground
C33	5V uC	5V Supply input from micro or external power
C34	AGND	Power Ground
D1	5V uC	5V Supply input from micro or external power
D21	CS	SPI chip select
D25	SCK	SPI Serial Clock Input
D26	MISO	SPI Data Out
D32	AGND	Power Ground
D33	5V uC	5V Supply input from micro or external power
D34	5V uC	5V Supply input from micro or external power

Figure 7. L9301 Input/Output

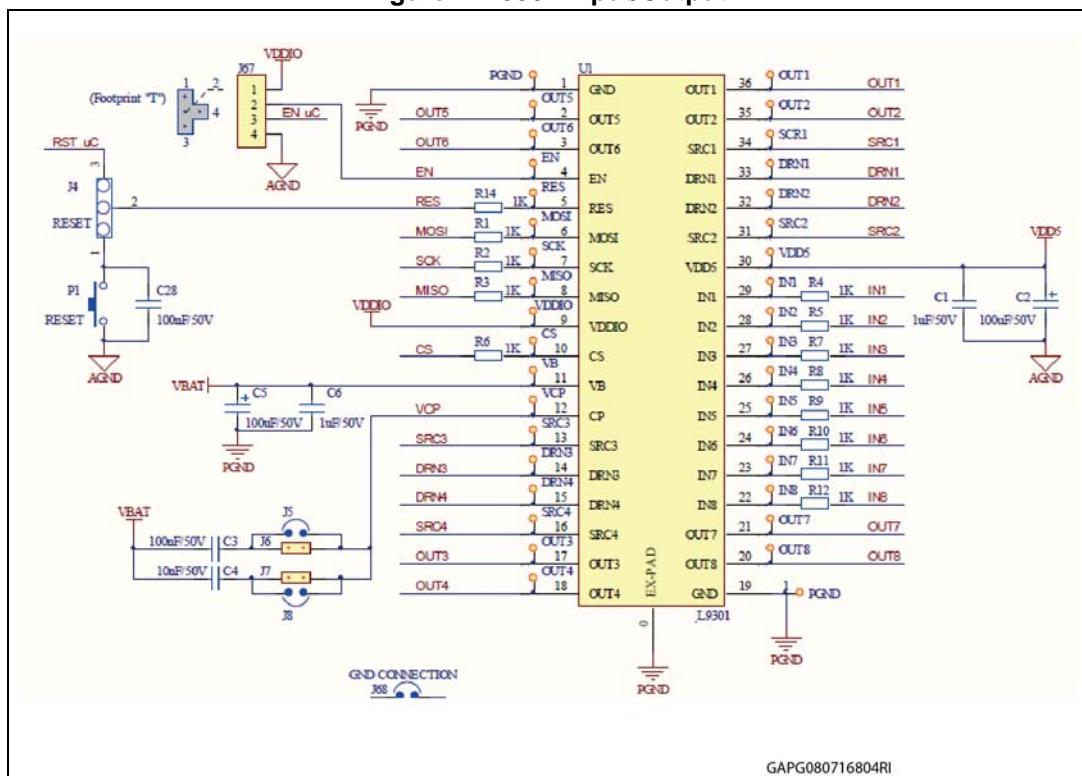
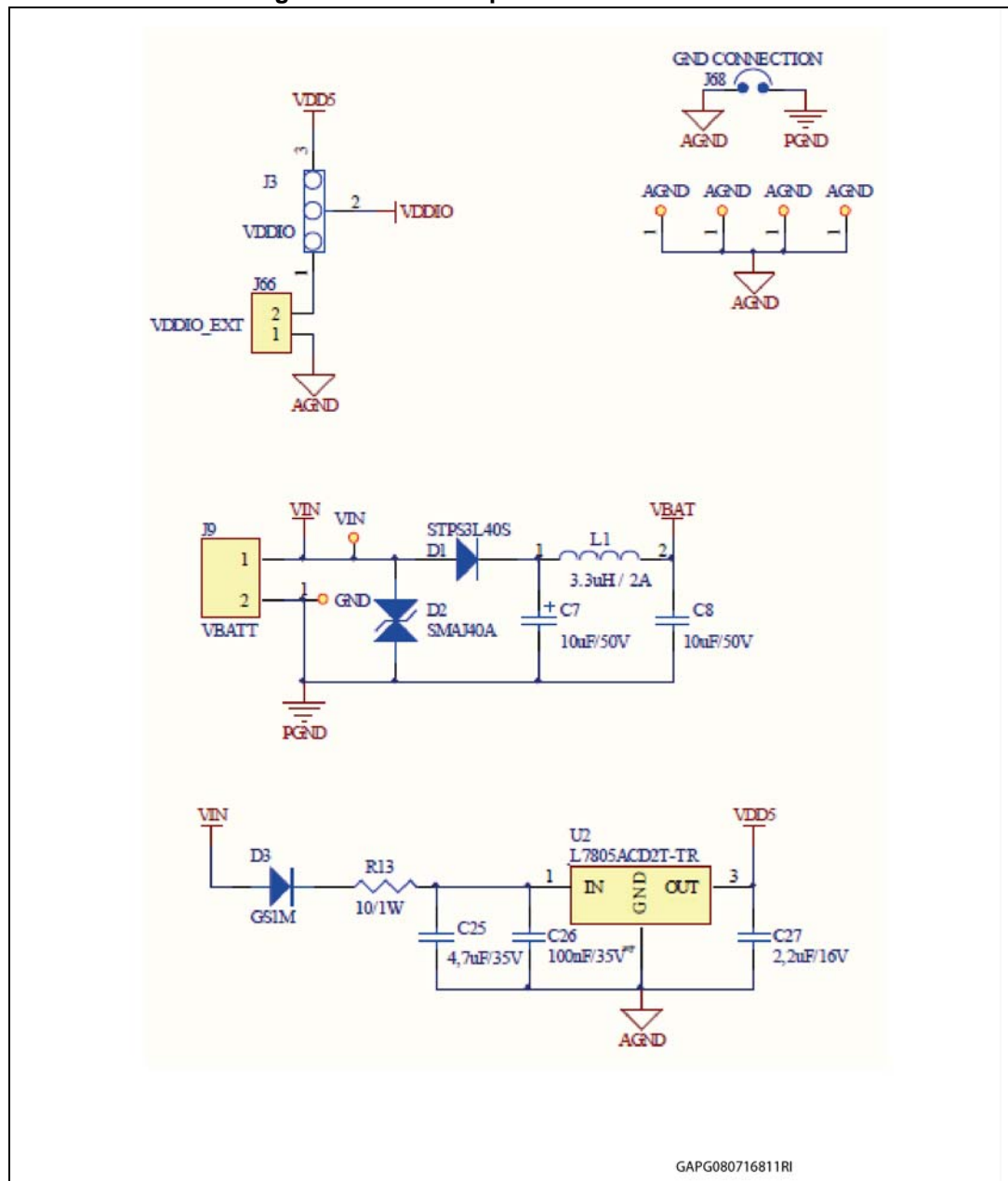


Figure 8 shows the series resistances (1 Kohm) input to 'RES, MOSI, SCK, MISO, CS' and to 'IN1:8'.

In Normal Mode 'EN' input must be to 5 V, you are able to choose 5 V from Vddio or from uC through the "Footprint T".

Moreover, you are able to select the 'Reset Mode' through jumper J4, from uC (A21) or button P1.

Figure 8. L9301 ISO pulse and L7805 Circuit

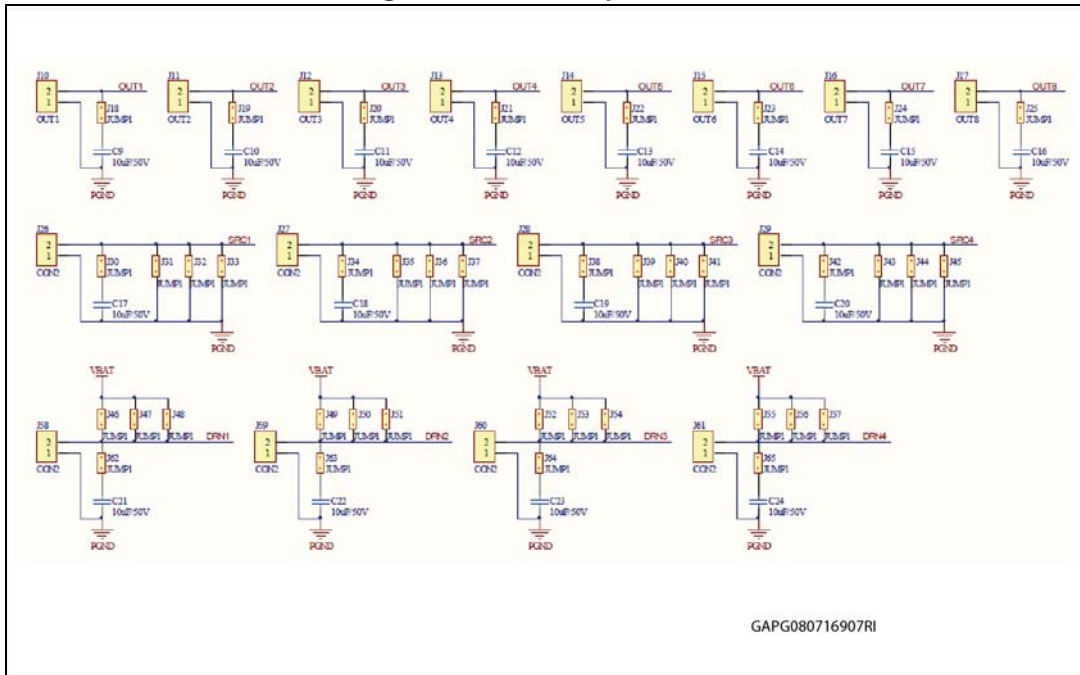


A GND and PGND are connected through the GND CONNECTION J68 (see Figure 9).

VBATT typically is 14 V and is applied to junction J9 (VIN on board), an ISO Pulse filter has been inserted before device power voltage VBAT.

VDDIO must be connected to 5 V, you can choose to use an external 5 V (VDDIO_EXT) or U2 (L7805) output through the jumper J3.

Figure 9. L9301 Output Board



In [Figure 9](#) is shown the device outputs OUT1:8, SRC1:4 and DRN1:4.

OUT1:8 has in parallel a capacitor to GND of 10uF/50V C9:16.

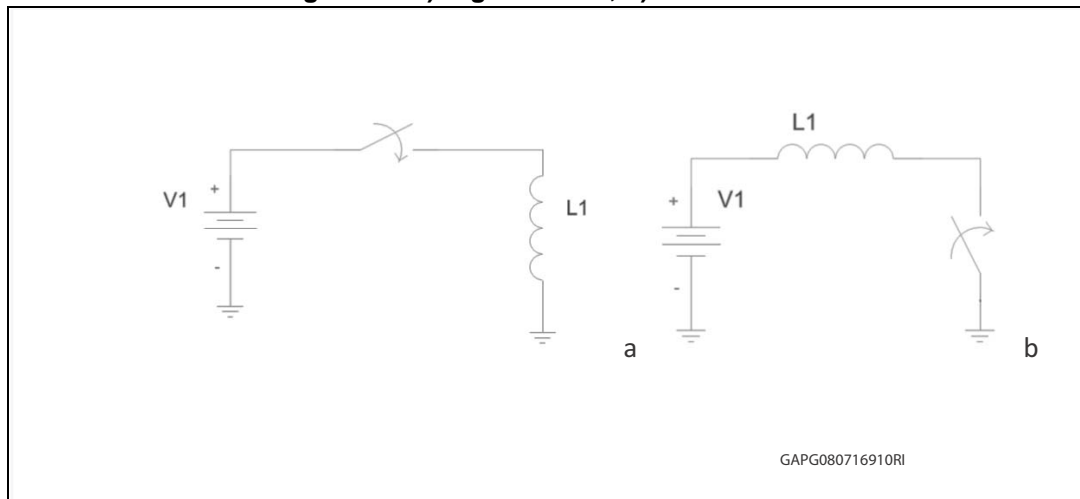
SRC1:4 is able to connect to GND through three jumpers J31:33 ... or has in parallel a capacitor to GND of 10uF/50V C17:20, depending on the device configuration work.

DRN1:4 is able to connect to VBAT through three jumpers J46:48 ... or has in parallel a capacitor to GND of 10uF/50V C21:24, depending on device configuration work.

5 The 4 configurations: tutorial

L9301 device gives #4 different configurations, in this paragraph the user can find the external board connection and jumper set up for each one. The four configurations are set via software by SPI using Graphical Interface (see [Section A.1.1: Document references](#)) and allow to connect the load in low-side and high-side see [Figure 10](#).

Figure 10. a) High-side HS, b) Low-side LS



- HS L9301 MOS output is located between power and load, it's a protection to power voltage;
- LS L9301 MOS out is located between load and ground, represents a protection to ground.

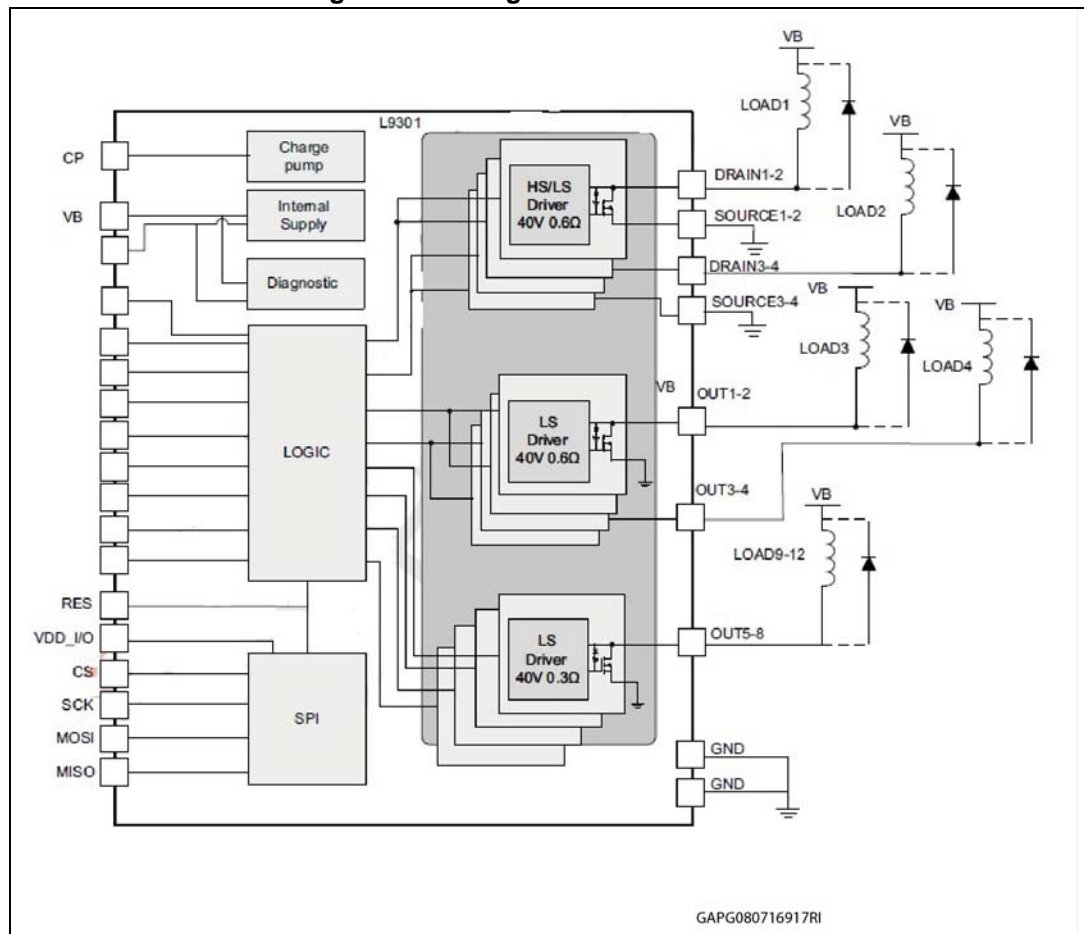
#4 possible configurations are:

- #1 Configuration: 8 LS driver with external free-wheeling diode
- #2 Configuration: 4 LS driver with internal free-wheeling and 4 LS with external free-wheeling diode
- #3 Configuration: 4 HS with internal free-wheeling and 4 LS drivers with external free-wheeling diode
- #4 Configuration: 8 LS with external free-wheeling diode and 4 HS/LS (configurable) drivers

The board, in default mode or after a power off, is in #1 configuration. In order to switch from configuration #1 to another one the user has to open J67 jumper (EN from 5Vdc to 0), select the right configuration from GUI and press SEND. After that, inserting J67 jumper (EN to 5 Vdc), it's possible to READ on the GUI the right actual configuration.

Config 1: 8 LS drivers with external free-wheeling diodes

Figure 11. Configuration#1 connection

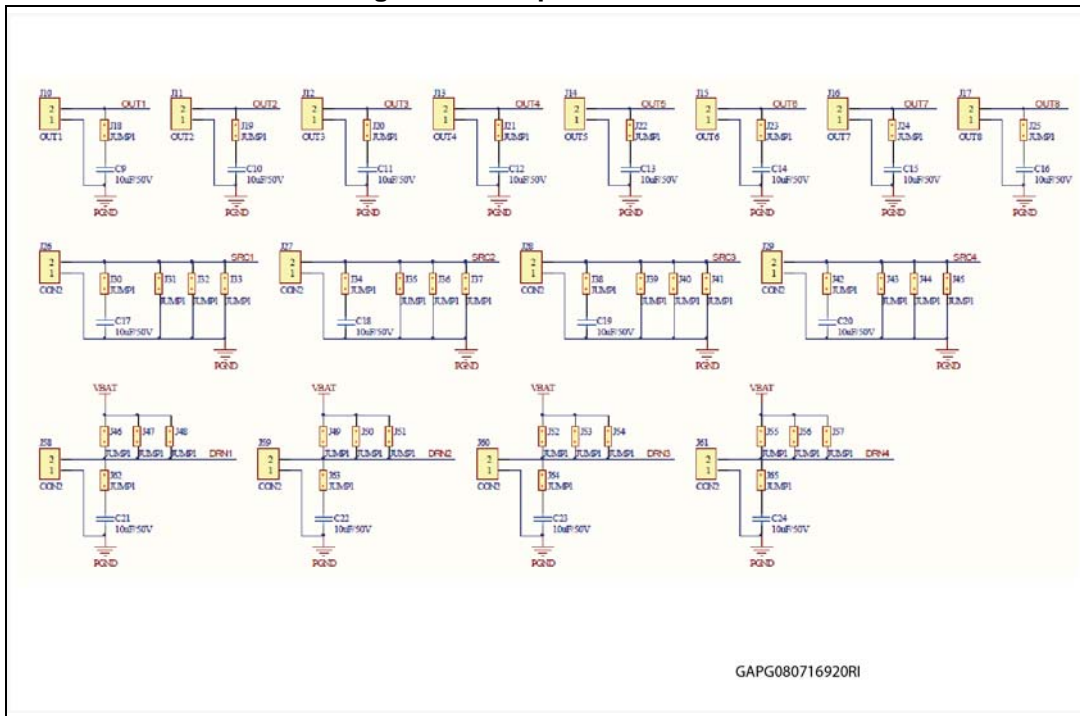


In this configuration 4LS top drivers and 4LS bottom drivers are available, the loads are connected between power voltage and the outputs, it's suggested to insert an external free-wheeling diode for each channel.

Motherboard Jumpers and Connections are showed below:

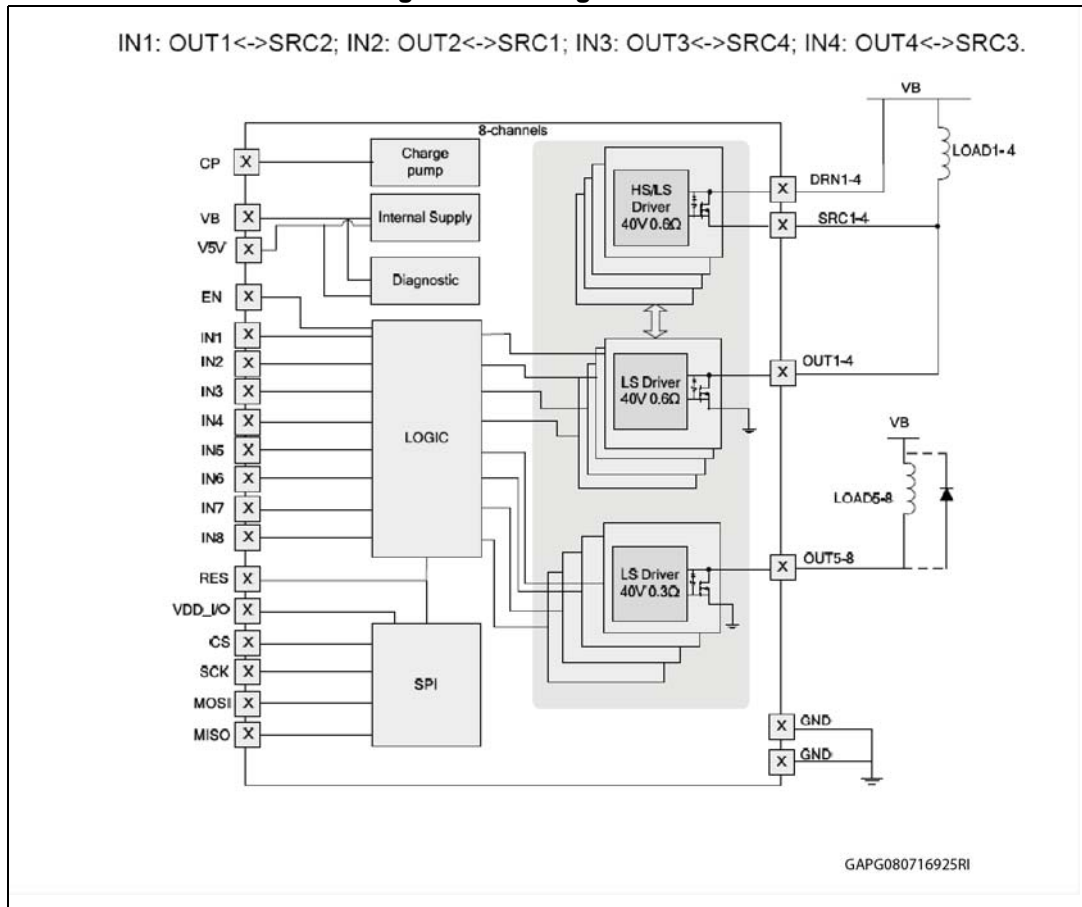
- Load #1: DRN1 and DRN2 externally wired, J62 and J63 closed, J46:51 opened, for SRC1 and SRC2 J30:37 closed
- Load #2: DRN3 and DRN4 externally wired, J64 and J65 closed, J52:57 opened, for SRC3 and SRC4 J38:45 closed
- Load #3: OUT1 and OUT2 externally wired, J18 or J19 (and not both) closed
- Load #4: OUT3 and OUT4 externally wired, J11 or J12 (and not both) closed
- Load #5 between power voltage and OUT5, J22 closed
- Load #6 between power voltage and OUT6, J23 closed
- Load #7 between power voltage and OUT7, J24 closed
- Load #8 between power voltage and OUT8, J25 closed

Figure 12. Jumper demo board



Config 2: 4LS with internal free-wheeling diode, 4LS with external free-wheeling diode

Figure 13. Configuration #2



The top LS drivers have integrated free-wheeling recirculation, otherwise, the bottom LS driver needs an external diode. All the channels can be driven by SPI or PWM.

The IN1-4 drive OUT1-4 so LOAD1-4, "PWM enable" bit must be set to 1.

The IN5-8 drive OUT5-8 so LOAD5-8.

When the channel (IN1-4 and OUT1-4) is OFF, the high-side works as integrated free-wheeling diode so DRN1-4 and SRC1-4 must be ON.

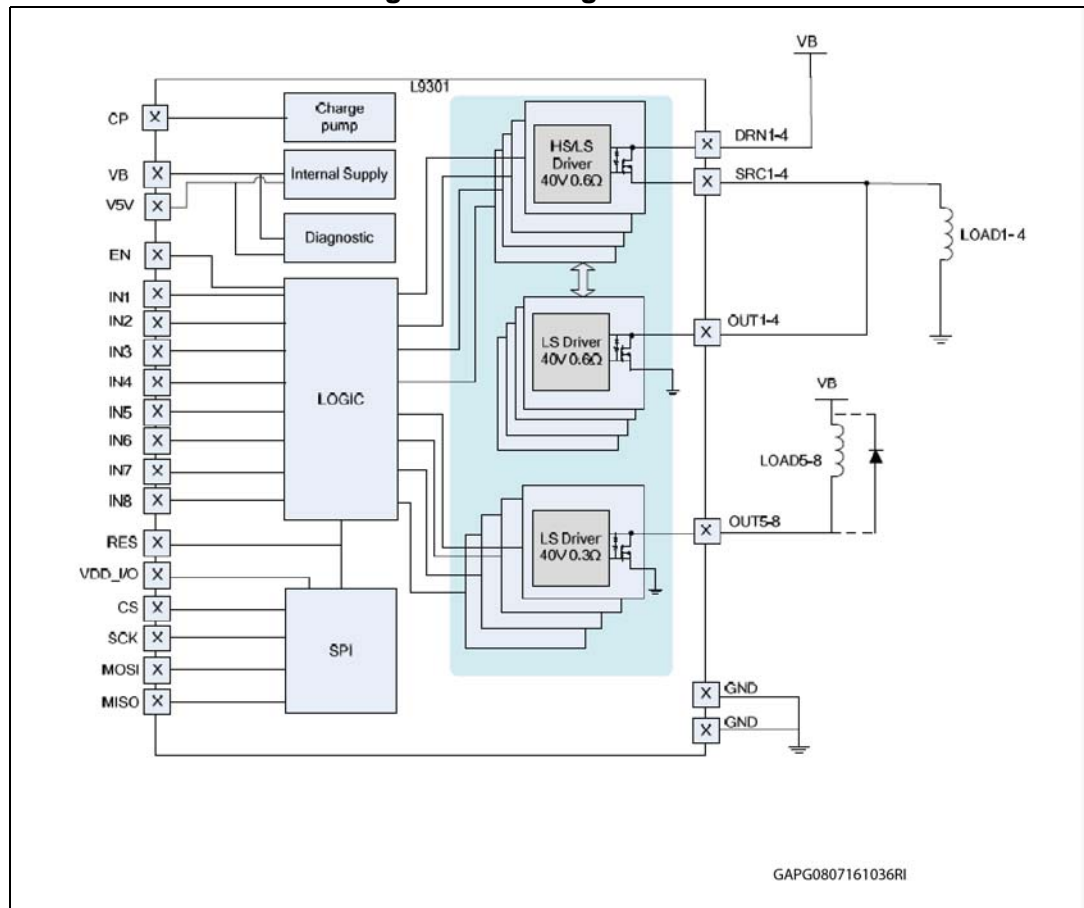
The configuration bit must be set on "driven by SPI".

Motherboard Jumpers and Connections are showed below:

- Load #1: DRN1 to Vbat so J46:48 closed and J62 opened, SRC1 and OUT1 externally wired, J30:33 opened, J18 or J30 (and not both) closed
- Load #2: DRN2 to Vbat so J49:51 closed and J63 opened, SRC2 and OUT2 externally wired, J34:37 opened, J19 or J34 (and not both) closed
- Load #3: DRN3 to Vbat so J52:54 closed and J64 opened, SRC3 and OUT3 externally wired, J38:41 opened, J20 or J38 (and not both) closed
- Load #4: DRN4 to Vbat so J55:57 closed and J65 opened, SRC4 and OUT4 externally wired, J42:45 opened, J21 or J42 (and not both) closed
- Load #5 between power voltage and OUT5, J22 closed
- Load #6 between power voltage and OUT6, J23 closed
- Load #7 between power voltage and OUT7, J24 closed
- Load #8 between power voltage and OUT8, J25 closed

Config 3: 4HS with internal free-wheeling diodes, 4LS with external free-wheeling diodes

Figure 14. Configuration #3



In this configuration there are 4 HS with integrated free-wheeling diode and 4 LS with external ones. All channels can be driven by SPI or PWM parallel signal.

To enable SRC1:4, Bit "PWM enable" must be set to 1 (see [Section A.1.1: Document references](#)).

The IN1-4 controls HS power SRC1-4 to drive LOAD1-4.

The IN5-8 controls OUT 5-8 to drive LOAD 5-8.

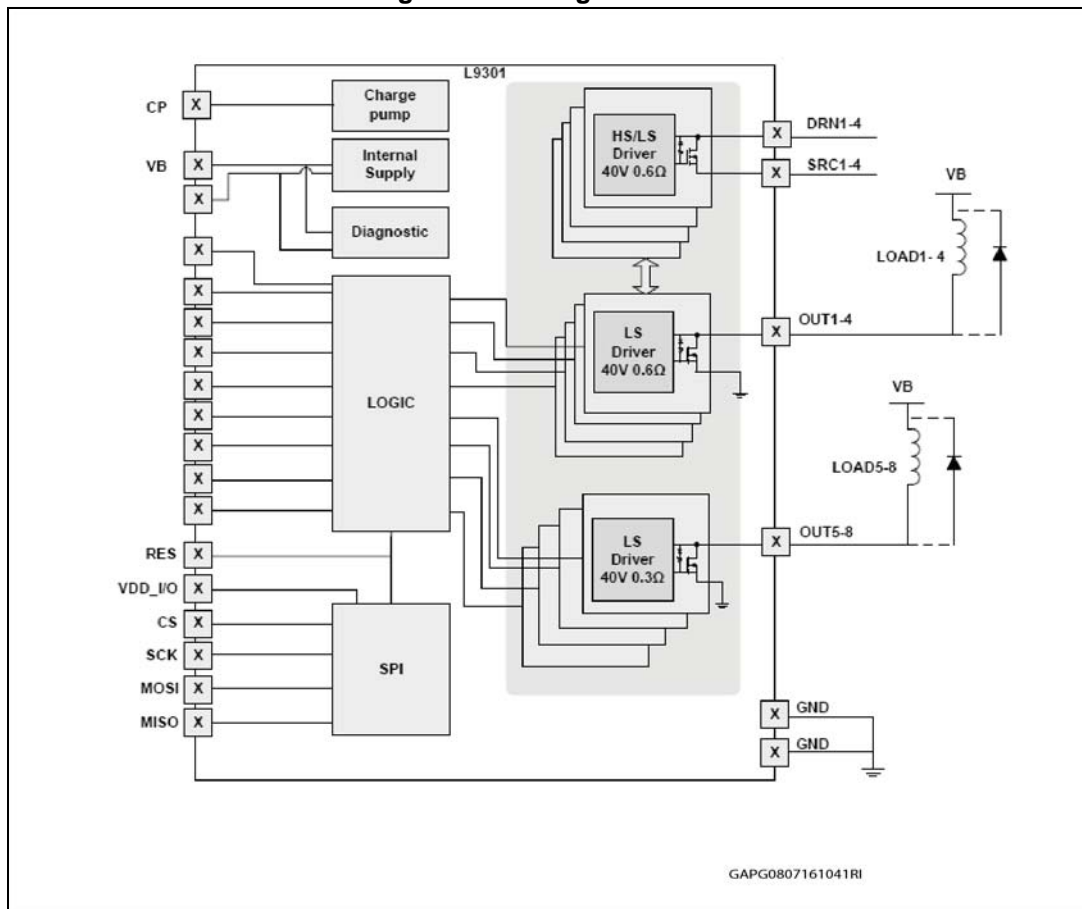
The selected configuration must be configured by SPI.

Motherboard Jumpers and Connections are showed below:

- Load #1: DRN1 to Vbat so J46:48 closed and J62 opened, SRC1 and OUT1 externally wired, J30:33 opened, J18 or J30 (and not both) closed
- Load #2: DRN2 to Vbat so J49:51 closed and J63 opened, SRC2 and OUT2 externally wired, J34:37 opened, J19 or J34 (and not both) closed
- Load #3: DRN3 to Vbat so J52:54 closed and J64 opened, SRC3 and OUT3 externally wired, J38:41 opened, J20 or J38 (and not both) closed
- Load #4: DRN4 to Vbat so J55:57 closed and J65 opened, SRC4 and OUT4 externally wired, J42:45 opened, J21 or J42 (and not both) closed
- Load #5 between power voltage and OUT5, J22 closed
- Load #6 between power voltage and OUT6, J23 closed
- Load #7 between power voltage and OUT7, J24 closed
- Load #8 between power voltage and OUT8, J25 closed

Config 4: 4 configurable drivers and 8 LS drivers

Figure 15. Configuration #4



In this configuration there are 4HS/LS drivers and 8LS drivers available.

The 8LS drivers can be driven by SPI, so the IN1-8 drive OUT1-8, otherwise the configurable drivers can be driven only by SPI and can be configured separately as LS or HS using the dedicated SPI bit.

Motherboard Jumpers and Connections for LOAD1-8 are showed below:

- Load #1 between power voltage and OUT1, J18 closed
- Load #2 between power voltage and OUT2, J19 closed
- Load #3 between power voltage and OUT3, J20 closed
- Load #4 between power voltage and OUT4, J21 closed
- Load #5 between power voltage and OUT5, J22 closed
- Load #6 between power voltage and OUT6, J23 closed
- Load #7 between power voltage and OUT7, J24 closed
- Load #8 between power voltage and OUT8, J25 closed

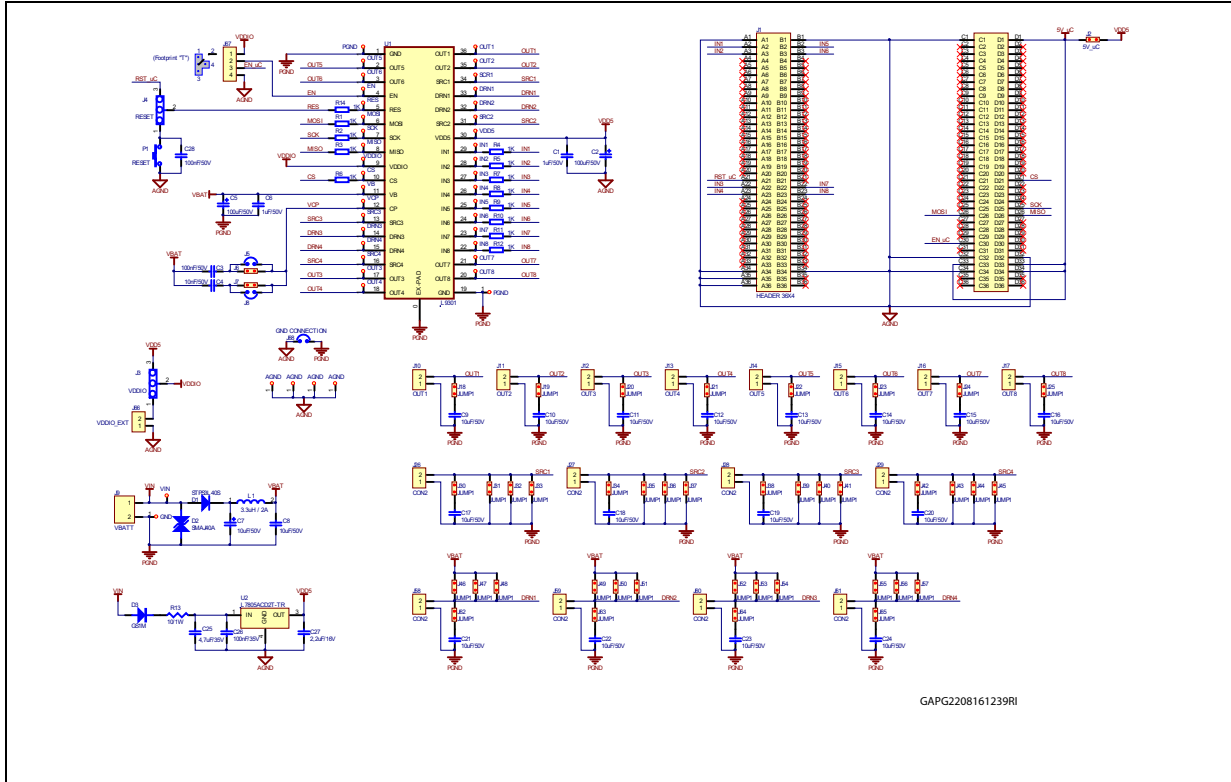
6 Getting started

6.1 Start up

1. Connect SPC560P-DISP and L9301 Demo Board
2. Configure all the jumpers according to chosen configuration
3. Configure J3 according to $V_{ddio}=V_{ddio_Ext}$ or $V_{ddio}=V_{dd5}$
4. Connect a Power supply to L9301 Demo Board respecting the right polarity
5. Connect the Load (one or more) with a current probe to the L9301 outputs
6. Switch on the power supply
7. Open GUI L9301 and set COM,
8. Choose one of 4 configurations ([Section 5: The 4 configurations: tutorial](#))
9. Choose frequency working and duty cycle, select the desired Load and press START.
10. If you can measure the current in the load connected, L9301 and SPC560P-DISP Demo Board are correctly working.
11. For further information see the GUI Documentation and Manual (see [Section A.1.1: Document references](#)).

Appendix A L9301 Evaluation board schematic

Figure 16. L9301 Evaluation board schematic



A.1 Further information

A.1.1 Document references

- *Automotive octal low side driver or quad low side plus quad high side driver (L9301, DocID028688).*
- *L9301: Firmware and GUI interface (UM2081, DocID029479).*

Revision history

Table 3. Document revision history

Date	Revision	Changes
22-Aug-2016	1	Initial release.

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