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CY62126EV18 MoBL®

1-Mbit (64 K × 16) Static RAM

Features

- High speed: 70 ns
- Temperature ranges
  - Industrial: –40 °C to +85 °C
- Voltage range: 1.65 V to 1.95 V
- Pin compatible with CY62126EV30
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 4 µA
- Ultra low active power
  - Typical active current: 1.3 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Automatic power down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Offered in Pb-free 48-ball very fine-pitch ball grid array (VFBGA) package

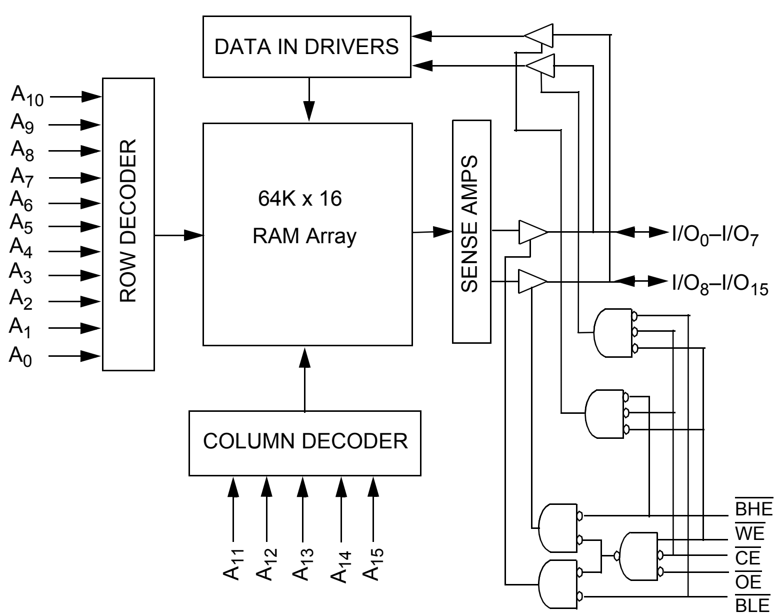
Functional Description

The CY62126EV18 is a high-performance CMOS static RAM organized as 64K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}$ HIGH). The input and output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH) or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O_0 through I/O_7) is written into the location specified on the address pins (A_0 through A_{15}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{15}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on I/O_8 to I/O_{15}. See the Truth Table on page 11 for a complete description of read and write modes.

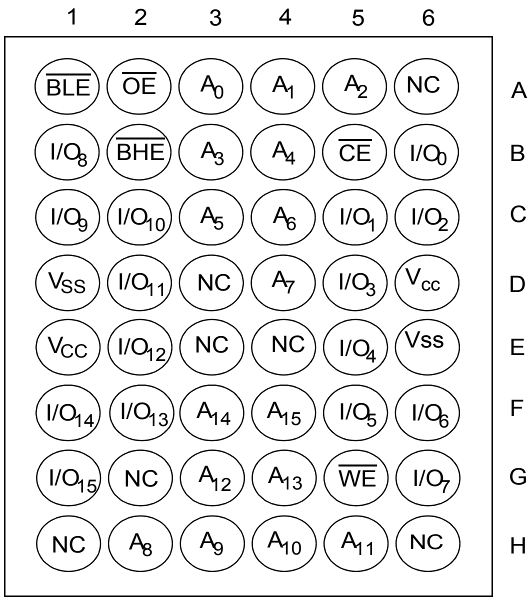
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 48-ball VFBGA Pinout (Top View)



Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating, I_{CC} (mA)				Standby, I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ[2]	Max		Typ[2]	Max	Typ[2]	Max	Typ[2]	Max
CY62126EV18LL	Industrial	1.65	1.8	1.95	70	1.3	2	11	12	1	4

Notes
1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the battery life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +150 °C

Ambient temperature with power applied .... –55 °C to +125 °C

Supply voltage to ground potential [3, 4]..................... –0.3 V to 2.25 V (V_{CCmax} + 0.3 V)

DC voltage applied to outputs in High Z state [3, 4] .... –0.3 V to 2.25 V (V_{CCmax} + 0.3 V)

DC input voltage [3, 4] .... –0.3 V to 2.25 V (V_{CCmax} + 0.3 V)

Output current into outputs (LOW) .... 20 mA

Static discharge voltage (MIL-STD-883, Method 3015) .... > 2001 V

Latch-up current .... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC} [5]
CY62126EV18LL	Industrial	–40 °C to +85 °C	1.65 V to 1.95 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		70 ns			Unit
				Min	Typ [6]	Max	
V_{OH}	Output high voltage	I_{OH} = –0.1 mA		1.4	–	–	V
V_{OL}	Output low voltage	I_{OL} = 0.1 mA		–	–	0.2	V
V_{IH}	Input high voltage	V_{CC} = 1.65 V to 1.95 V		1.4	–	V_{CC} + 0.2 V	V
V_{IL}	Input low voltage	V_{CC} = 1.65 V to 1.95 V		–0.2	–	0.4	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}		–1	–	+1	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	$f = f_{max} = 1/t_{RC}$	V_{CC} = V_{CCmax} I_{OUT} = 0 mA CMOS levels	–	11	12	mA
		f = 1 MHz		–	1.3	2.0	
I_{SB1} [7]	Automatic CE power down current —CMOS inputs	$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V, $f = f_{max}$ (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$, and $\overline{WE}$), V_{CC} = 1.95 V		–	1	4	µA
I_{SB2} [7]	Automatic CE power down current —CMOS inputs	$\overline{CE}$ ≥ V_{CC} – 0.2 V, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} ≤ 0.2 V, f = 0, V_{CC} = 1.95 V		–	1	4	µA

Notes
3. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
4. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
5. Full device AC operation assumes a 100 µs ramp time from 0 to V_{cc}(min) and 200 µs wait time after V_{cc} stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
7. Chip enable ($\overline{CE}$) needs to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

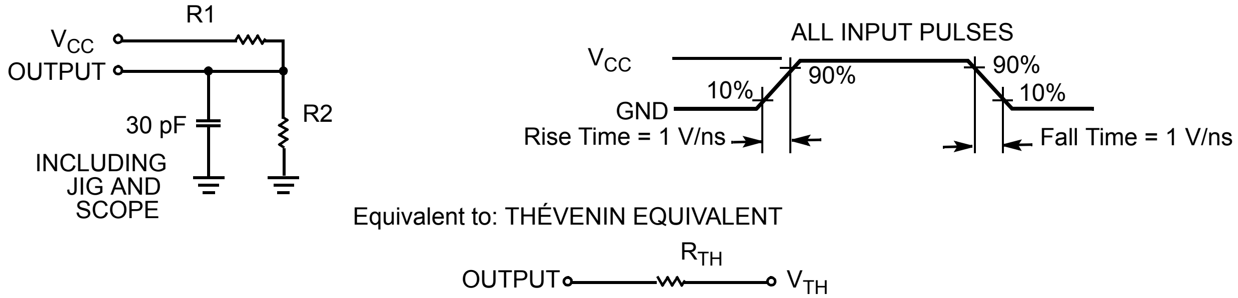
Parameter[8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	48-ball VFBGA Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still Air, soldered on a 4.25 × 1.125 inch, two-layer printed circuit board	58.85	°C/W
Θ_{JC}	Thermal resistance (junction to case)		17.01	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	1.65 V–1.95 V	Unit
R1	13500	Ω
R2	10800	Ω
R_{TH}	6000	Ω
V_{TH}	0.8	V

Note
8. Tested initially and after any design or process changes that may affect these parameters.

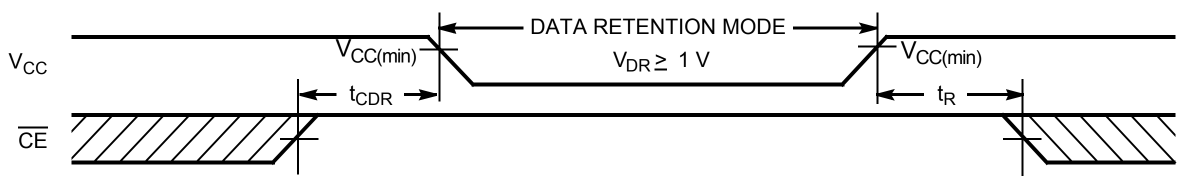
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [9]	Max	Unit
V_{DR}	V_{CC} for data retention			1	–	–	V
I_{CCDR}[10]	Data retention current	$V_{CC} = V_{DR}$, $\overline{CE} \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Industrial	–	–	3	µA
t_{CDR}[11]	Chip deselect to data retention time			0	–	–	ns
t_R[12]	Operation recovery time			70	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25$ °C.
10. Chip enable ($\overline{CE}$) needs to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} > 100$ µs.

Switching Characteristics

Over the Operating Range

Parameter [13]	Description	70 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	70	–	ns
t_{AA}	Address to data valid	–	70	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	70	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z [14]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z [14, 15]	–	25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z [14]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z [14, 15]	–	25	ns
t_{PU}	$\overline{CE}$ LOW to power up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power down	–	70	ns
t_{DBE}	$\overline{BHE}$ / $\overline{BLE}$ LOW to data valid	–	35	ns
t_{LZBE}	$\overline{BHE}$ / $\overline{BLE}$ LOW to Low Z [14]	5	–	ns
t_{HZBE}	$\overline{BHE}$ / $\overline{BLE}$ HIGH to High Z [14, 15]	–	25	ns
Write Cycle [16, 17]				
t_{WC}	Write cycle time	70	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	60	–	ns
t_{AW}	Address setup to write end	60	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	60	–	ns
t_{BW}	$\overline{BHE}$ / $\overline{BLE}$ pulse width	60	–	ns
t_{SD}	Data setup to write end	35	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to High Z [14, 15]	–	25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z [14]	10	–	ns

Notes

13. Test conditions assume signal transition time of 1.8 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
14. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
15. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
16. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$ or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must refer to the edge of signal that terminates write.
17. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address transition controlled) [18, 19]

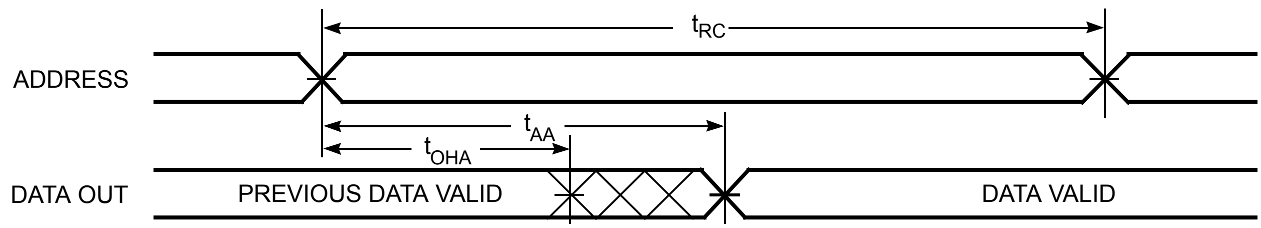
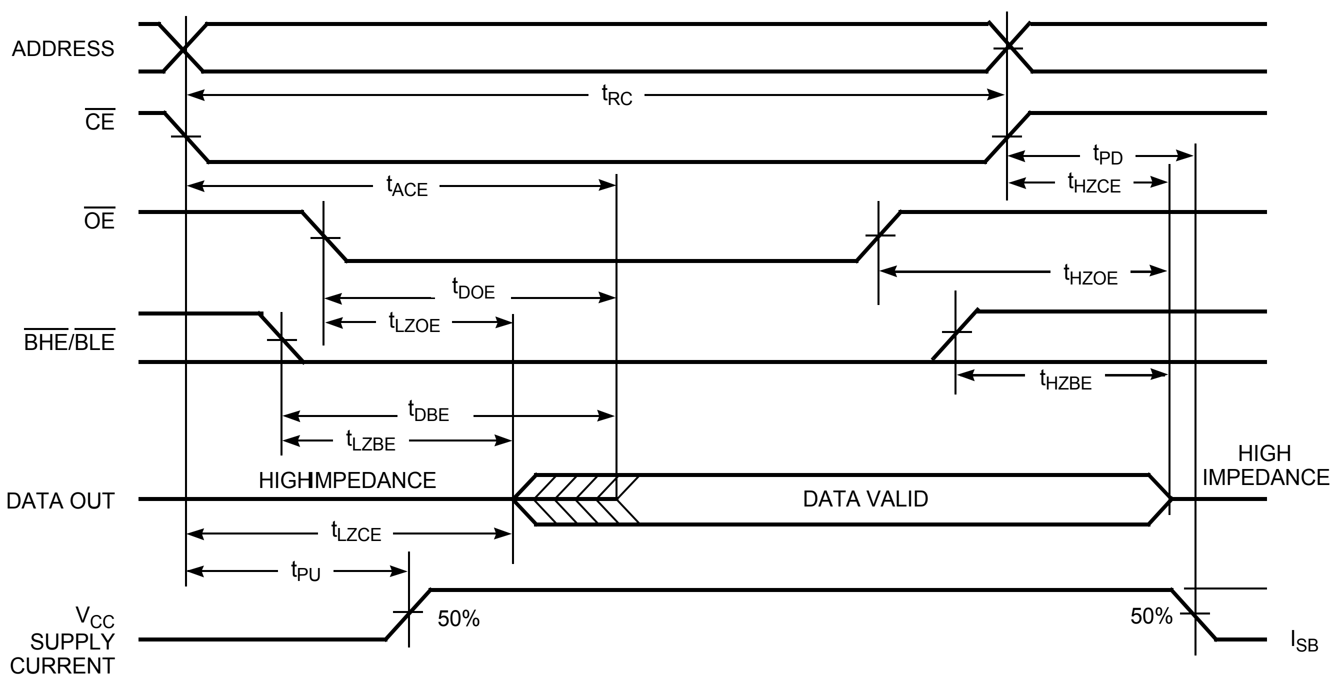


Figure 5. Read Cycle No. 2 ($\overline{OE}$ controlled) [19, 20]



Notes

18. The device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}, $\overline{BHE}$, $\overline{BLE}$, or both = V_{IL}.
19. $\overline{WE}$ is high for read cycle.
20. Address valid before or similar to $\overline{CE}$ and $\overline{BHE}$, $\overline{BLE}$ transition LOW.

Switching Waveforms *(continued)*

Figure 6. Write Cycle No. 1 (WE controlled) [21, 22, 23]

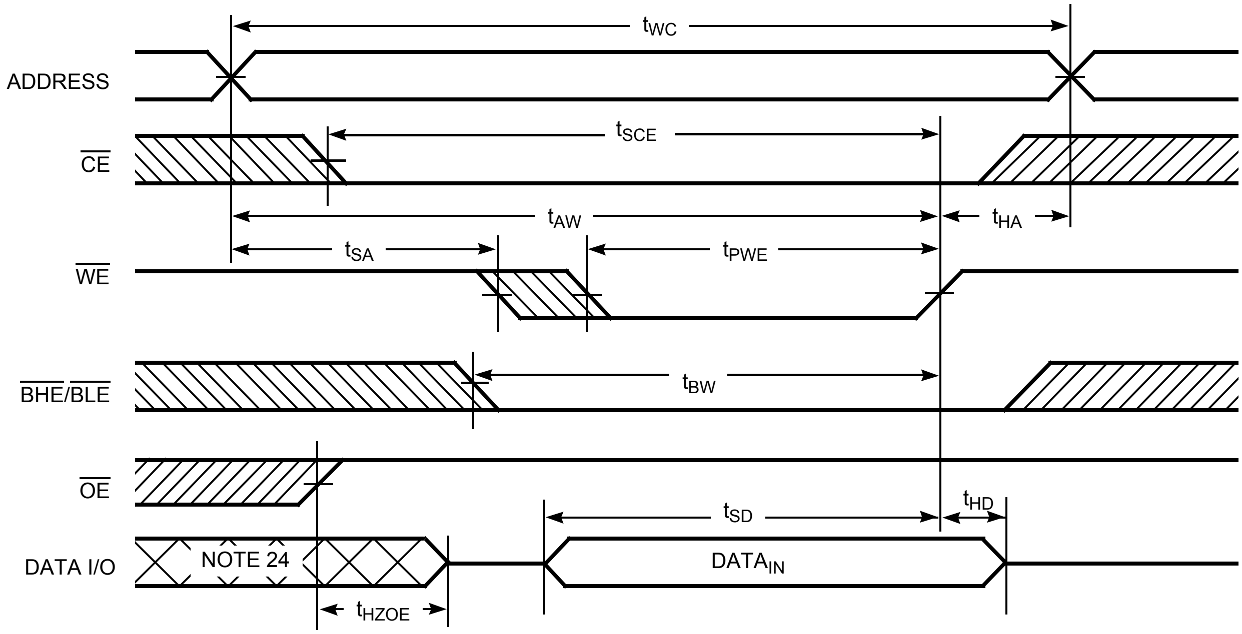
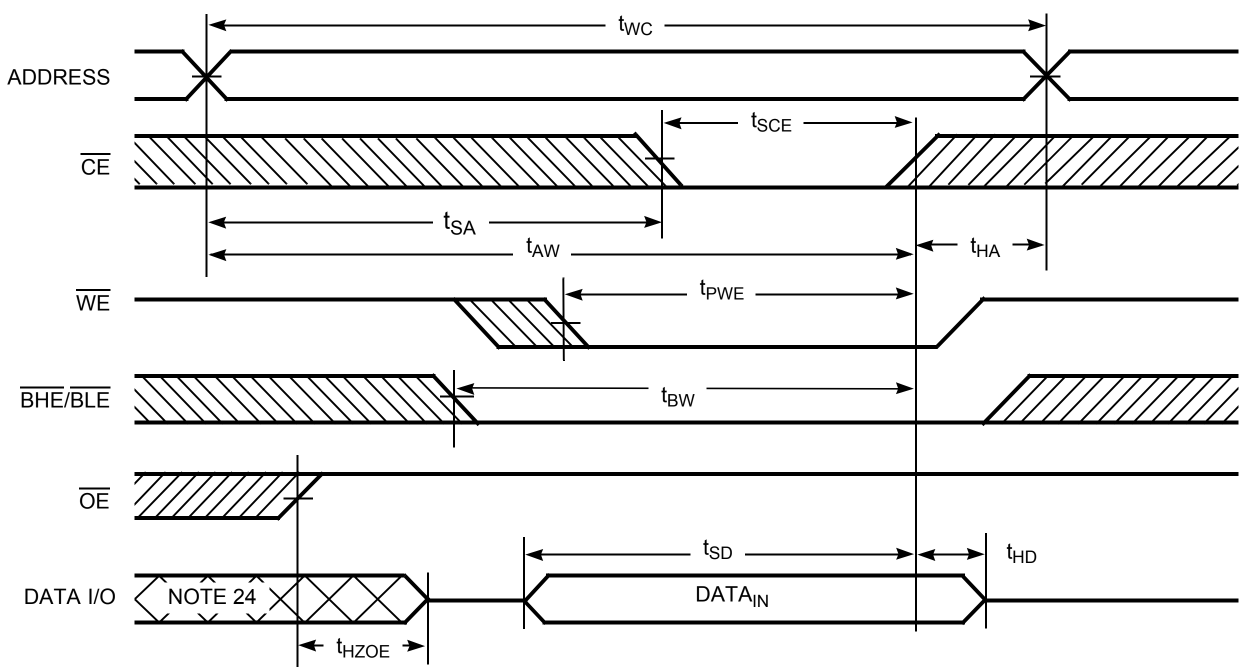


Figure 7. Write Cycle No. 2 (CE controlled) [21, 22, 23]



Notes

21. The internal write time of the memory is defined by the overlap of WE, CE = V_{IL}, BHE, BLE or both = V_{IL}. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must refer to the edge of signal that terminates write.
22. Data I/O is high impedance if OE = V_{IH}.
23. If CE goes high simultaneously with WE = V_{IH}, the output remains in a high impedance state.
24. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms *(continued)*

Figure 8. Write Cycle No. 3 (WE controlled, OE LOW [25, 26]

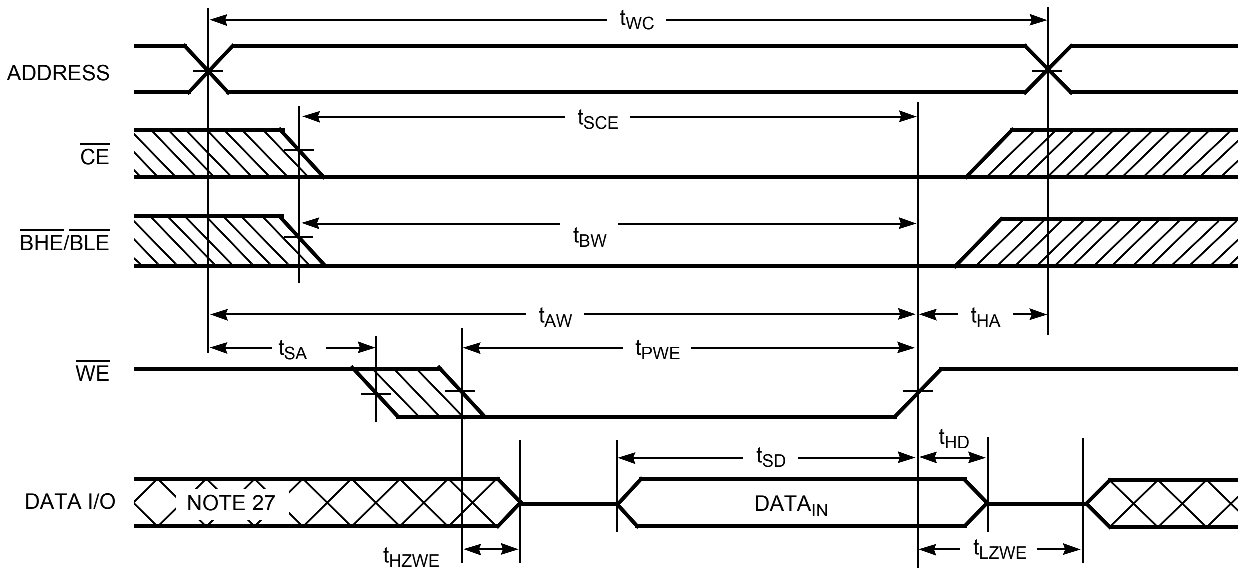
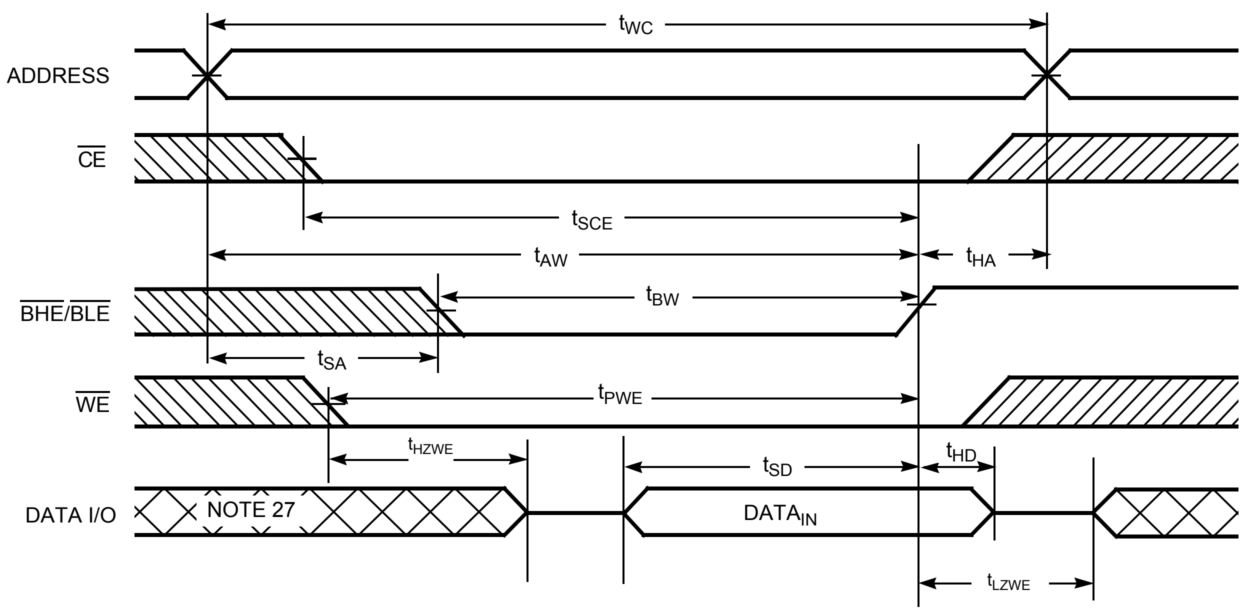


Figure 9. Write Cycle No. 4 (BHE/BLE controlled, OE LOW) [25]



Notes
25. If CE goes high simultaneously with WE = V_{IH}, the output remains in a high impedance state.
26. The minimum write cycle pulse width should be equal to sum of t_{SD} and t_{HZWE}.
27. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE}$[28]	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	High Z	Deselect/power down	Standby (I_{SB})
L	X	X	H	H	High Z	Output disabled	Active (I_{CC})
L	H	L	L	L	Data out (I/O_0–I/O_{15})	Read	Active (I_{CC})
L	H	L	H	L	Data out (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Read	Active (I_{CC})
L	H	L	L	H	Data out (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Read	Active (I_{CC})
L	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	L	X	L	L	Data in (I/O_0–I/O_{15})	Write	Active (I_{CC})
L	L	X	H	L	Data in (I/O_0–I/O_7); I/O_8–I/O_{15} in High Z	Write	Active (I_{CC})
L	L	X	L	H	Data in (I/O_8–I/O_{15}); I/O_0–I/O_7 in High Z	Write	Active (I_{CC})

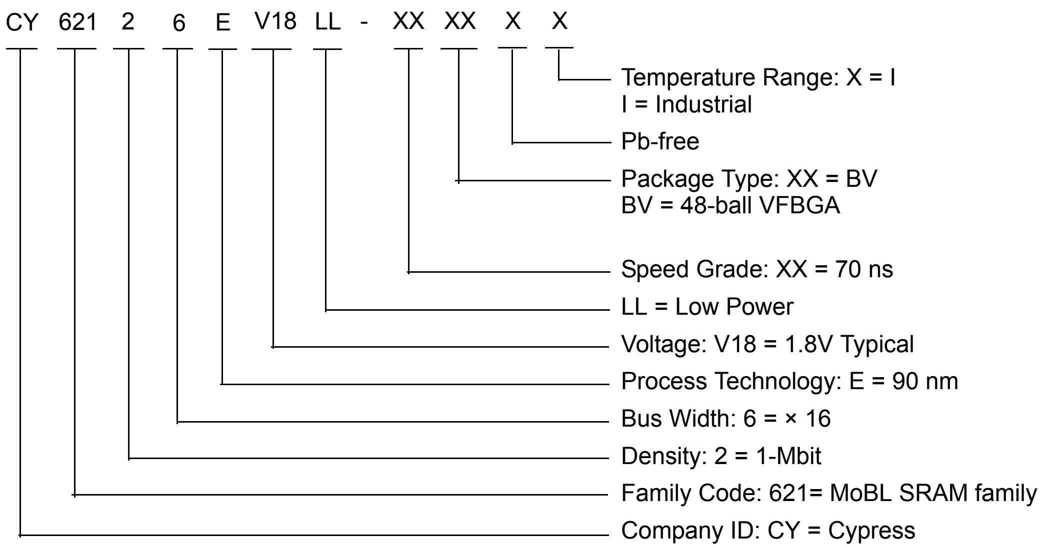
Note
28. Chip enable must be at CMOS levels (not floating). Intermediate voltage levels on this pin is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY62126EV18LL-70BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial

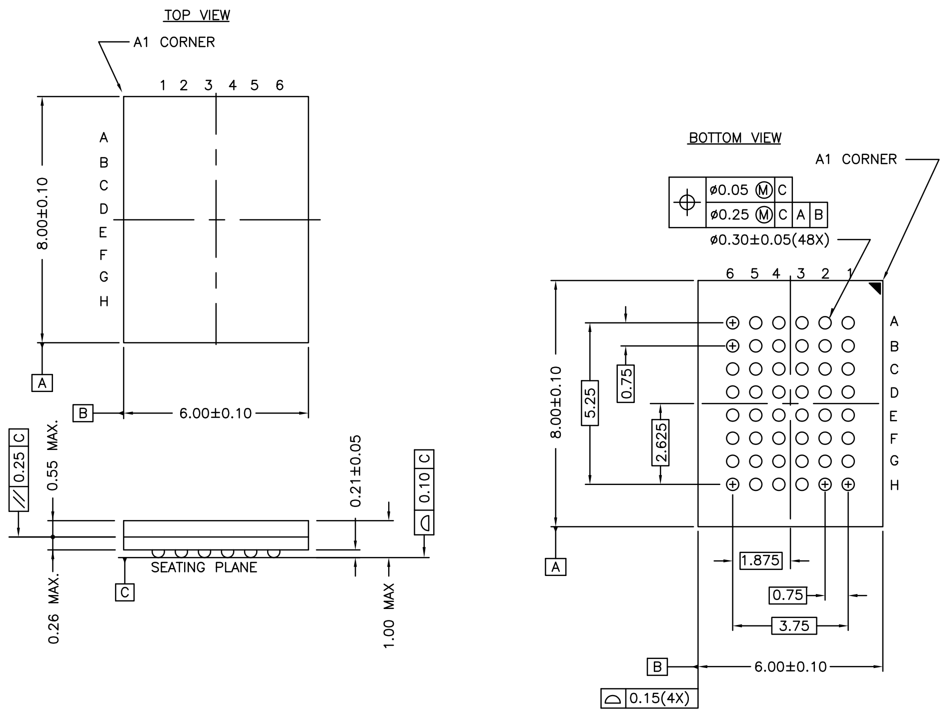
Contact your local Cypress sales representative for availability of other parts.

Ordering Code Definitions



Package Diagram

Figure 10. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
RAM	Random Access Memory
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62126EV18 MoBL®, 1-Mbit (64 K × 16) Static RAM Document Number: 001-94739				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	4547224	VINI	11/07/2014	New datasheet.
*A	5536310	VINI	11/29/2016	Changed datasheet status to Final. Updated template.
*B	6013631	AESATMP9	01/04/2018	Updated logo and copyright.

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