

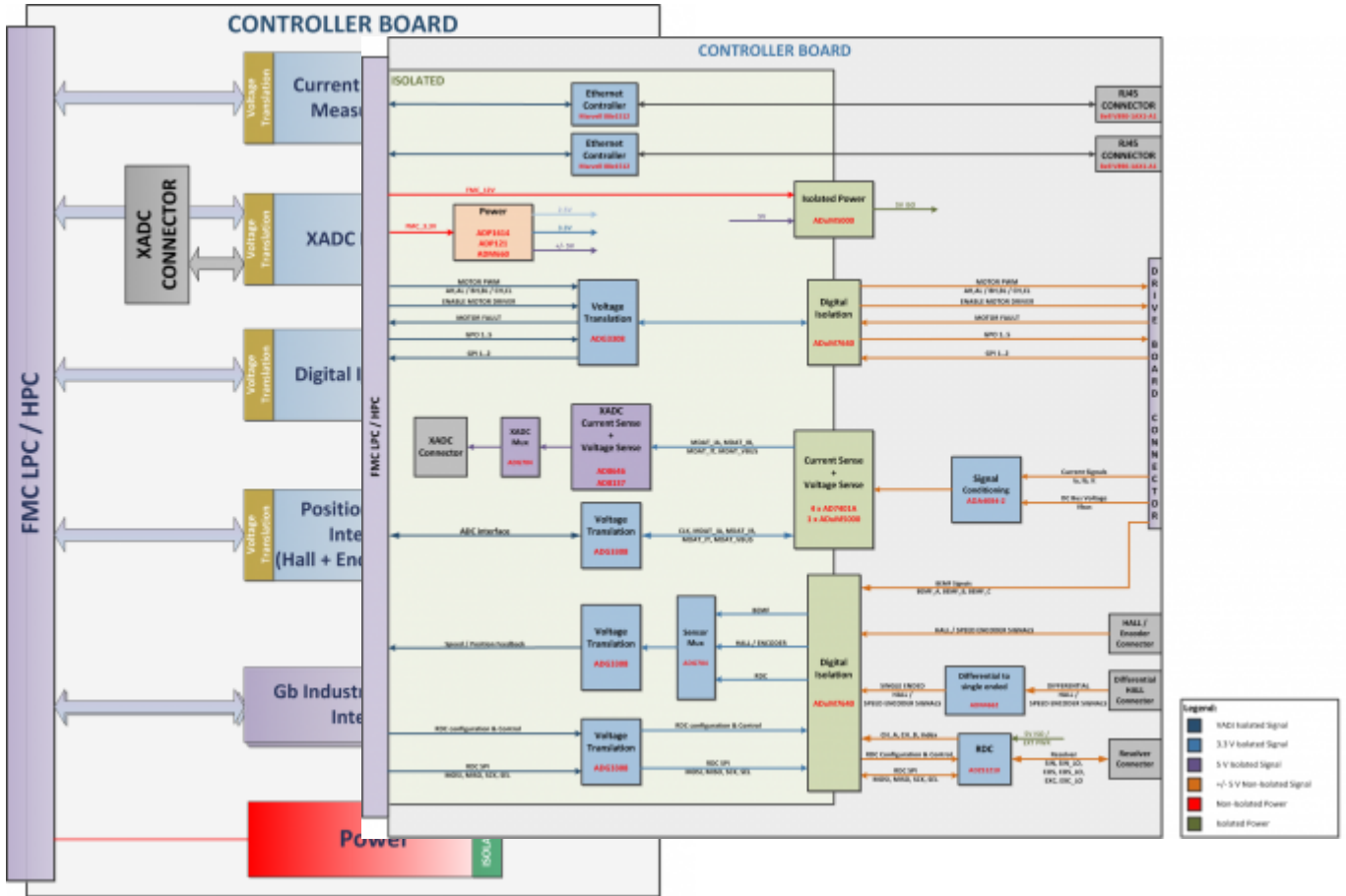
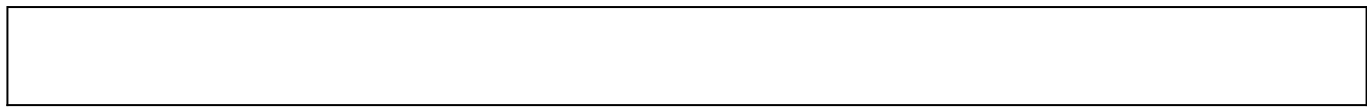


AD-FMCMOTCON1-EBZ Controller Board

Features and Block Diagram

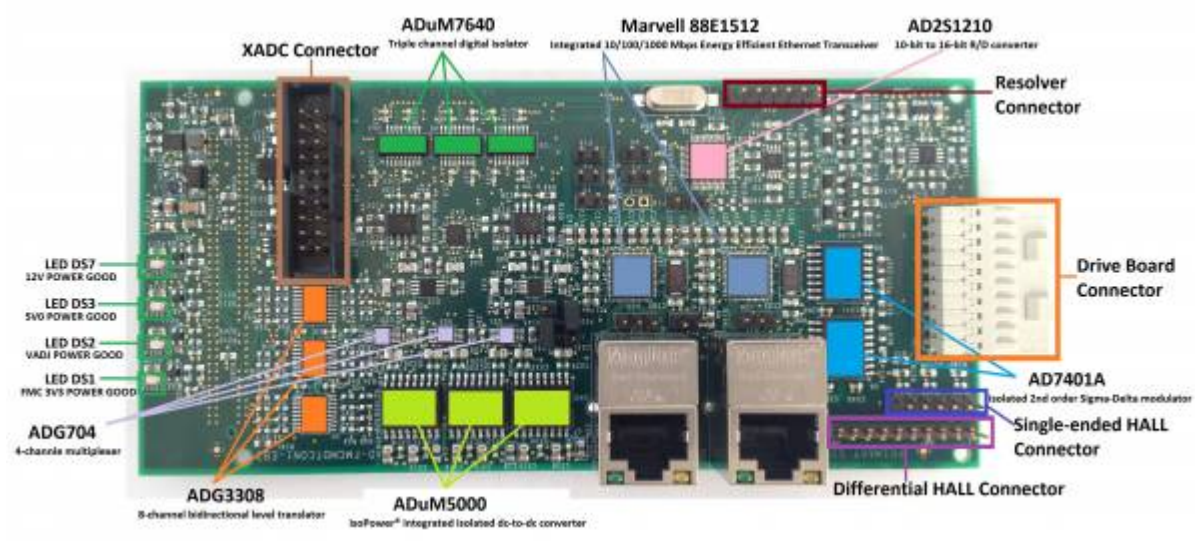
- Compatible with all Xilinx FPGA platforms with FMC LPC or HPC connectors
- 2 x Gbit Ethernet PHYs for high speed industrial communication
- Hall + Differential Hall + Encoder + Resolver interfaces
- Current and voltage measurement using isolated ADCs
- Xilinx XADC interface
- Fully isolated control and feedback signals

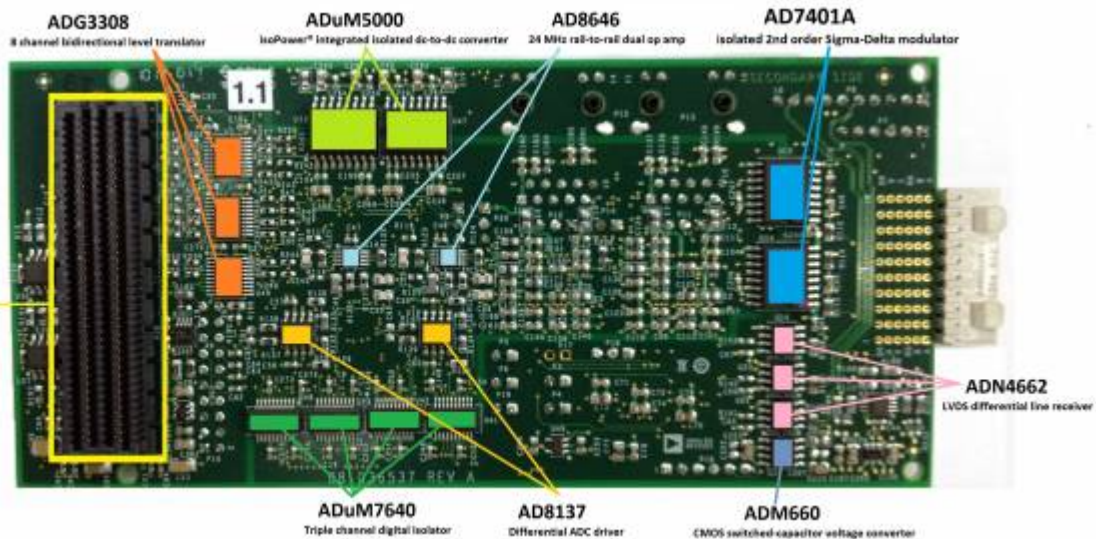
[Simplified Block Diagram](#) | [Detailed Block Diagram](#)



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Picture and Main Components





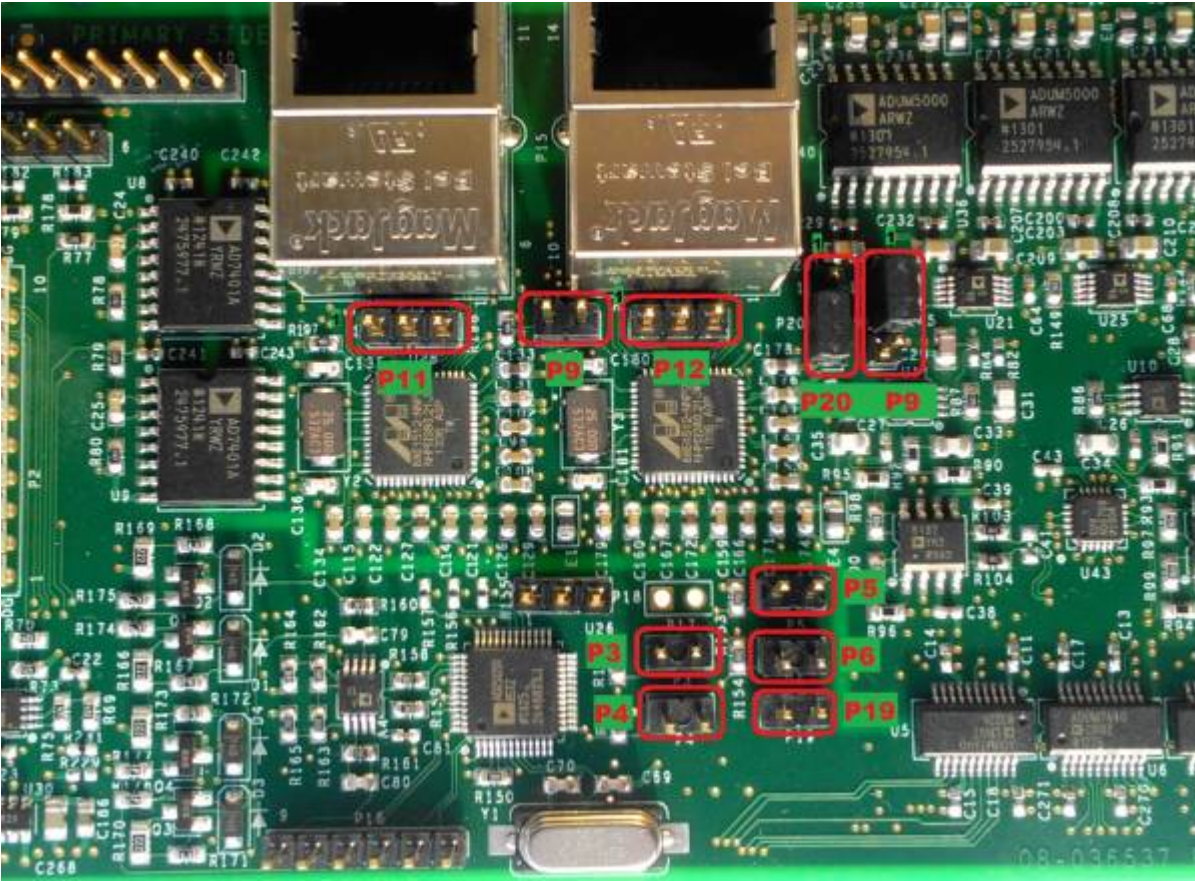
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Key Parts

Measurement	
AD7401A	5 kV rms, isolated 2nd order Sigma-Delta modulator
ADA4084-2	30 V, Low noise, rail-to-rail I/O, low power operational amplifier
AD8646	24 MHz rail-to-rail dual op amp
AD2S1210	Variable resolution, 10-bit to 16-bit R/D converter with reference oscillator
Power	
ADuM5000	isoPower® integrated isolated dc-to-dc converter
ADP1614	1000 mA, 2.5 MHz buck-boost dc-to-dc converter
ADM660	CMOS switched-capacitor voltage converter
Isolation	
ADuM7640	Triple channel digital isolator
Voltage Translation	
ADG3308	8-channel bidirectional level translator
Multiplexers	
ADG704	CMOS, low voltage 2.5 Ω 4-channel multiplexer
ADG759	CMOS low voltage, 3 ohms 4-channel multiplexer
High Speed Communication	
88E1512	Marvell Integrated 10/100/1000 Mbps Energy Efficient Ethernet Transceiver

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Jumper settings



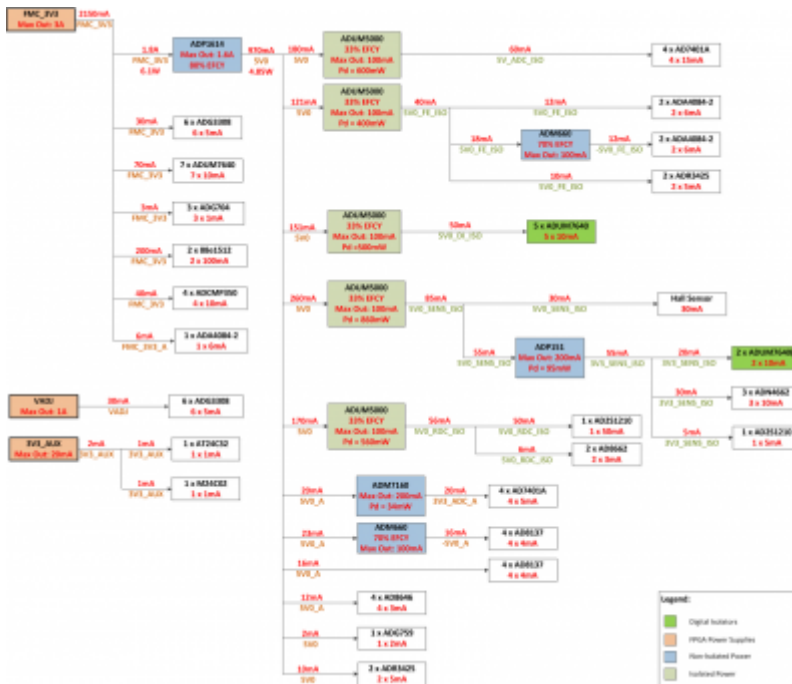
Sensor Selection		
Back EMF	P9 - position 0	P20 - position 0
Single ended Hall	P9 - position 1	P20 - position 0
Differential Hall	P9 - position 0	P20 - position 1
Reserved	P9 - position 1	P20 - position 1
Resolver Configuration Mode		
Normal Mode - Position input	P3 - Not inserted	P5 - Not inserted
Normal Mode - Velocity input	P3 - Not inserted	P5 - Inserted
Reserved	P3 - Inserted	P5 - Not inserted
Configuration Mode	P3 - Inserted	P5 - Inserted
Resolver Resolution Settings		
10 Bits	P4 - Not inserted	P6 - Not inserted
12 Bits	P4 - Not inserted	P6 - Inserted
14 Bits	P4 - Inserted	P6 - Not inserted
16 Bits	P4 - Inserted	P6 - Inserted
PHYs Configuration		
2.5V VDDO, different PHY addresses	P11 & P12 - Position 0	P9 - Inserted

LEDs

LED	Description
DS1	FMC 3.3V Power Good

DS2	Vadj Power Good
DS3	5V Power Good
DS7	12V Power Good

Power Map



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ADC FPGA Interface

The AD7401 Isolated Sigma-Delta Modulators present on the controller board have a 2 wires signal interface with the FPGA:



- 10 / 20 MHz clock input
- 1 bit digital data stream output

The reconstruction of the data provided by the AD7401 modulator can be done using a SINC3 filter. A filter model and HDL implementation are provided in the AD7401 datasheet. Typical filter output characteristics:

- Output code: 16 bit
- Sampling rate: 78kHz

The output code resolution and sampling rate can be controlled by changing the filter's model and decimation. Polyphase interpolation filters are utilized to increase the sampling rate of the system.

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Position & Speed Sensors FPGA Interface

Single digital interface for multiple position sensors

- Single Ended HALL
- Differential HALL
- BEMF
- Encoder

3 digital signals between HW and the FPGA

- HALL A / BEMF A / Encoder Channel A
- HALL B / BEMF B / Encoder Channel B
- HALL C / BEMF C / Encoder Index

Sensor selection is done with jumpers on the controller board. The hardware conditions the analog signals and sends clean digital signals to the FPGA.

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Downloads

AD-FMCMOTCON1-EBZ



- [Schematics](#)
- [Bill of Materials](#)
- [Allegro Board File](#) (This file is [compressed](#)). Get the [Allegro FREE Physical Viewer](#) (You need 16.5 or higher).

Navigation - AD-FMCMOTCON1-EBZ

Up: [Overview](#) Next.: [Low Voltage Drive Board](#)

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