



# NX6020CAKS

60 V / 50 V, 170 mA / 160 mA N/P-channel Trench MOSFET

18 January 2018

Product data sheet

## 1. General description

Complementary N/P-channel enhancement mode Field-Effect Transistor (FET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Trench MOSFET technology
- Very fast switching
- ElectroStatic Discharge (ESD) protection

## 3. Applications

- Relay driver
- High-speed line driver
- Level shifter
- Power supply converter

## 4. Quick reference data

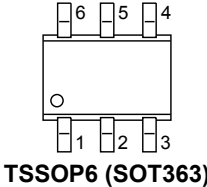
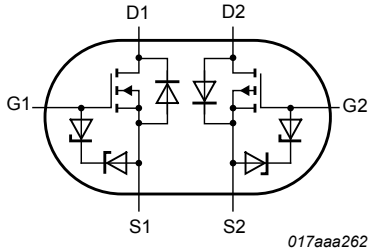
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>TR1 (N-channel)</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	60	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	170	mA
<b>TR1 (N-channel), Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 100\text{ mA}; T_j = 25\text{ °C}$	-	3	4.5	$\Omega$
<b>TR2 (P-channel)</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-50	V
$I_D$	drain current	$V_{GS} = -10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-160	mA
<b>TR2 (P-channel), Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}; I_D = -100\text{ mA}; T_j = 25\text{ °C}$	-	4.5	7.5	$\Omega$

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm<sup>2</sup>.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>TSSOP6 (SOT363)</p>	 <p>017aaa262</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NX6020CAKS	TSSOP6	plastic surface-mounted package; 6 leads	SOT363

## 7. Marking

Table 4. Marking codes

Type number	Marking code[1]
NX6020CAKS	2A%

[1] % = placeholder for manufacturing site code

## 8. Limiting values

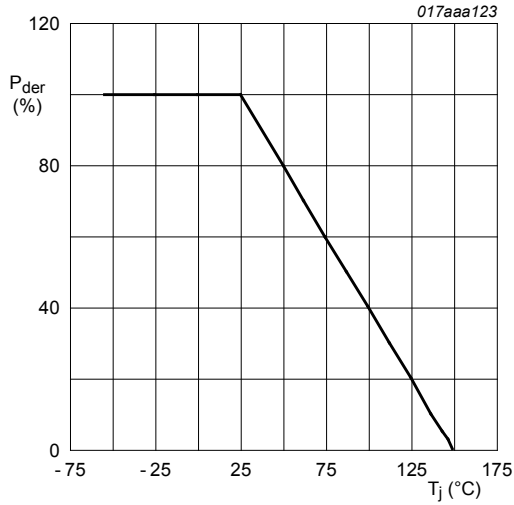
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
<b>TR1 (N-channel)</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$		-	60	V
$V_{GS}$	gate-source voltage			-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	170	mA
		$V_{GS} = 10\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	100	mA
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	680	mA
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	220	mW
			[1]	-	255	mW
		$T_{sp} = 25\text{ °C}$		-	1.06	W
<b>TR2 (P-channel)</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$		-	-50	V
$V_{GS}$	gate-source voltage			-20	20	V
$I_D$	drain current	$V_{GS} = -10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-160	mA
		$V_{GS} = -10\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	-100	mA
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	-640	mA
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	280	mW
			[1]	-	320	mW
		$T_{sp} = 25\text{ °C}$		-	990	mW
<b>Per device</b>						
$P_{tot}$	total power dissipation	$T_{amb} = 25\text{ °C}$	[2]	-	330	mW
$T_j$	junction temperature			-55	150	°C
$T_{amb}$	ambient temperature			-55	150	°C
$T_{stg}$	storage temperature			-65	150	°C
<b>TR1 (N-channel), Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25\text{ °C}$	[1]	-	170	mA
<b>TR2 (P-channel), Source-drain diode</b>						
$I_S$	source current	$T_{amb} = 25\text{ °C}$	[1]	-	-160	mA

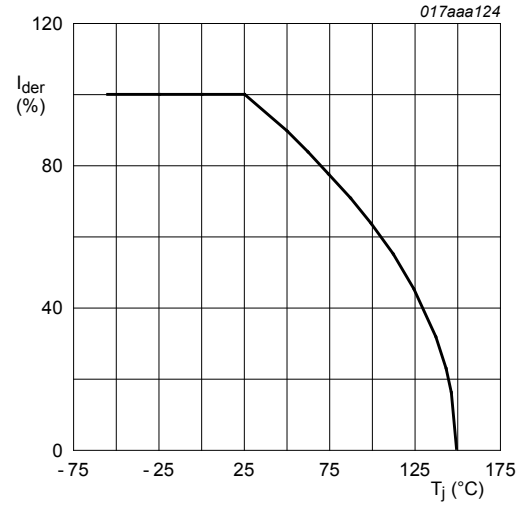
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm<sup>2</sup>.

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.



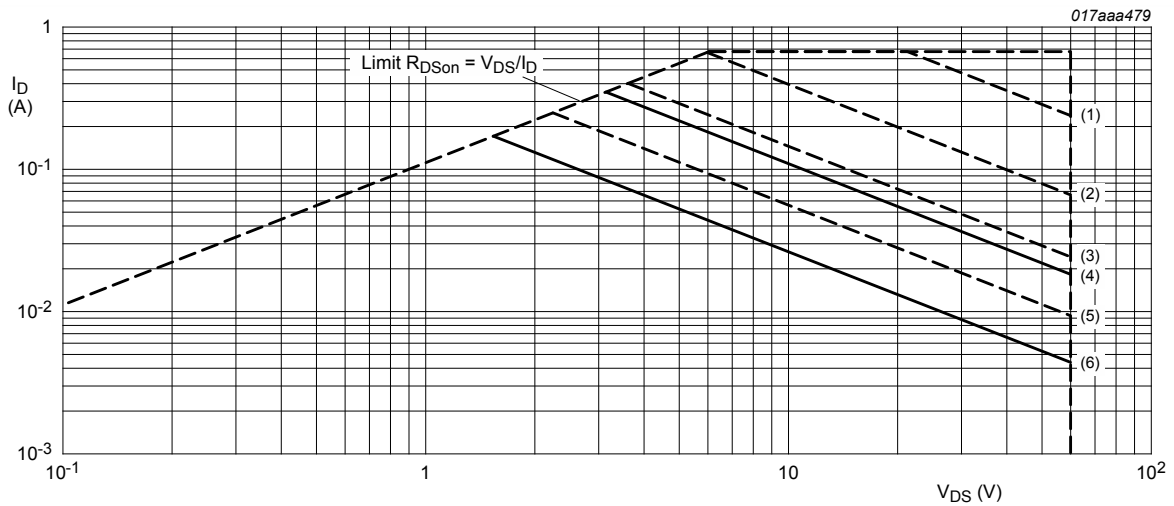
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

Fig. 1. Normalized total power dissipation as a function of junction temperature



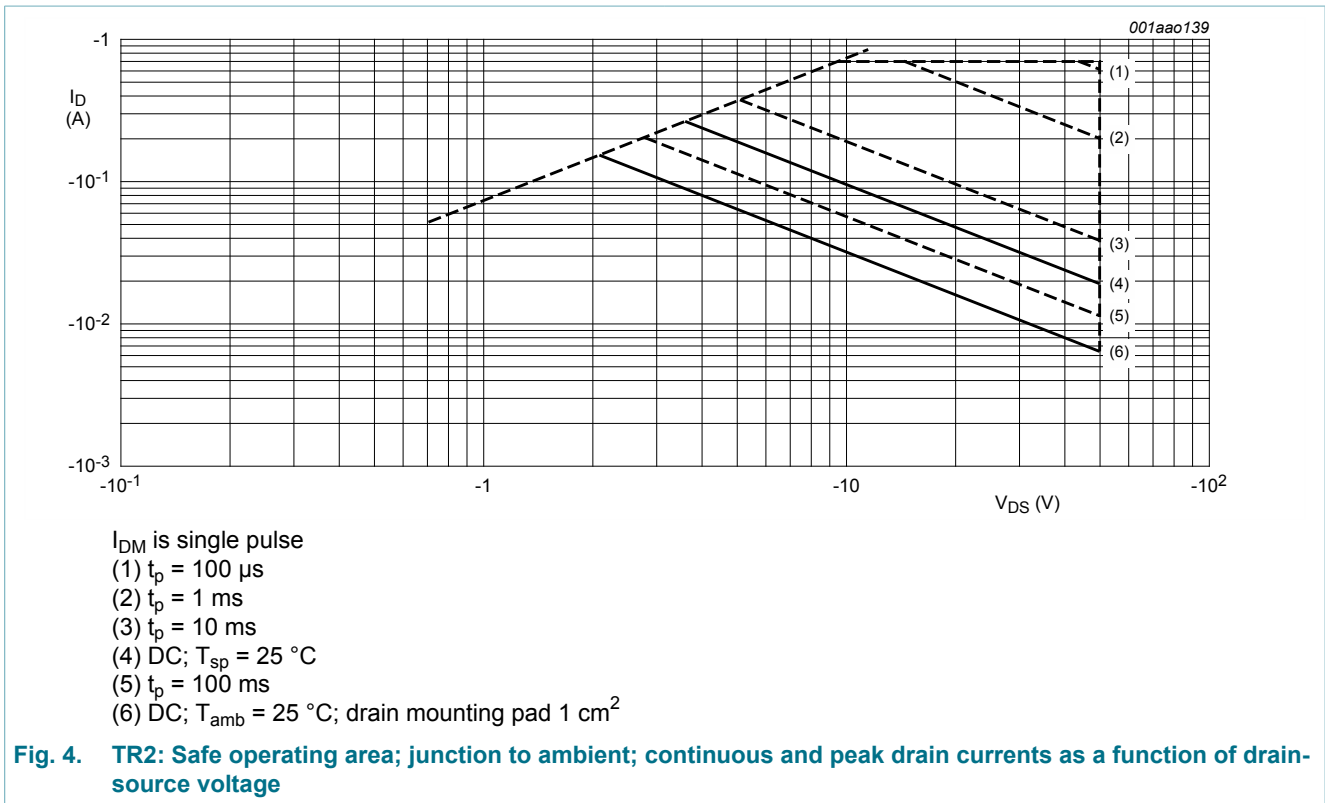
$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$

Fig. 2. Normalized continuous drain current as a function of junction temperature



- $I_{DM}$  = single pulse
- (1)  $t_p = 100 \mu s$
  - (2)  $t_p = 1 ms$
  - (3)  $t_p = 10 ms$
  - (4) DC;  $T_{sp} = 25^{\circ}C$
  - (5)  $t_p = 100 ms$
  - (6) DC;  $T_{amb} = 25^{\circ}C$ ; drain mounting pad  $1 cm^2$

Fig. 3. TR1: Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage



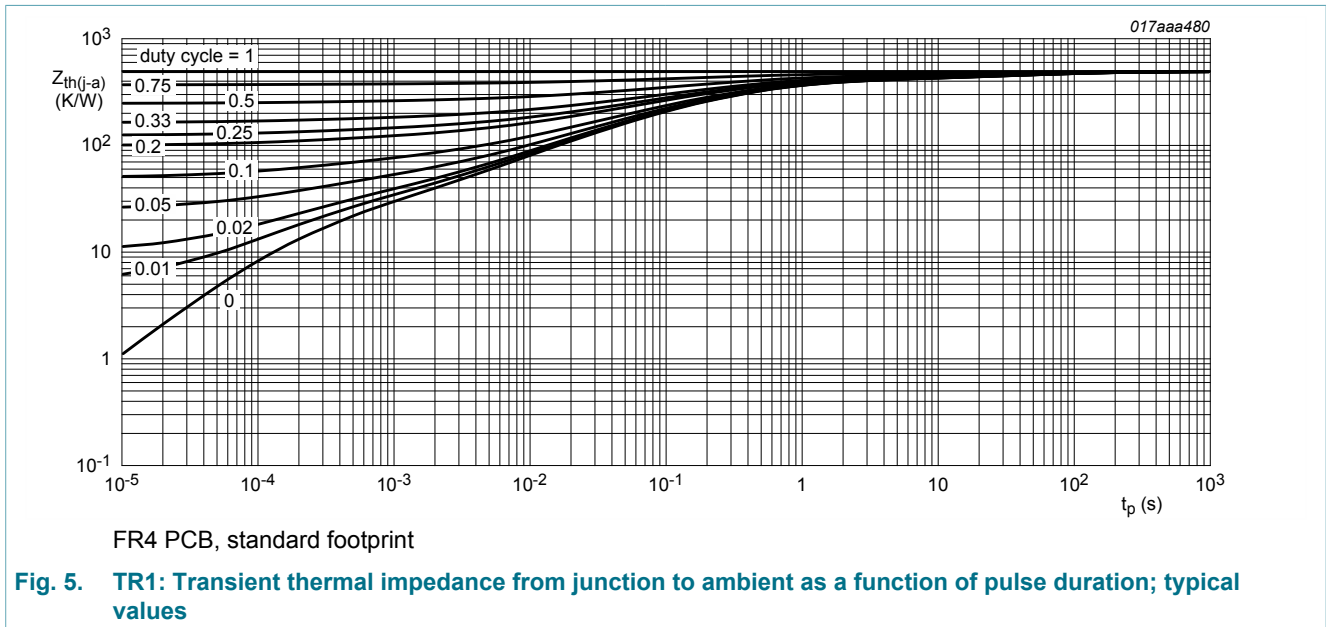
## 9. Thermal characteristics

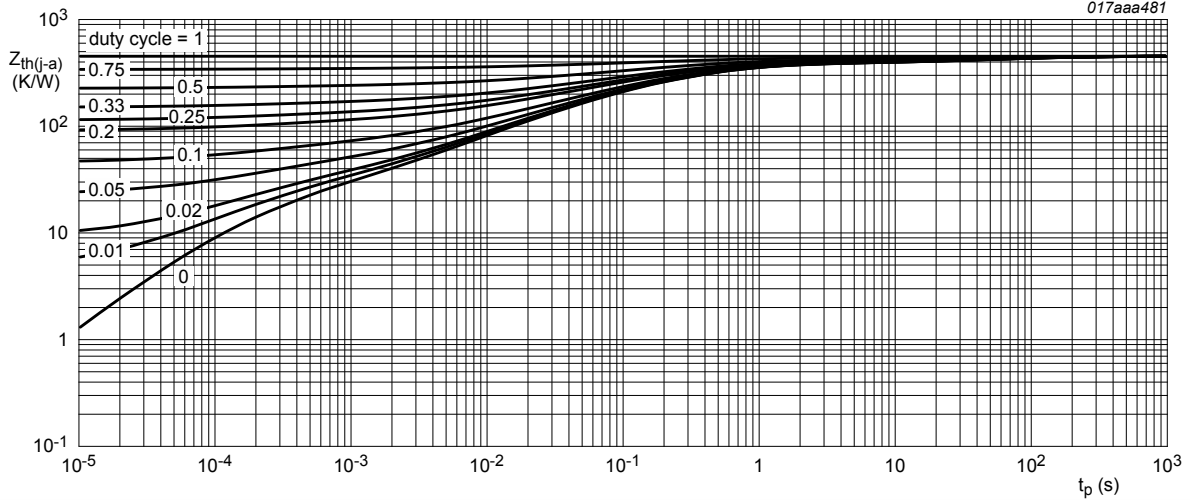
Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>TR1 (N-channel)</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	500	560	K/W
			[2]	-	450	480	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	115	K/W
<b>TR2 (P-channel)</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	390	445	K/W
			[2]	-	340	390	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	130	K/W
<b>Per device</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	300	K/W

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper; tin-plated and standard footprint.

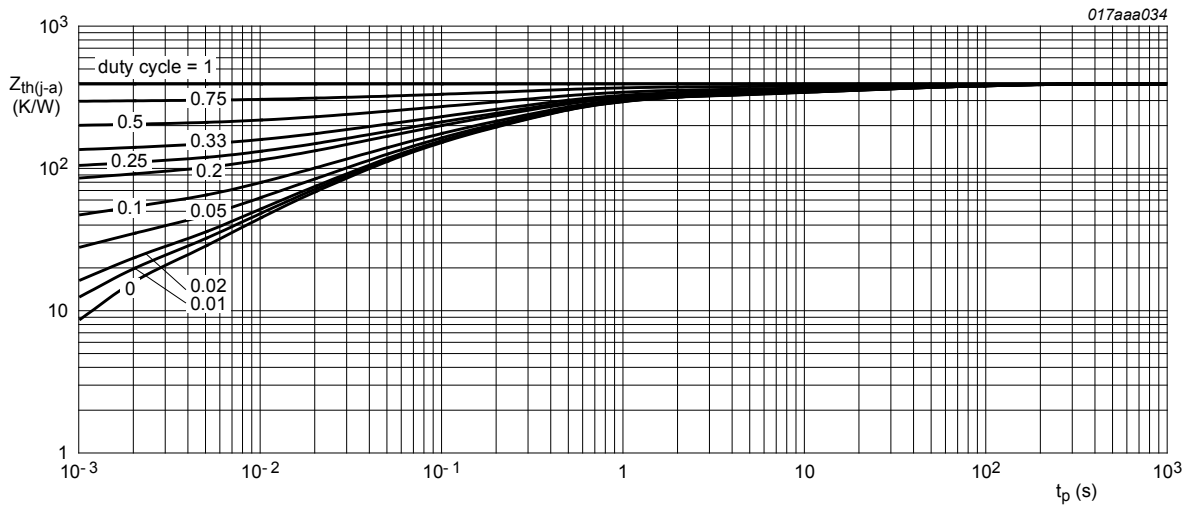
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm<sup>2</sup>.





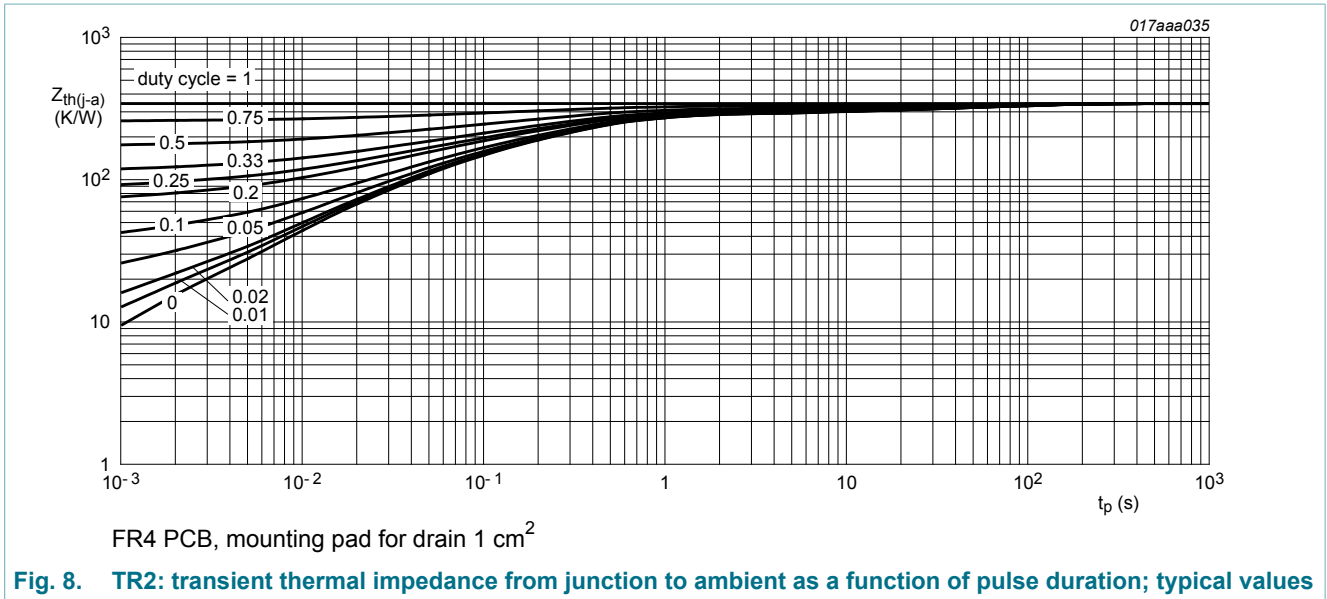
FR4 PCB, mounting pad for drain 1 cm<sup>2</sup>

Fig. 6. TR1: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, standard footprint

Fig. 7. TR2: transient thermal impedance from junction to ambient as a function of pulse duration; typical values





## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>TR1 (N-channel), Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$	1.1	1.6	2.1	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
		$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	10	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	2	$\mu A$
		$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	2	$\mu A$
		$V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	0.5	$\mu A$
		$V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	0.5	$\mu A$
		$V_{GS} = 5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 100 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	3	4.5	$\Omega$
		$V_{GS} = 10 V; I_D = 100 \text{ mA}; T_j = 150 \text{ }^\circ C$	-	6.2	9.2	$\Omega$
		$V_{GS} = 5 V; I_D = 100 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	3.7	5.2	$\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = 10 V; I_D = 200 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	230	-	mS
<b>TR2 (P-channel), Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -10 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-50	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$	-1.1	-1.6	-2.1	V
$I_{DSS}$	drain leakage current	$V_{DS} = -50 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	$\mu A$
		$V_{DS} = -50 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	-2	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-10	$\mu A$
		$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-10	$\mu A$
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10 V; I_D = -100 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	4.5	7.5	$\Omega$
		$V_{GS} = -10 V; I_D = -100 \text{ mA}; T_j = 150 \text{ }^\circ C$	-	8	13.5	$\Omega$
		$V_{GS} = -5 V; I_D = -100 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	5.7	8.5	$\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -10 V; I_D = -100 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	150	-	mS
<b>TR1 (N-channel), Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 30 V; I_D = 200 \text{ mA}; V_{GS} = 4.5 V; T_j = 25 \text{ }^\circ C$	-	0.33	0.43	nC
$Q_{GS}$	gate-source charge		-	0.12	-	nC
$Q_{GD}$	gate-drain charge		-	0.09	-	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{iss}$	input capacitance	$V_{DS} = 10\text{ V}; f = 1\text{ MHz}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	11	17	pF
$C_{oss}$	output capacitance		-	3.4	-	pF
$C_{rss}$	reverse transfer capacitance		-	1.4	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40\text{ V}; R_L = 250\text{ }\Omega; V_{GS} = 10\text{ V}; R_{G(ext)} = 6\text{ }\Omega; T_j = 25\text{ }^\circ\text{C}$	-	6	12	ns
$t_r$	rise time		-	7	-	ns
$t_{d(off)}$	turn-off delay time		-	20	40	ns
$t_f$	fall time		-	14	-	ns
<b>TR2 (P-channel), Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -25\text{ V}; I_D = -200\text{ mA}; V_{GS} = -5\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	0.26	0.35	nC
$Q_{GS}$	gate-source charge		-	0.12	-	nC
$Q_{GD}$	gate-drain charge		-	0.09	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -25\text{ V}; f = 1\text{ MHz}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	24	36	pF
$C_{oss}$	output capacitance		-	4.5	-	pF
$C_{rss}$	reverse transfer capacitance		-	1.3	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -30\text{ V}; R_L = 250\text{ }\Omega; V_{GS} = -10\text{ V}; R_{G(ext)} = 6\text{ }\Omega; T_j = 25\text{ }^\circ\text{C}$	-	13	26	ns
$t_r$	rise time		-	11	-	ns
$t_{d(off)}$	turn-off delay time		-	48	96	ns
$t_f$	fall time		-	25	-	ns
<b>TR1 (N-channel), Source-drain diode characteristics</b>						
$V_{SD}$	source-drain voltage	$I_S = 115\text{ mA}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	0.47	0.7	1.2	V
<b>TR2 (P-channel), Source-drain diode characteristics</b>						
$V_{SD}$	source-drain voltage	$I_S = -115\text{ mA}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-0.48	-0.85	-1.2	V

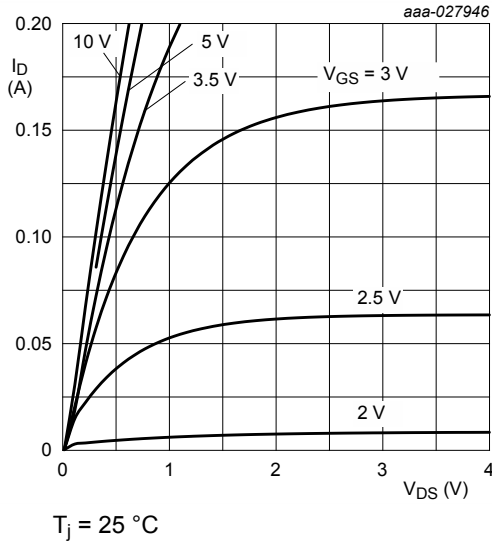


Fig. 9. TR1: Output characteristics: drain current as a function of drain-source voltage; typical values

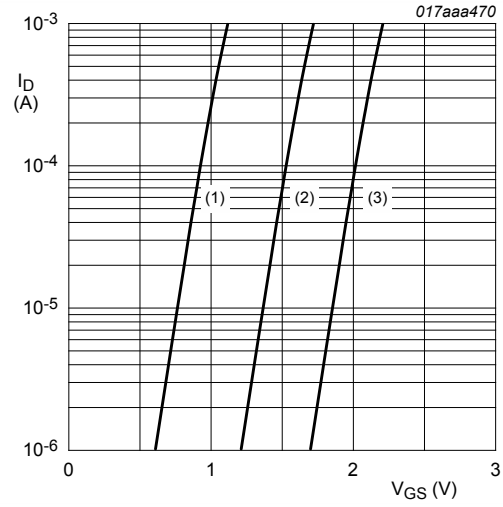


Fig. 10. TR1: Sub-threshold drain current as a function of gate-source voltage

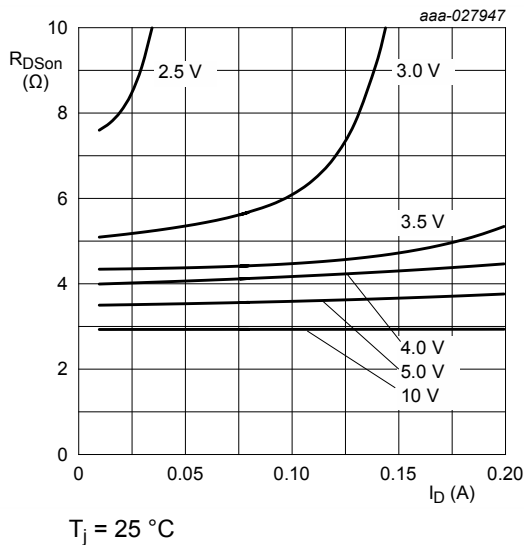


Fig. 11. TR1: Drain-source on-state resistance as a function of drain current; typical values

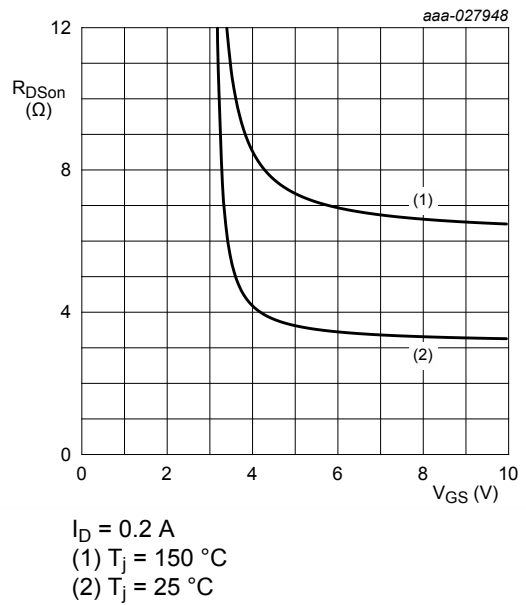
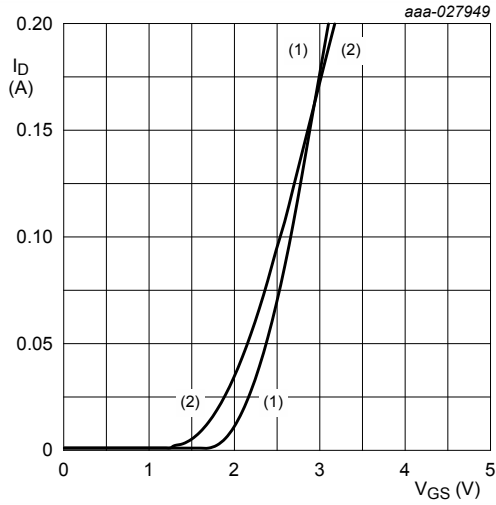
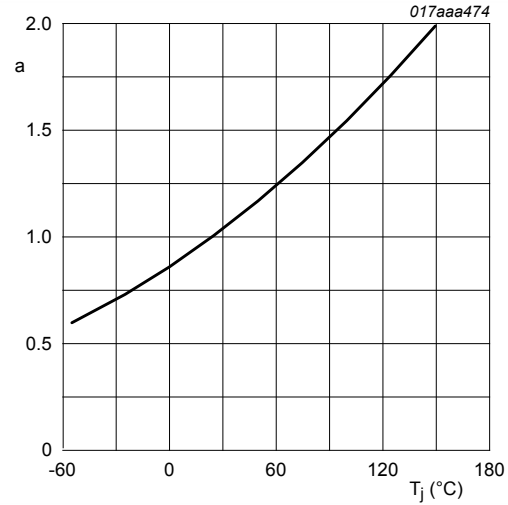


Fig. 12. TR1: Drain-source on-state resistance as a function of gate-source voltage; typical values



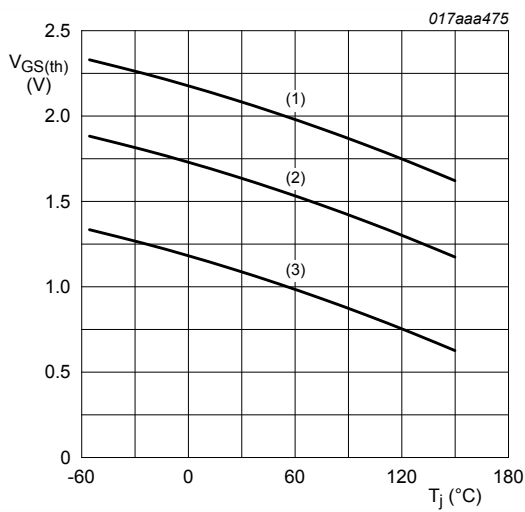
$V_{DS} > I_D \times R_{DSon}$   
 (1)  $T_j = 25\text{ °C}$   
 (2)  $T_j = 150\text{ °C}$

**Fig. 13. TR1: Transfer characteristics: drain current as a function of gate-source voltage; typical values**



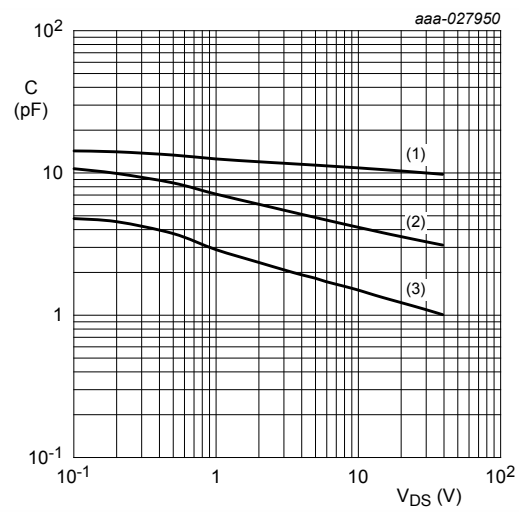
$$a = \frac{R_{DSon}}{R_{DSon(25\text{°C})}}$$

**Fig. 14. TR1: Normalized drain-source on-state resistance as a function of junction temperature; typical values**



$I_D = 0.25\text{ mA}; V_{DS} = V_{GS}$   
 (1) maximum values  
 (2) typical values  
 (3) minimum values

**Fig. 15. TR1: Gate-source threshold voltage as a function of junction temperature**



$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$   
 (1)  $C_{iss}$   
 (2)  $C_{oss}$   
 (3)  $C_{rss}$

**Fig. 16. TR1: Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

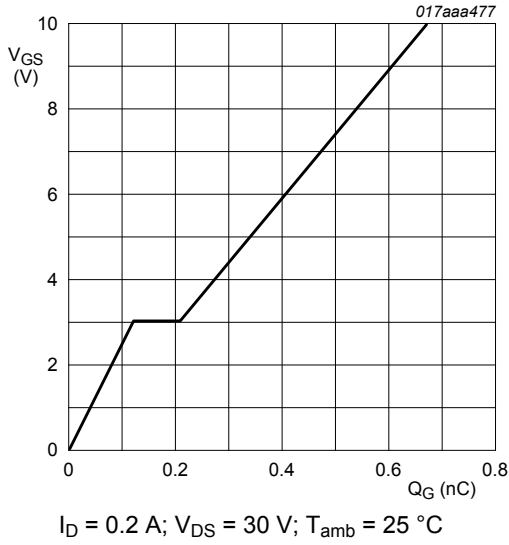


Fig. 17. TR1: Gate-source voltage as a function of gate charge; typical values

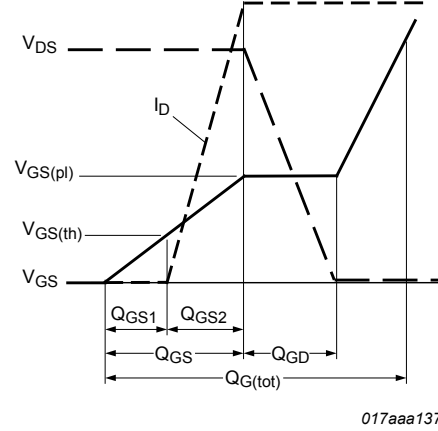
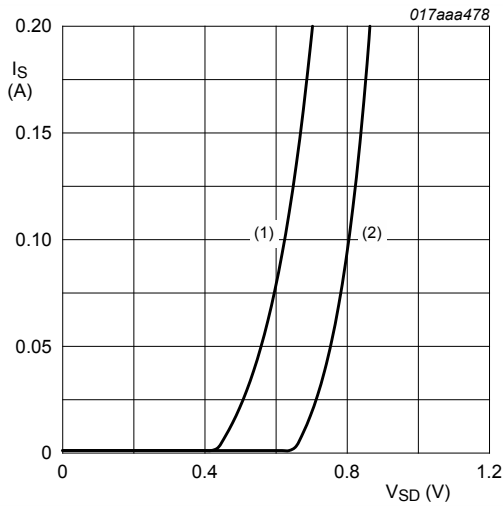


Fig. 18. TR1: Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$   
 (1)  $T_j = 150 \text{ }^\circ\text{C}$   
 (2)  $T_j = 25 \text{ }^\circ\text{C}$

Fig. 19. TR1: Source current as a function of source-drain voltage; typical values

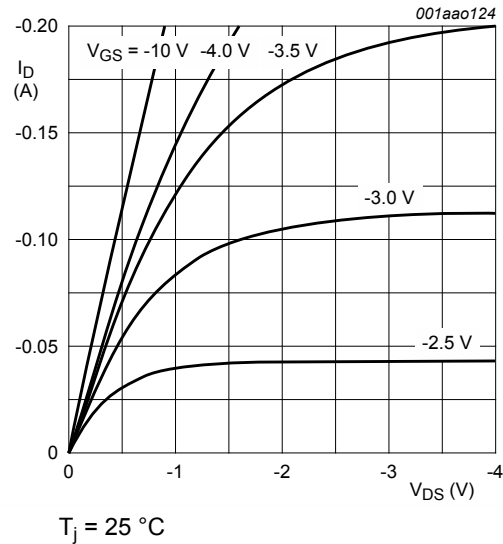
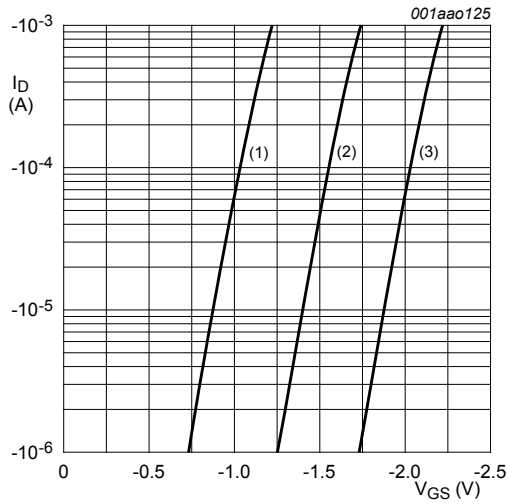
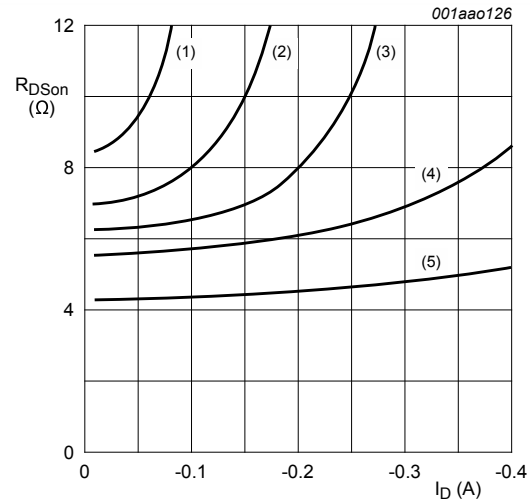


Fig. 20. TR2: Output characteristics: drain current as a function of drain-source voltage; typical values



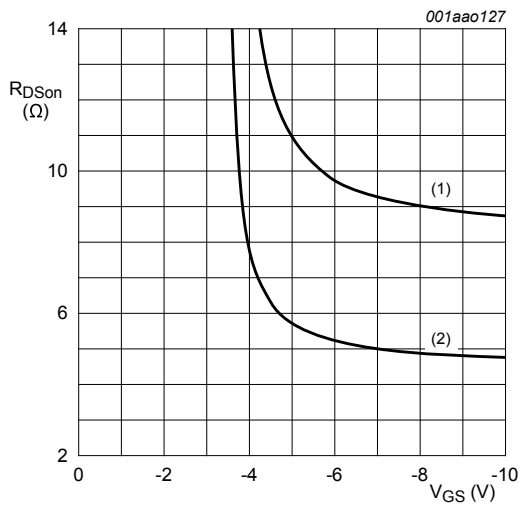
$T_j = 25\text{ }^\circ\text{C}$ ;  $V_{DS} = -5\text{ V}$   
 (1) minimum values  
 (2) typical values  
 (3) maximum values

**Fig. 21. TR2: Sub-threshold drain current as a function of gate-source voltage**



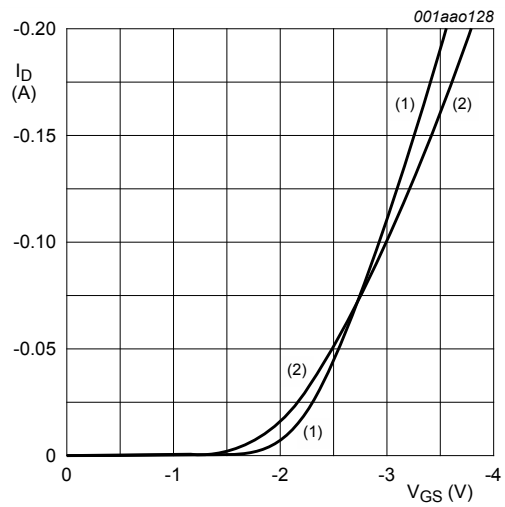
$T_j = 25\text{ }^\circ\text{C}$   
 (1)  $V_{GS} = -3.0\text{ V}$   
 (2)  $V_{GS} = -3.5\text{ V}$   
 (3)  $V_{GS} = -4.0\text{ V}$   
 (4)  $V_{GS} = -5.0\text{ V}$   
 (5)  $V_{GS} = -10.0\text{ V}$

**Fig. 22. TR2: Drain-source on-state resistance as a function of drain current; typical values**



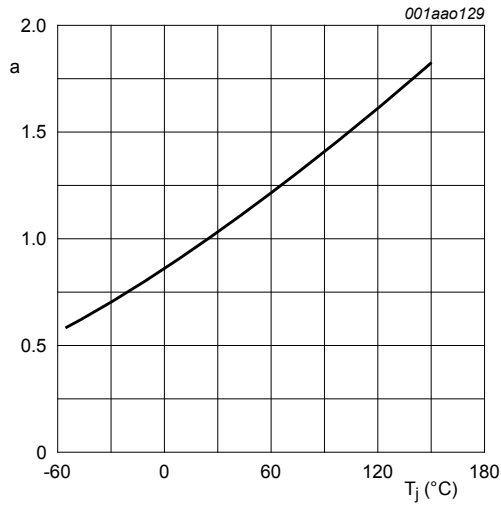
$I_D = -200\text{ mA}$   
 (1)  $T_j = 150\text{ }^\circ\text{C}$   
 (2)  $T_j = 25\text{ }^\circ\text{C}$

**Fig. 23. TR2: Drain-source on-state resistance as a function of gate-source voltage; typical values**



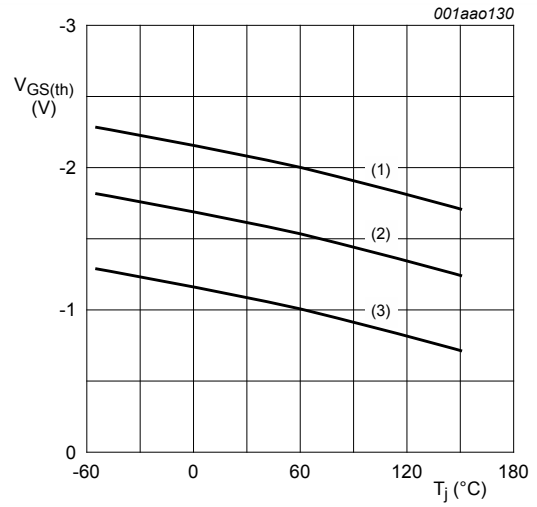
$V_{DS} > I_D \times R_{DSon}$   
 (1)  $T_j = 25\text{ }^\circ\text{C}$   
 (2)  $T_j = 150\text{ }^\circ\text{C}$

**Fig. 24. TR2: Transfer characteristics: drain current as a function of gate-source voltage; typical values**



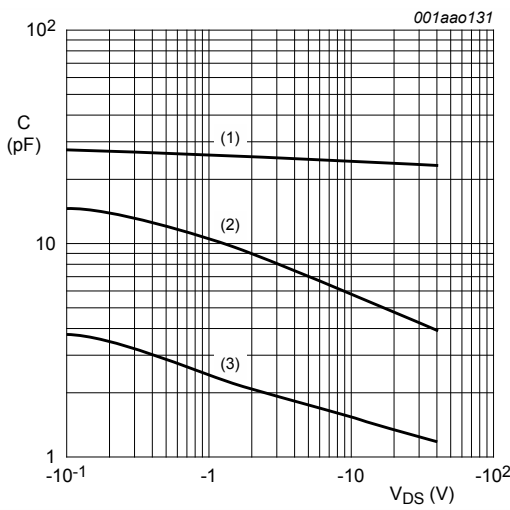
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

**Fig. 25. TR2: Normalized drain-source on-state resistance as a function of junction temperature; typical values**



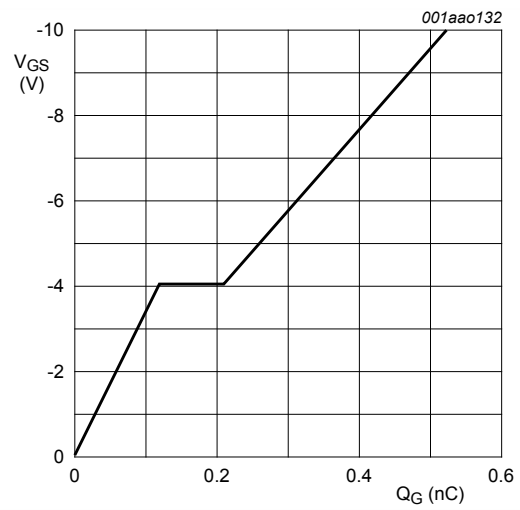
$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}$   
 (1) maximum values  
 (2) typical values  
 (3) minimum values

**Fig. 26. TR2: Gate-source threshold voltage as a function of junction temperature**



$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$   
 (1)  $C_{iss}$   
 (2)  $C_{oss}$   
 (3)  $C_{rss}$

**Fig. 27. TR2: Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$I_D = -200 \text{ mA}; V_{DS} = -25 \text{ V}; T_{amb} = 25 \text{ }^{\circ}\text{C}$

**Fig. 28. TR2: Gate-source voltage as a function of gate charge; typical values**

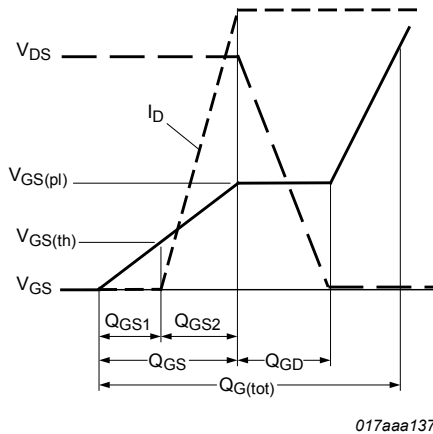
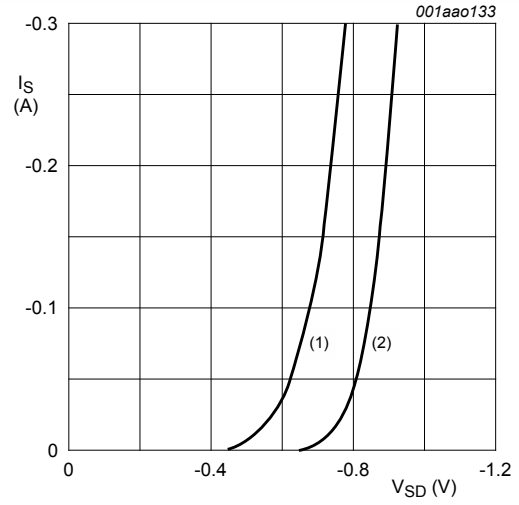


Fig. 29. TR2: Gate charge waveform definitions



$V_{GS} = 0 V$   
 (1)  $T_j = 150^\circ C$   
 (2)  $T_j = 25^\circ C$

Fig. 30. TR2: Source current as a function of source-drain voltage; typical values

## 11. Test information

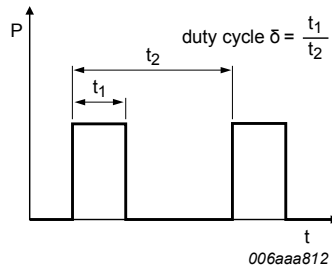


Fig. 31. Duty cycle definition



## 12. Package outline

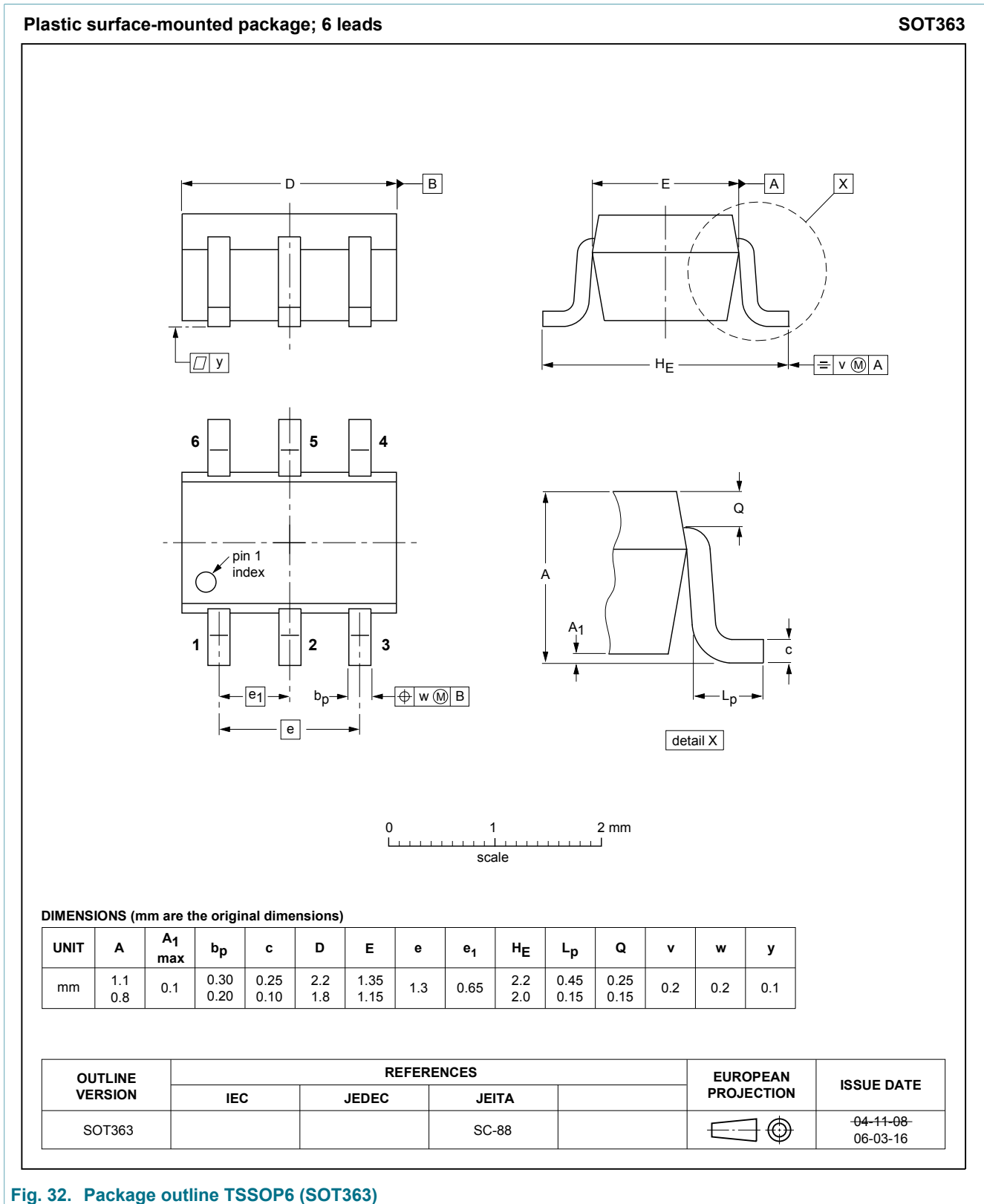


Fig. 32. Package outline TSSOP6 (SOT363)

### 13. Soldering

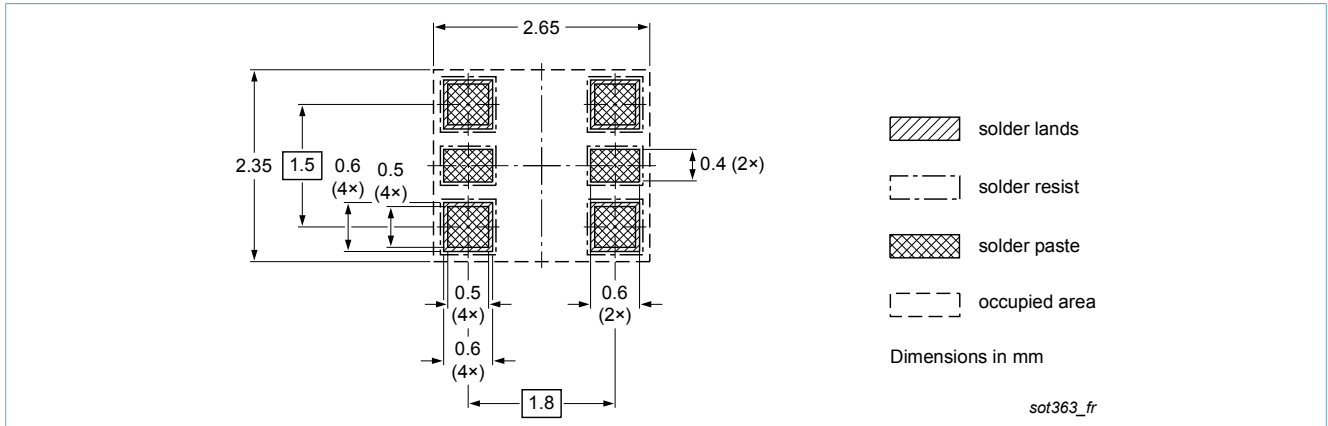


Fig. 33. Reflow soldering footprint for TSSOP6 (SOT363)

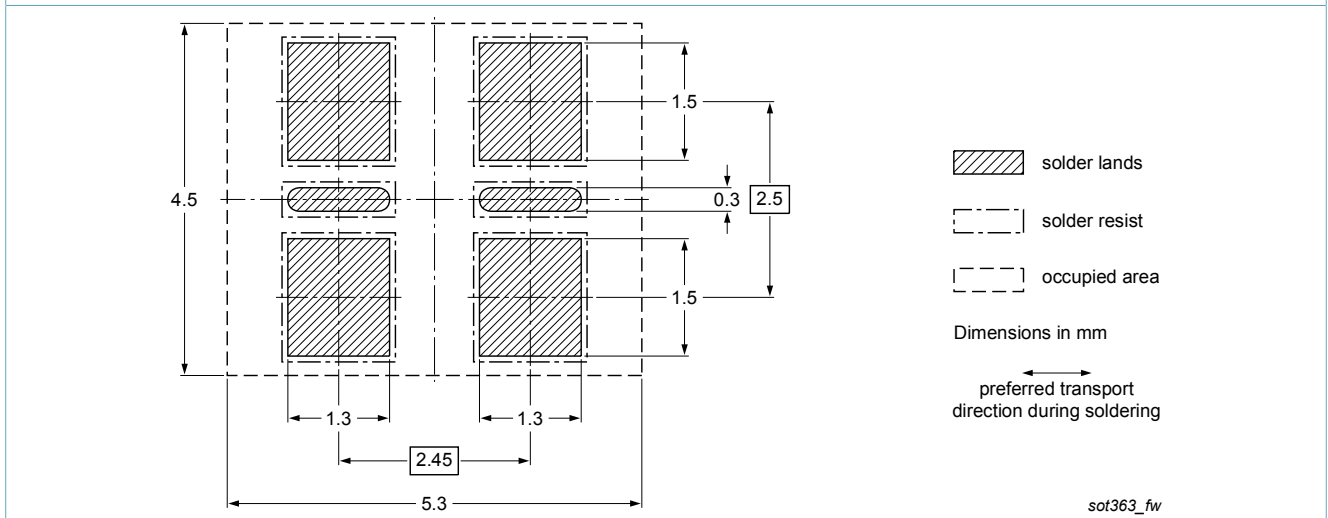


Fig. 34. Wave soldering footprint for TSSOP6 (SOT363)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NX6020CAKS v.2	20180118	Product data sheet	-	NX6020CAKS v.1
Modifications:	<ul style="list-style-type: none"><li>• Data sheet status changed to Product.</li><li>• Section: Limiting values, ESD maximum rating removed.</li></ul>			
NX6020CAKS v.1	20171220	Preliminary data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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