AKM

AP1651BEL
Dimmable LED driver IC for Lighting

1. Genaral Description

The AP1651BEL (hereinafter referred to as the AP1651) is a current mode non-isolated low side buck converter controller IC designed to support an LED general lighting application as a second stage (e.g. after PFC stage). This IC provides "constant ripple control ", featuring the constant peak and bottom current of the inductor which is sensed through low side sense resistors. This control scheme does not depend on either the varying input voltage or the varying forward voltage of the LEDs, allowing the LED current to be obtained with high stability.

The AP1651 supports two types of dimming; PWM dimming by pulse input and complex dimming by DC input. Deep dimming down to 1% is achievable by using DC dimming. In addition, the DC dimming has an even deeper dimming function by using an internal linear regulator for the LEDs. This "ultra-dimming" which is supported from 500μA to 100μA is able to provide a new night light application.

This IC provides several protection function; over current protection, UVLO, and thermal shutdown for the IC chip.

2. Features

- Low-side Switching Step-down Converter
- Current mode
    - Continuous Conduction Mode (CCM)
    - Linear Regulator Mode (Automatic Mode Selection)
- Operating Voltage Range   VDD = 11V to 26V
- Operating Temperature   Ta = - 40 to 105 °C
- Dimming function
    - External DC input (Complex Dimming 100% to 1% and Ultra-low current to 0%)
    - Voltage Input of External Pulse (Dimming by PWM)
- Protection function:
    - Over Current Protection for External N-channel Power MOSFET
    - Under Voltage Lockout Function (UVLO)
    - CS pin Open Protection
    - Thermal Shutdown (TSD)
- Package   14-pin SOP

AKM Simulator

http://akm.transim.com/

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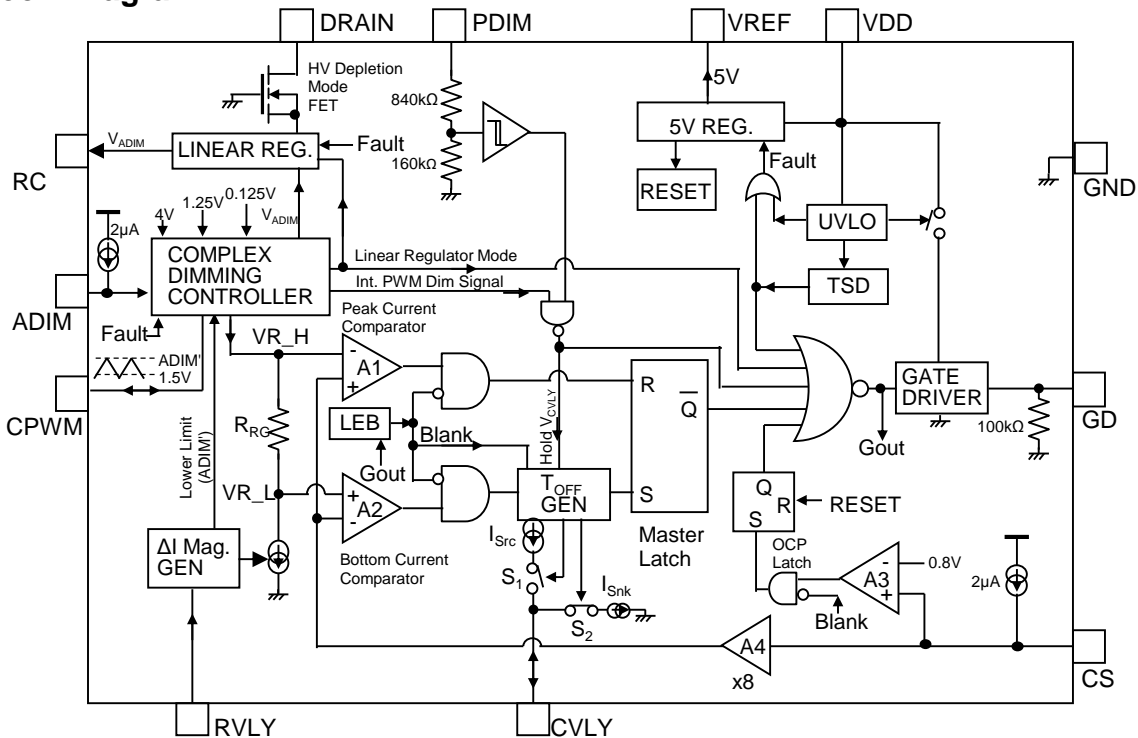
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■ Block Diagram

Figure 1. Block Diagram

■ Functions

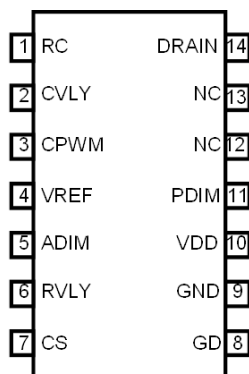| BLOCK Name	Description
5V REG	This block generates a 5V voltage from the VDD pin voltage and outputs to the internal 5V logic circuit and the VREF pin.
UVLO	By monitoring the VDD pin voltage, driver output is held to GND level and 5V regulator is inactivated so that malfunction at low voltage is prevented.
RESET	Circuit for Power On Reset when UVLO is released.
GATE DRIVER	Level sifter and Driver for external N-channel power MOSFET.
COMPREX DIMMING CONTROLLER	Control Circuit for Complex Dimming, Full and No LED current outputs This circuit generates a mode-select-signal and a dim level from the ADIM input voltage. It also generates a PWM dimming signal which is generated by comparing the ADIM pin voltage and a triangle wave that is determined by ΔI Mag GEN output voltage.
T_{OFF} GEN	This circuit generates the OFF time by turning ON/OFF the current source (I_{Src}) which charges an external capacitor between the CVLY pin and the GND. Input signals are LEB and Bottom current comparator (A2). When the PWM dimming signal is low, both current for charging and outputting (I_{Src}, $I_{Snk.}$) are stopped.
ΔI Mag. GEN	This circuit generates a Bottom Control voltage (VRL) from the hysteresis level setting by RVLY pin voltage. It also outputs lower limit level of the peak current control (ADIM') to the internal complex dimming controller.
LINEAR REG.	A regulator circuit that controls the HV Depletion Mode FET to be equal the RC pin voltage and the ADIM pin voltage at the linear regulator mode.
TSD	Overheat detection circuit.
LEB	Output Leading edge blanking logic signal from the GATE DRIVER output.

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5. Ordering Guide

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AP1651BEL   Ta = -40〜105°C   14-pin SOP

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6. Pin Configurations and Functions

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■ **Pin Configurations**

1	RC	DRAIN 14
2	CVLY	NC 13
3	CPWM	NC 12
4	VREF	PDIM 11
5	ADIM	VDD 10
6	RVLY	GND 9
7	CS	GD 8

■ **Functions**

No.	Name	I/O	Function
1	RC	O	Output pin for Internal High Voltage linear Regulator A 500µA LED current is output when $V_{ADIM} = 1V$ by connecting an external current sensing resistor (2kΩ±1%) between this pin and the GND. This resistor should be more than 500Ω.
2	CVLY	O	External Capacitor Pin for Internal Block (T_{off} GEN Block) Connect an external 0.01µF ceramic capacitor between this pin and the GND.
3	CPWM	O	External Capacitor for Internal PWM generator (Peak+PWM state of Complex Dimming Controller). Connect an external 0.01µF ceramic capacitor between this pin and the GND.
4	VREF	O	Internal Regulator Output Pin Connect a 10µF capacitor between this pin and the GND.
5	ADIM	I	DC Dimming (Complex dimming) Signal Input Pin Control LED current depending on the input voltage ranged 4 to 0.2V, and stops the LED current under the condition that the input voltage is less than 0.05V.
6	RVLY	I	Hysteresis Width Setting Pin for Inductor The Hysteresis Width is determined by the input voltage to this pin and a resistor connected between the CS pin and the GND.
7	CS	I	Inductor Current Detection Pin An Inductor peak current is set by connecting a resistor between this pin and the GND. It also detects an over current and the bottom current of the inductor. This pin is pulled up by a 2µA (typ) internally.
8	GD	O	Gate Drive Output Pin for External N-channel Power MOSFET This pin is pulled down by a 100kΩ (typ) resistor internally.
9	GND	PWR	Ground Pin
10	VDD	PWR	Power Supply Pin
11	PDIM	I	PWM Dimming Signal Input Pin. LEDs can be dimmed by inputting pulse voltage to this pin repeatedly. The output driver is turned off when the GND voltage is input to this pin. This pin is pulled down by a 2MΩ (typ) resistor internally.
12 13	NC	-	No Connection Pin This pin must not connect to anywhere.
14	DRAIN	I	Linear Current Regulator Input Pin. Drain pin of the internal high voltage MOSFET for linear regulator. Connect this pin to the cathode of an LED string through a current limit resistor.

7.   Absolute Maximum Ratings

Parameter	Symbol	min	max	Unit
VDD (Note 1)	V_{DDMAX}	-0.3	30	V
GD (Note 1, Note 2)	V_{OUTMAX}	-0.3	V_{DDMAX} +0.3 or 30	V
VREF (Note 1)	V_{REFMAX}	-0.3	6.0	V
RC, CPWM, CVLY, RVLY, PDIM, ADIM, CS (Note 1, Note 3)	-	-0.3	V_{REFMAX} +0.3 or 6.0	V
DRAIN (Note 1)	$V_{DRAINMAX}$	-0.3	450	V
Power Dissipation (Note 4, Note 5, Note 6)	P_D	-	1000	mW
Junction Temperature	T_j	-40	125	°C
Storage Temperature	T_{STG}	-55	150	°C

Note 1. All voltages refer to the GND pin (GND) as zero (reference) voltage.
Note 2. If V_{DDMAX} exceeds 29.7V, the maximum value is limited to 30V.
Note 3. If V_{REFMAX} exceeds 5.7V, the maximum value is limited to 6V.
Note 4. This value is decreased by 10mW/°C in the condition that the temperature is over 25°C.
Note 5. 100 mm × 100 mm, t=1.0mm CEM Single-sided Board.
Note 6. Thermal design should be designed in consideration with the calorific value of the internal regulator as well as power supplies.
   DC-DC mode (ADIM terminal voltage>1.4V):
     IC Power Dissipation =
      $V_{DD} \times$ IC Consumption electric current 5.5mA + VREF Output [($V_{DD} - V_{REF}$) $\times$ ($-I_{VREF}$)]
   Linear regulator mode (1.1V>ADIM terminal voltage>0.05V):
     IC power Dissipation =
      Internal linear regulator electric power consumption [($V_{DRAIN} - V_{ADIM}$) ×(V_{ADIM} / RC resistor with the outside R2)] + $V_{DD} \times$ IC Consumption electric current 2.0mA + VREF Output[($V_{DD} - V_{REF}$) $\times$ ($-I_{VREF}$)]

WARNING: The maximum ratings are the absolute limitation values with the possibility of damaging the IC. When operation exceeds these limits, the specifications cannot be guaranteed.

8.   Recommended Operating Conditions

Parameter	Symbol	min	typ	max	Unit
Operating Voltage Range (Note 7)	V_{DD}	11	-	26	V
DRAIN (Note 7)	V_{DRAIN}		-	400	V
RC, CPWM, CVLY, RVLY, PDIM, ADIM, CS (Note 7)	-	GND	-	V_{REF}	V
RVLY Pin Voltage (Note 7)	V_{RVLY}	1.8	-	4.0	V
PDIM Pin Voltage(Note 7)	V_{PDIM}	GND	-	V_{REF}	V
VREF Pin Voltage	I_{VREF}		-	-5	mA
Operating Temperature (Note 8)	Ta	-40	-	105	°C

Note 7. All voltages refer to GND pin (GND) as zero (reference) voltage.
Note 8. In applications that have high power dissipation and/or low thermal conductivity, the maximum value of Ta must be lowered not to exceed the maximum junction temperature.

9. Electrical Characteristics

(Ta=25°C, V_{DD}=15V, GND=0V, R_2=2kΩ(RC), C_3=0.01μF (CPWM),C_4=0.01μF (CVLY), V_{RVLY}=3.25V, V_{PDIM}= V_{ADIM}= $V_{REF,}$ unless otherwise specified. Each current is defined as positive when it is input to the pin, and defined as negative when it is output from the pin.) *Refer to Figure 16 for external devices.

1. Power Consumption

Parameter	Symbol	min	typ	max	Unit	Condition
Power Consumption	I_{DD1}	-	3.0	5.5	mA	V_{CS}=0.6V,V_{CVLY}=2V, GD-GND=1000pF
	I_{DD2}	-	1.4	2.0	mA	PDIM=0V

2. Control

Parameter	Symbol	min	typ	max	Unit	Condition
Power Supply Voltage (VDD)						
UVLO Detect Voltage1	V_{UVH}	9.5	10	10.5	V	V_{DD} voltage rising
UVLO Detect Voltage2	V_{UVL}	8.0	8.5	9.0	V	V_{DD} voltage falling
UVLO Hysteresis	V_{UVHYS}	0.5	1.5	2.5	V	
Internal Regulator (VREF)						
VREF Voltage	V_{REF}	4.8	5.0	5.2	V	I_{VREF}=0mA
VREF Dropout Voltage	V_{DROP}	-	20	100	mV	I_{VREF}=-5mA
Mode Select (ADIM)						
Step down DC-DC Converter Mode	V_{ADIM}	1.4	-	-	V	
Linear Regulator Mode	V_{ADIM}	-	-	1.1	V	
Output is stopped.	V_{ADIM}	-	-	0.05	V	
Full Output	V_{ADIM}	4.5	-	-	V	ADIM dimmer OFF: 100% output
ADIM pin Pull-up Current	I_{ADIM}	1.6	2.0	2.4	μA	
DC-DC Converter Mode						
Peak Sense Voltage(CS)	V_{SEN}	0.47	0.5	0.53	V	V_{ADIM}=V_{REF}
Leading Edge Blanking Time	T_{LEB}	220	350	430	ns	CS=0.6V
CVLY Charge/Discharge Ratio	CD_R	67	100	133	-	I_{Src}/I_{Snk}
Maximum off time	T_{OFFMax}	-	40	48	μs	V_{CVLY}=GND
Internal PWM Dimming Frequency	F_{PWM}	0.75	1.0	1.25	kHz	C_3=0.01μF(CPWM-GND)
Minimum Duty of the Internal PWM Dimming	D_{MIN}	28	5.0	7.5	%	V_{ADIM}=1.5V
Linear Regulator Mode						
DRAIN Current	I_{DRAIN1}	470	500	530	μA	V_{ADIM}=1.0V,V_{DRAIN}=400V
	I_{DRAIN2}	94	100	106	μA	V_{ADIM}=0.2V,V_{DRAIN}=400V
DRAIN Off Leak	$I_{DRAINOFF}$	-	-	1	μA	V_{ADIM}=0V,V_{DRAIN}=400V
PWM Dimming (PDIM)						
PDIM Threshold Voltage	V_{PDIM1}	-	-	0.5	V	Disable
	V_{PDIM2}	1.5	-	-	V	Enable
PDIM Pull Down	R_{GD}	0.4	1.0	2.0	MΩ	
Gate Driver						
GD Pull Down	R_{GD}	40	100	200	kΩ	
Rise Time	T_r	10	50	140	ns	GD connected 1000pF
Fall Time	T_f	10	40	140	ns	GD connected 1000pF

3. Protection

Parameter	Symbol	min	typ	max	Unit	Condition
CS pin Over Current	OCP	0.72	0.8	0.88	V	Latch off
CS pin Pull-up Current	I_{CS}	1.8	2.0	2.2	µA	V_{CS}=GND
Thermal Shutdown	T_{TSD}	130	150	-	°C	When the temperature rises (Note 9)
TSD Hysteresis	T_{TSDHYS}	-	55	-	°C	When the temperature falls after thermal shutdown (Note 9)

Note 9. These values are design values.

10. Functional Descriptions

■ Operation

The AP1651 integrates an N-channel power MOSFET controller for a current control type non-isolated buck converter circuit and a high voltage linear regulator, which are suitable for driving LEDs in a series connection. "Step-down DC-DC coveter mode" (hereinafter DC-DC mode) or "linear regulator mode" can be selected by an external DC voltage. This DC voltage can also control LED dimming in addition to mode selecting, so that a complex dimming that changes operation mode automatically while adjusting the LED output level from the maximum to the minimum is realized.

The average current of an inductor is equal to that of LEDs on a non-isolated buck converter because the inductor is directly connected to LEDs during the entire switching cycle. Therefore, if the inductor average current is controlled to be constant, the LEDs average current also keeps constant. A hysteresis control mode is a one of control method that keeps the average current of the inductor constant. A stable current characteristic, that has a tolerance to changes of input/output conditions, is provided by this hysteresis control by directly controlling the peak current of the inductor and the difference between the bottom current and peak current (hysteresis width).

The AP1651 adopts a constant ripple current control method of the inductor current, which supplies a constant current in continuous conduction mode (CCM). With this method, the average current on the LEDs connected in series can be kept constant in spite of the possible system variations caused by following reasons:
    1) Input voltage change
    2) Change in the number of LEDs connected in series
    3) Variation in LED forward voltages (VF) of the LEDs
    4) Change in LED forward voltages caused by temperature variation.
    5) Inductor value variation
In order to obtain the constant ripple current control, the peak current and hysteresis width need to be determined properly, and then the coil inductance value should be determined by input/output voltage conditions and a switching frequency range. Off time is set by hysteresis width control automatically. In addition, a stable operation can be achieved without loop compensation even when the switching duty exceeds 50%, providing a simplified circuit design with the AP1651.

Dimming by the ADIM pin controls the LED current automatically from 100% to 1% and also from 500uA to 100uA by changing 3 modes which are called "peak current control mode", "peak current control with PWM dimming mode" and "linear regulator mode". These modes can be switched by the ADIM pin voltage.

"Peak current control mode": The average current is controlled by changing peak current under constant ripple control. Since the constant ripple control needs to detect the peak and bottom current of the inductor, the peak current cannot be less than the ripple amplitude (the average current should be more than 1/2 of the ripple amplitude). The AP1651 automatically sets the lower limit of the peak current control, and if the current goes down below, it operates in "peak current control with PWM dimming mode".

"Peak current control with PWM dimming mode": The average current is controlled by using both peak current control and internal PWM method under the constant ripple control.

These 2 modes described above can control the average current seamlessly from 100% to 1%.

"Linear regulator mode": When the ADIM pin voltage is at V_{ADIM2}(0.2 to 1.0V), AP1651 stops the switching operation of the external N-channel power MOSFET and the LED current is controlled by the DRAIN pin using the internal constant current source. This mode is suitable for tiny current applications such as a night light.

AP1651 also supports the PWM dimming. When the ADIM pin voltage is higher than the peak current control mode, the LED average current is controlled by the external N channel power MOSFET intermittent switching operation which is synchronizing with the pulse input from the PDIM pin.

■ DC-DC Mode

Figure 2 shows current paths of a buck converter and voltage and current waveforms of each node.
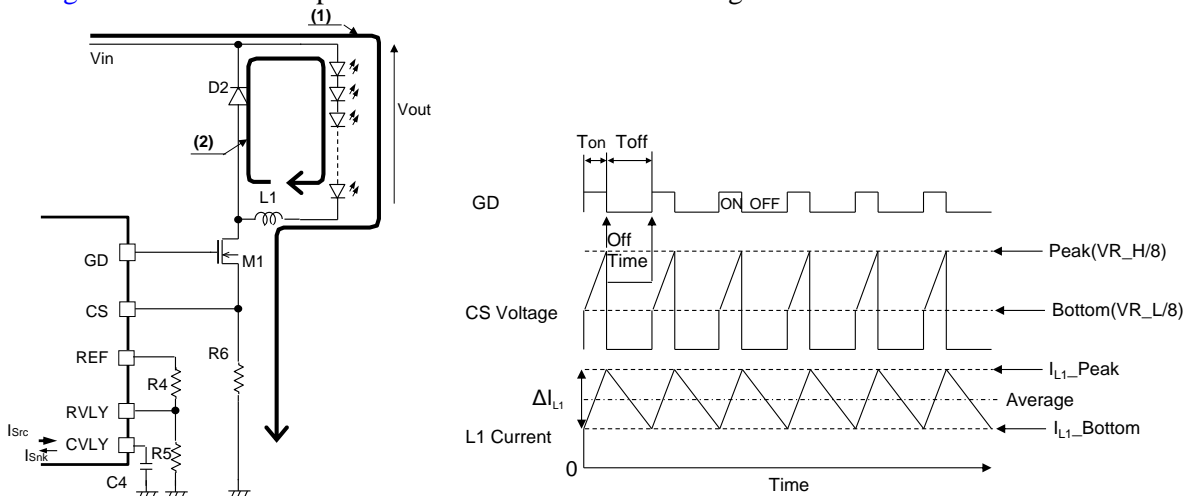

Figure 2. Operation Images of Buck Converter

The current of inductor L1 is controlled by turning ON and OFF the external N-channel power MOSFET (M1) with the GD pin output. The current path when the GD pin turns ON is shown as (1) and OFF is shown as (2) in Figure 2.

When the coil (L_1) current reaches the peak current (L_{1peak}) while the GD pin is ON, the A1 comparator which is internally connected to the CS pin is inverted and the GD pin is switched OFF. The GD pin is switched ON automatically when the OFF time which is determined by the CVLY voltage is passed. The bottom current is detected by the A2 comparator connected to the CS pin and the AP1651 controls the OFF time to keep the target value (VRL/8) by charging/discharging the CVLY pin.

Relationship of the CVLY pin voltage and the OFF time can be described approximately as follows

$$T_{OFF,Typ}[\mu s] = -16.842 \times V_{CVLY}[V] + 42.105 \quad ....(1)$$

where the range of V_{CVLY} is 0.125V $\leq$ VCVLY $\leq$ 2.35V.

The CVLY pin is connected to an internal current source (I_{Src}) and current sink (I_{Snk}). The CVLY pin charges a capacitor (C_4), which is connected to the CVLY pin, during the time from a falling edge of T_{LEB} until the A2 comparator output is inverted. This pin is discharging the capacitor in any other time.

The balance of this charge and discharge of the capacitor between the CVLY pin and the GND controls the CVLY voltage (off-time) to be optimal for the output voltage, and the desired hysteresis width can be obtained.

Figure 3 shows a waveform of the CS pin voltage and the CVLY pin voltage when the bottom current of the inductor is lower than the setting value.

In this case, the OFF time needs to be shortened. After the GD pin turns ON, the capacitor (C4) connected to the CVLY pin is charged until the CS pin voltage reaches VRL/8. This charge causes the CVLY pin voltage to be increased, and the OFF time becomes shorter gradually. When the CS pin voltage is equal to VRL/8 with the GD pin is ON, the charge and discharge currents on the CVLY pin are evenly balanced which means stable state.
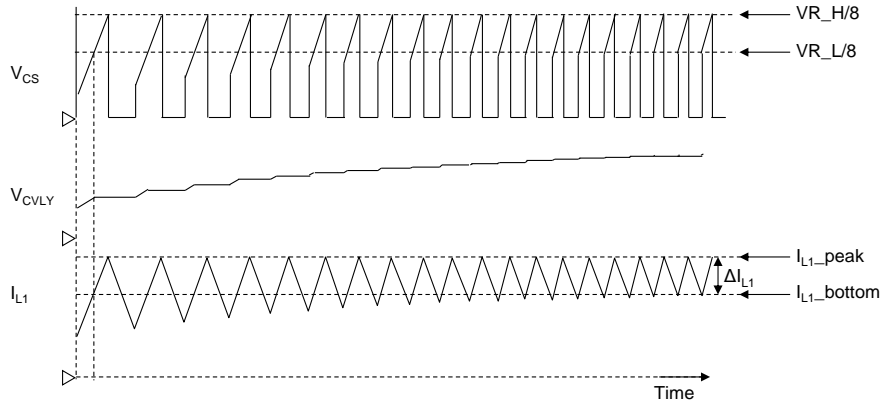
Figure 3. Bottom current control by the CVLY pin voltage

On the other hand, in the case that the bottom current is higher than $I_{L1bottom}$, the CS pin voltage becomes over VRL/8 when the GD pin turns ON. Consequently the capacitor (C4) connected to the CVLY pin is not charged, and just discharged by a very small current (Isnk). The CVLY pin voltage is decreased by this discharging and the OFF time becomes longer in every switching cycle. When the CS pin voltage becomes equal to VRL/8 while the GD pin is ON, the charge and discharge currents on the CVLY pin are balanced in a stable state.

1) Peak Current and Hysteresis Width Setting
Inductor average current (I_{L1Ave}) in the constant hysteresis width control is determined by the peak current (I_{L1peak}) and the hysteresis width (ΔI_{L1}) as follows:

$$I_{L1\_Ave} = I_{L1\_peak} - \frac{1}{2}\Delta I_{L1} \quad ...(2)$$

Hysteresis Width Setting:
The hysteresis width is determined by the RVLY pin voltage. An approximation of the RVLY pin voltage is described with the hysteresis width ΔI_{L1} [A] and resistor $R_6[\Omega]$ as follows:

$$V_{RVLY} = V_{REF} - 16.1 \times R_6 \times \Delta I_{L1} \quad [V] \, ...(3)$$

In this case, $V_{REF} = 5V$ and the hysteresis width (V_{CSHYS}) that is detected by the CS pin is described by the following equation.

$$V_{CSHYS} = R_6 \times \Delta I_{L1} = 0.0621 \times (V_{REF} - V_{RVLY}) \quad [V] \, ...(4)$$

Peak Current Setting:
When the GD pin turns ON, the CS pin voltage generated by the current and the resistor (R_6) is detected. When the ADIM pin voltage is higher than V_{MTH} (4.5V(typ)), the peak current (I_{L1peak}) is the current at 0.5V(typ) as the CS pin voltage. Therefore, the peak current is set by R_6 [Ω]. The relationship between I_{L1peak} and R_6 is approximated by the following equation.

$$I_{L1\_peak} = \frac{V_{SEN}}{R_6} \quad [\Omega] \, ...(5)$$

In this case, I_{L1peak} is a desired peak current. R_6 is calculated by the following equation.

$$R_6 = \frac{V_{SEN}}{I_{L1\_peak}} = \frac{V_{SEN} - \dfrac{V_{CSHYS}}{2}}{I_{L1\_Ave}} \quad [\Omega] \, ...(6)$$

The ratio of the inductor current and the hysteresis width with a maximum LED current ($V_{ADIM} \geq 4.5V$) is described by V_{SEN} and V_{CSHYS} as follows regarding equation (2), (4) and (6).

$$\frac{\Delta I_{L1}}{I_{L1\_Ave}} = \frac{1}{\dfrac{V_{SEN}}{V_{CSHYS}} - \dfrac{1}{2}} \quad \dots(7)$$

2) Switching Frequency

Since the constant ripple current control keeps the peak and bottom current constant, the current can be controlled without being affected by the input voltage fluctuation and LED VF variation while the switching frequency is changed by these changes.

Figure 4 shows examples of the frequency change when the input voltage and the number of LEDs connected in series (VF) are changed. In order to keep the frequency within desired switching frequency range, L1 and ΔI_{L1} need to be configured properly.
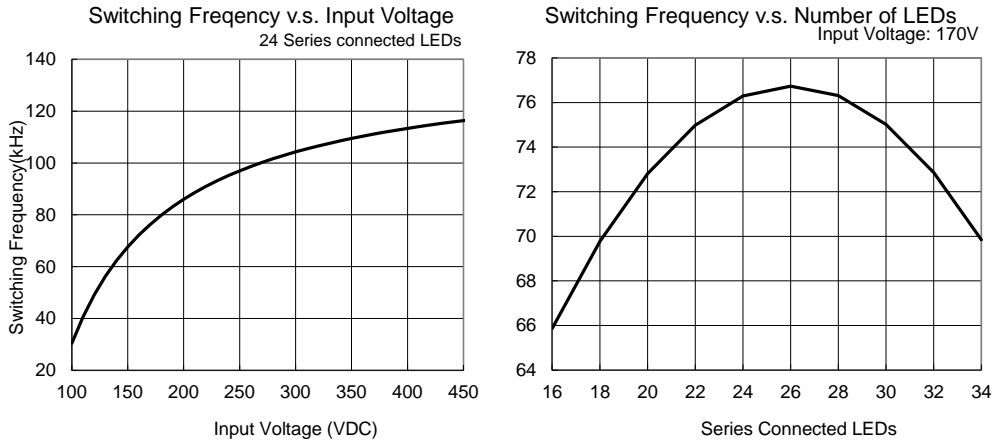
Figure 4. Examples of Switching Frequency Change by Input Voltage and Number of LEDs

Switching frequency F_{SW} is approximately given by the following expression.

$$F_{sw} = \frac{1}{L_1 \times \Delta I_{L1}} \times \frac{V_{out}}{V_{in}} (V_{in} - V_{out}) \quad [\text{Hz}] \dots(8)$$

L_1: Inductance value (H), ΔI_{L1}: Hysteresis width (A), V_{in}: LED anode voltage (V),
V_{out}: Total voltage of forward direction of LEDs in series (Vf [V])

Equation (8) shows that the coil inductance value is determined by a switching frequency, input/output voltage condition and hysteresis width. Therefore, for example, when desired input/output voltage conditions and switching frequency are known, the coil inductance value and the hysteresis width can be determined by deciding each one of the value.

3) Leading Edge Blanking Time and Minimum ON time of the GD pin

The AP1651 does not detect a current for a certain period after the N-channel power MOSFET (M_1) turns ON. This is called Leading Edge Blanking Time (T_{LEB}). This is a necessary period to avoid erroneous operation such as instantaneous shut down of the GD pin or ceasing the switching operation by the over current protection caused by a reverse recovery current of the diode (D_2) or a discharge current from parasitic capacitor are large when the M_1 is turned ON.
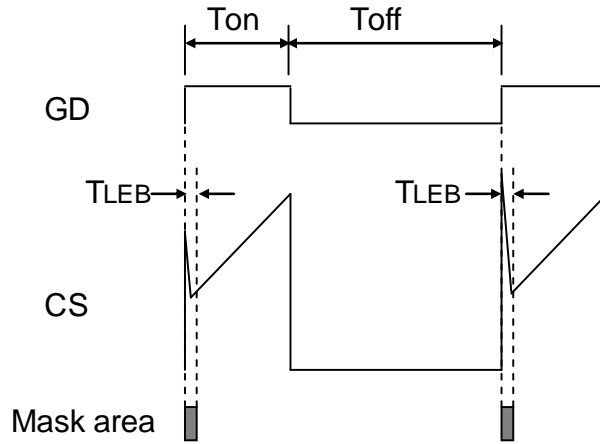
Figure 5. Masking Time for Preventing False Detection (T_{LEB}) on The CS Pin Voltage

However, all current detection on the CS pin starts after T_{LEB}, then the shortest ON time of the M_1 is limited by T_{LEB}. The T_{LEB} is 450ns in the worst case at 25°C. ON time (T_{on}) is limited by T_{LEB} and approximately given by the following equation.

$$\frac{V_{out}}{V_{in}} = T_{ON} \times F_{SW} \qquad \dots(9)$$

If ON time is less than T_{LEB} during the operation, the peak current will be higher than the setting and the average current will also shift higher, furthermore, the switching may be ceased due to the over current protection on the external N-channel power MOSFET.

$$V_{in} - V_{out} = \frac{L_1 \times \Delta I_{L1}}{T_{ON}} \qquad \dots(10)$$
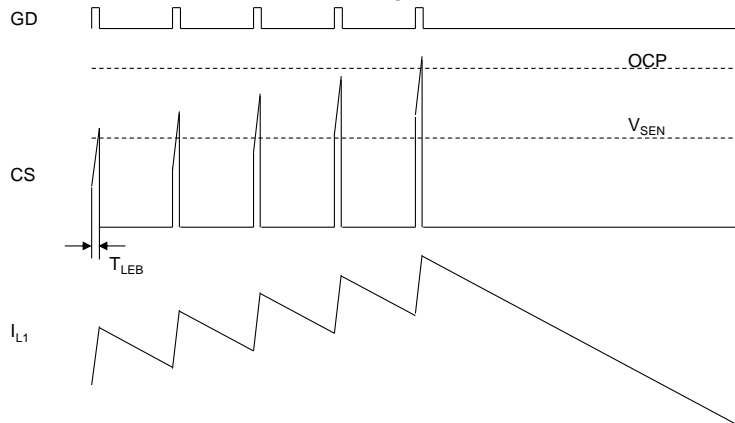
Figure 6. Peak Current Error by the Shortest ON Time (Shortest ON Time $< T_{LEB}$)

■ Linear Regulator Mode

Figure 7 shows current paths of a linear regulator with the AP1651.

The dashed line (3) is the current path. A fine current is controlled by flowing as V_{in}−LED−L_1−R_7−DRAIN pin−RC pin−R_2−GND.
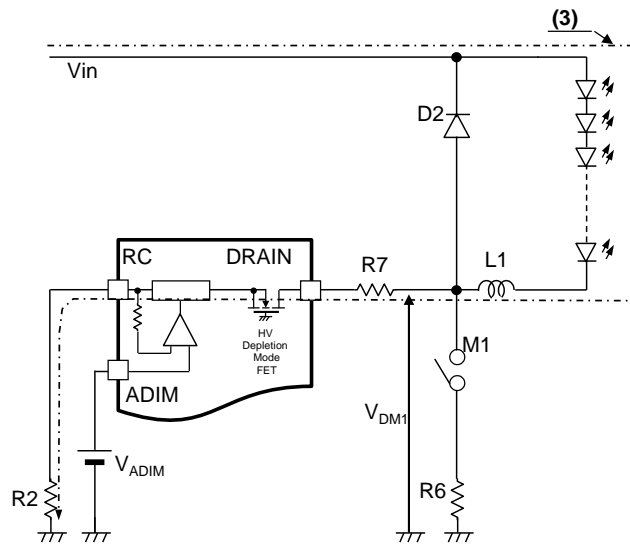

Figure 7. Operation Image of Linear Regulator Mode

The RC pin is controlled as so that its voltage becomes the same level as the ADIN pin voltage. Therefore, the current in this mode is determined by the R2 resistor which is connected to between the RC pin and the GND.

$$R_2 = \frac{V_{ADIM}}{I_{LEDs}} \quad [\Omega] \ldots (11)$$

I_{LEDs} indicates the current [A] that flows LED line, and V_{ADIM} indicates the voltage of the ADIM pin in linear regulator mode. For example, a 500μA (typ) current flows at $V_{ADIM} = 1V$ when the R2 resistor is 2kΩ. The R7 is a limiting resistor for the voltage between the DRAIN pin and the RC pin in a linear regulator mode operation. Heat generation of the IC can be suppressed by increasing the R7 value but the DRAIN pin must always be equal to or more than 10V (R2=2kΩ) in this mode.

$$R_7 = \frac{V_{in,MIN} - V_{out,MAX} - 10}{I_{LED}} \quad [\Omega] \ldots (12)$$

$V_{in, MIN}$ indicates the operating minimum input voltage (V). $V_{out, MAX}$ indicates the operating maximum output voltage (V) and normally it is the total forward voltage of LEDs (Vf). Power loss of the IC: P_{IC} is calculated by the following equation approximately.

$$P_{IC} = \left(V_{in,MAX} - V_{out,MIN}\right) \times I_{LED,MAX} - R_7 \times \left(I_{LED,MAX}\right)^2 - V_{ADIM} \times I_{LED,MAX} \quad [W] \ldots (13)$$

P_{IC} should be considered for thermal design. Please confirm these values on the actual printed board since the thermal resistance of the IC differs depending on the board. When the IC is over heated, the linear regulator will be stopped by the thermal shut down function.

When the VDD voltage is under UVLO voltage, a current of several hundred micro ampere flows between the DRAIN pin and the GND regardless of the ADIM pin or the PDIM pin voltage. The power supply circuit to the VDD pin should be designed as that the Vin becomes less than Vf (Vin < Vf) before the VDD pin voltage drops under V_{UVL}.

■ Dimming Control

1) Complex Dimming by the ADIM pin

Wide dimming range using the ADIM pin is available. One of the following three modes of dimming operation: "peak current control mode", "peak current control with PWM dimming mode" and "linear regulator mode" is chosen by the ADIM pin voltage. The input voltage range of the ADIM pin is from 0V to VREF(5V(typ)). The LED current is changed by the applied input voltage when it is less than 4V as Figure 8 shows.
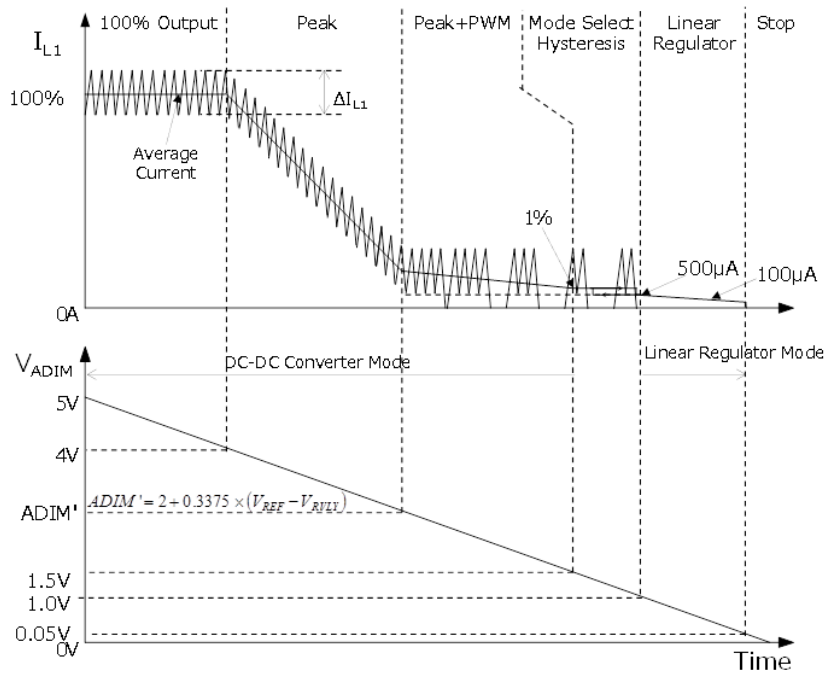

Figure 8. Complex Dimming by DC input (ADIM pin)

A brief overview of the three dimming methods by using the ADIM pin voltage, as shown on Figure 8, is as follows:

By decreasing the ADIM pin voltage below 5V, the peak current control starts from 4V. In this mode, the average current goes down by decreasing the peak current under constant hysteresis width control.

When the bottom current drops to a certain level, "peak current control with PWM dimming" mode is started. In this time, the peak current stops decreasing at the ADIM' voltage shown in Figure 8, and simultaneously, PWM dimming starts. The value of the ADIM' is approximately determined by the RVLY pin voltage defined by the ripple amplitude as following formula:

$$ADIM' = 2 + 0.3375 \times \left(V_{REF} - V_{RVLY}\right) \quad \dots(14)$$

- The average current is adjustable from 100% to 1% by changing the ADIM pin voltage in the range of V_{ADIM3} (V_{REF} to 1.5V).
- There is an invariable zone between 1.5V to 1V of the ADIM pin voltage where the average current cannot be changed at all.
- When the ADIM pin voltage is less than 1V, "linear regulator mode" starts. In this mode the switching operation stops (external N-channel power MOSFET is always off), and an internal constant current source connected to the DRAIN pin is active instead. The LED current can be dimmed from approximately 500µA to 100µA by tuning the ADIM pin voltage between 1V(typ) and 0.2V(typ).
- If the ADIM pin voltage is less than 0.05V, the operation mode is changed from the constant current source mode to LED current off mode in which the LED turns OFF.
- Operation of the PWM dimming in Peak + PWM state is the same as PWM dimming by the PDIM pin mentioned in the next paragraph except using an internal triangle waves.

PWM dimming frequency setting (C_3) in Peak + PWM state is controlled by the ADIM pin.
The PWM dimming frequency F_{PWM} (kHz) is approximately determined by the following expression according to the capacitor C_3 value (μF) connected between the CPWM pin and the GND.

$$F_{PWM} \approx \frac{1}{C_3} \times 10.33 \times 10^{-9} \qquad \text{[kHz]} \ldots (15)$$

The PWM dimming frequency must be set in the range from 200Hz to 5kHz.

Figure 9 shows hysteresis in dimming characteristics around PWM minimum pulse width. When a dimming level is lowered in the state where the bottom current control is performing, the LED current is controlled according to PWM pulse width (point A). When a dimming level is raised after the state where the bottom current control does not perform or power off, in order to that the bottom current control may not perform until the PWM pulse high width becomes longer than the sum of GD on time (GD ON) and maximum off time (40μsec), LED current does not increase (point B). Therefore, the dimming characteristics have a hysteresis.
In complex dimming by the ADIM pin, the minimum duty of PWM signal which generate in IC is 5%.
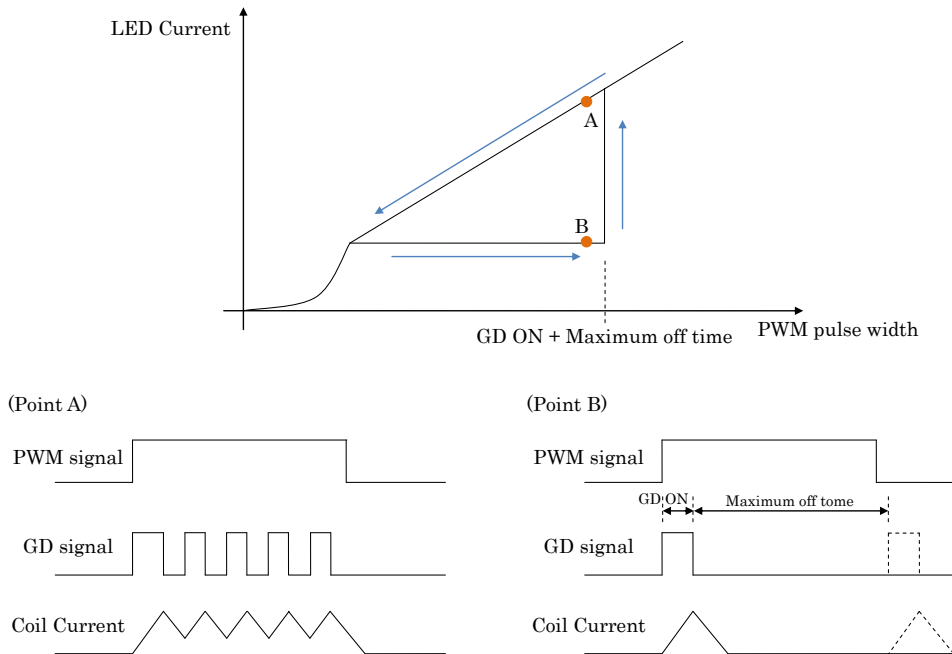

Figure 9. Hysteresis in dimming characteristics around PWM minimum pulse width

2) PWM Dimming by the PDIM pin

LED PWM dimming is available using the PDIM pin. It is controlled by applying a pulse voltage to the PDIM pin. Waveform diagram of the PDIM pin voltage (V_{PDIM}), Coil Current (I_{L1}), Switching Voltage of the current source for internal charging (S_1) and Switching Voltage of the current source for discharging (S_2) are shown in Figure 10.
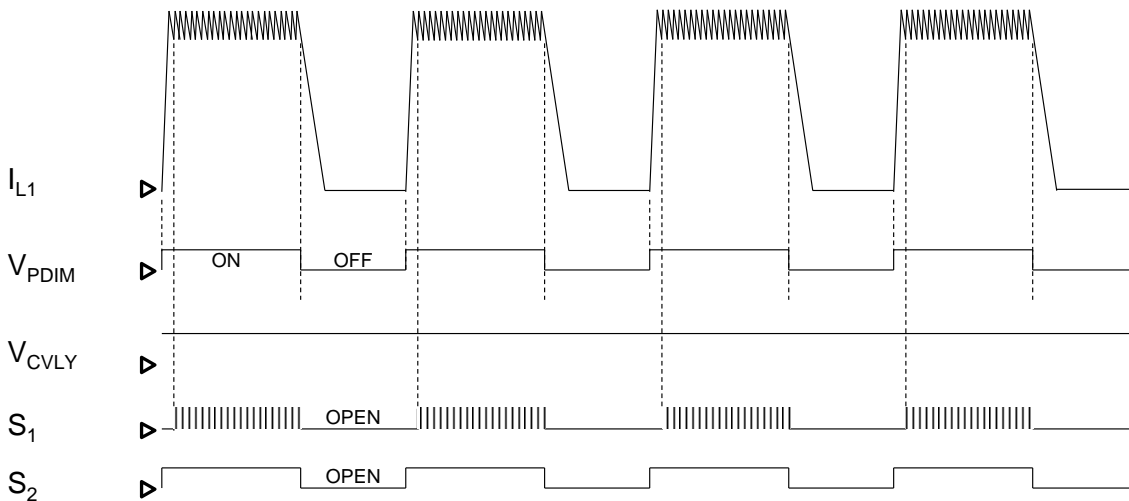

Figure 10. PWM Dimming Waveform

When V_{PDIM} turns ON from OFF state, the switching operation of the external N-channel power MOSFET (M_1) is started. The switching operation of the M_1 is stopped when V_{PDIM} is turned OFF. A dimming that is proportional to the PWM pulse duty is available by inputting PWM pulse to the PDIM pin repeatedly. For the first switching operation, the S_1 voltage is forcibly opened to avoid a spike current caused by an over charge of the capacitance C4 connected to the CVLY pin because the rise-up time that the I_{L1} reach to I_{L1Peak}(VRH/8) level after the M_1 is powered ON is long. When V_{PDIM} is OFF, the S_2 voltage is opened by discharging the C_4 not to lower the bottom current. By these operations, the CVLY pin voltage is kept in a level regardless of the duty of PWM dimming pulse. However, ON pulse of V_{PDIM} is needed at least for 2cycles to charge the C_4 capacitor. The LED current may be lower than the setting value if the ON pulse is shorter than this cycle. The minimum ON time of repeated pulse $T_{PWM,ON,MIN}$ to the PDIM pin is approximately calculated by the following expression.

$$T_{PWM,ON,MIN} = \frac{V_{ADIM} - 2}{4 \cdot R_6} \times \frac{L_1}{V_{in} - V_{out}} + 48 \times 10^{-6} \quad [s] \dots (16)$$

The CPWM pin should be connected to the GND in an application that uses both peak dimming by the ADIM pin and PWM dimming by the PDIM pin. By connecting the CPWM pin to the GND, a conflict in PWM dimming operation can be avoided since PWM dimming in DC-DC mode (complex dimming) is not executed.

During V_{PDIM} is OFF, S_1 and S_2 are open and therefore the CVLY pin is Hi-Z state. If V_{PDIM} OFF state continues for a long time such as when shut off LED by the PDIM pin, the charge of C_4 may be charge and discharge by the leak current etc. of IC or board. In the case of charged to C_4, the AP1651 start up in the short T_{OFF} time at turn on, and I_L is increased, and therefore the AP1651 may be latch stop by OCP. It shows an example of latch stop to Figure 11.
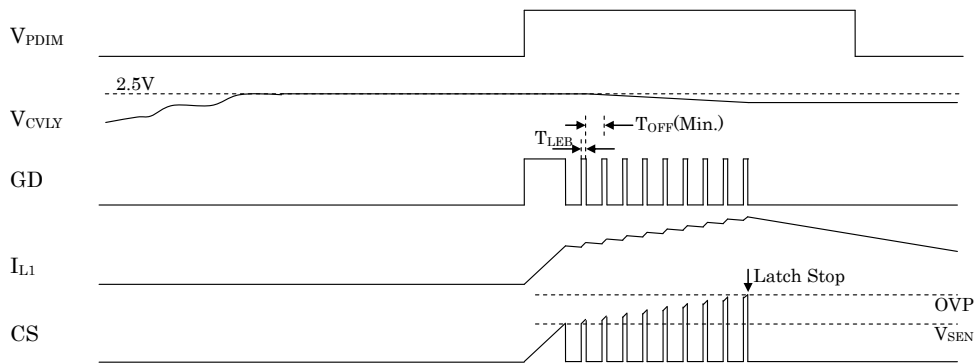
Figure 11. An example of latch stop at the time of LED turning on control by the PDIM pin

V_{ADIM} should be set below 1.1V to prevent from latch stop at the time of LED turning on during turning off by the PDIM pin. The AP1651 starts up from max T_{OFF} time because when set below 1.1V to V_{ADIM}, V_{CVLY} is fixed 0V. Also PCB layout should be noted not to make leak pass to charge to C4. It is effective to be covered with GND pattern and limited the leak path to the discharge side.

■ Gate Driver (GD)

The GD pin is a control pin for the external N-channel power MOSFET. It turns ON and OFF the external N-channel power MOSFET in the buck converter circuit. The GD pin outputs an equivalent voltage with the VDD pin. So the VDD pin voltage should be set in consideration for breakdown voltage of the external N-channel power MOSFET. The AP1651 controls the hysteresis width by detecting the current after masking period (T_{LEB}) following a power-up of the external N-channel power MOSFET.

■ Internal 5V Regulator (VREF)

The AP1651 has a 5V internal regulator for a reference voltage of internal circuits. The input voltage is applied from the VDD pin. A 5mA current at maximum can be output from the VREF pin under a proper thermal condition. A 1μF capacitor should be connected between the VREF pin and the GND for a stabilization. This connection line should be short as possible. Up to 10μF capacitance can be connected to the VREF pin depending on the ADIM dimming.

■ Protection Function

Table 1. Protection Function List

Protection Function	Detection Pin	Operation	Detection Condition	Corresponding Block and Operation	Release Condition
CS pin Open	CS	DC-DC	GD:ON AND CS≥0.8V	DRIVER Output: GND	(Note 11)
Over Current	CS	DC-DC	GD:ON AND CS≥0.8V	DRIVER Output: GND	(Note 11)
Thermal Protection	None	DC-DC and Linear Regulator	$Tj \geq T_{TSD}(150°C)$	DRIVER Output: GND 5V REG.: STOP LINEAR REG: STOP COMPLEX DIMMING CONTROLLER: STOP	$Tj \leq T_{TSD(150°C)} - \Delta T_{TSDHYS(55°C)}$
VDD UVLO	VDD	DC-DC and Linear Regulator	VDD≤ V_{UVL}(8.5V)	DRIVEROutput: GND 5V REG.: STOP LINEAR REG: STOP COMPLEX DIMMING CONTROLLER: STOP TSD: STOP	VDD≥V_{UVH}(10.5V)

Note 10. Values in this table are typical or design values. Refer to the "Electrical Characteristics" for details.

Note 11. In order to release the latch off state, apply a voltage that is less than V_{UVL} to the VDD pin for at least 10ms (in the case of the capacitor connected to the VREF pin is 1µF).

Note 12. When the VREF pin is shorted to the GND, the IC prevents heat generation by limiting the maximum current of the internal regulator to 12mA (design value).

1) CS pin Open Protection

This function prevents that the external N-channel power MOSFET continues to be ON when the CS pin is opened. If the CS pin is open, the CS pin voltage becomes the same level as the VREF voltage by an internal pull-up current circuit of the CS pin. By this voltage increase, over current protection is activated and the switching operation ceases.

2) Over Current Protection

If the CS pin voltage becomes higher than 0.8V after T_{LEB} period while the GD pin ON, the GD pin is turned OFF and fixed. In order to resume the switching operation, the IC needs to be reset (the VDD needs to be lower than V_{UVL} once).

3) Thermal Protection

To prevent a thermal runaway of the IC, the junction temperature is always monitored and the IC operation is controlled. When the junction temperature exceeds T_{TSD} (150°C typical in designed value), corresponding blocks shown in Table 1 are powered down. The AP1651 returns to normal operation when the junction temperature drops to the level below the hysteresis temperature T_{TSDHYS} (55°C in design value).

4) UVLO (Under Voltage Lockout)

Malfunctions at low supply voltage and the situation of insufficient gate drive voltage for the external N-channel power MOSFET are prevented.
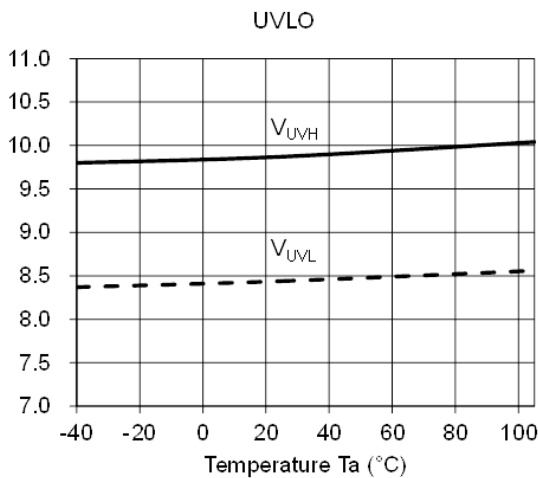
■ Typical Characteristic Examples
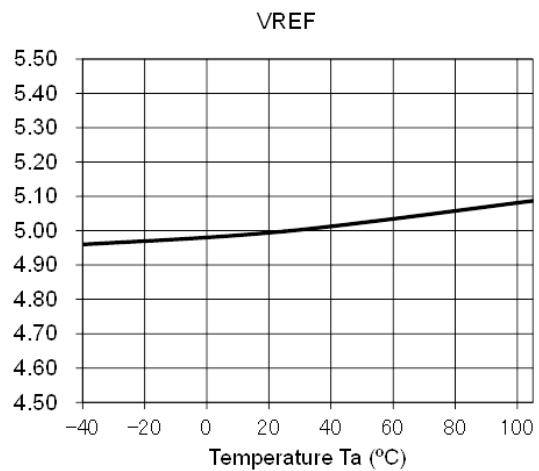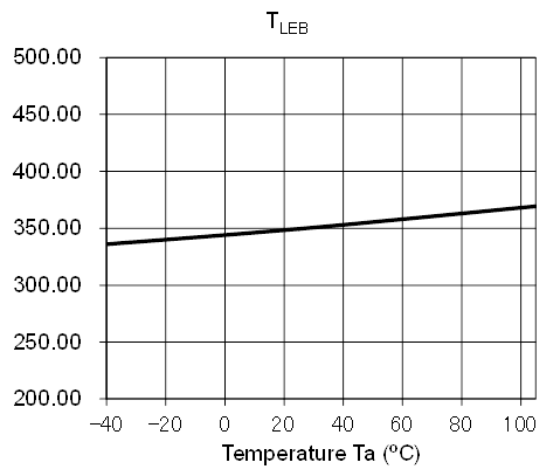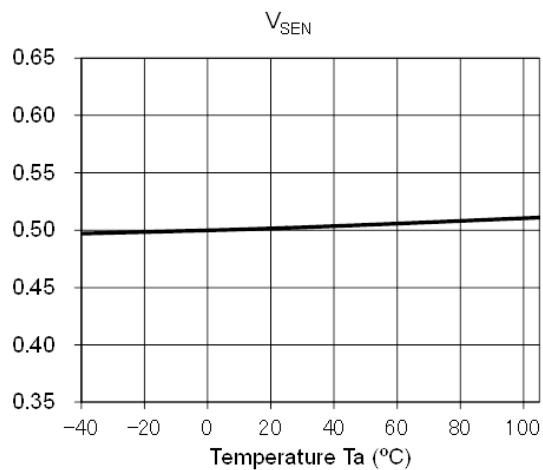

Figure 12. UVLO

Figure 13. VREF Pin Voltage

Figure 14. CS pin Peak Current Detection Voltage (VADIM=5V)   Figure 15. Leading Edge Blanking Time
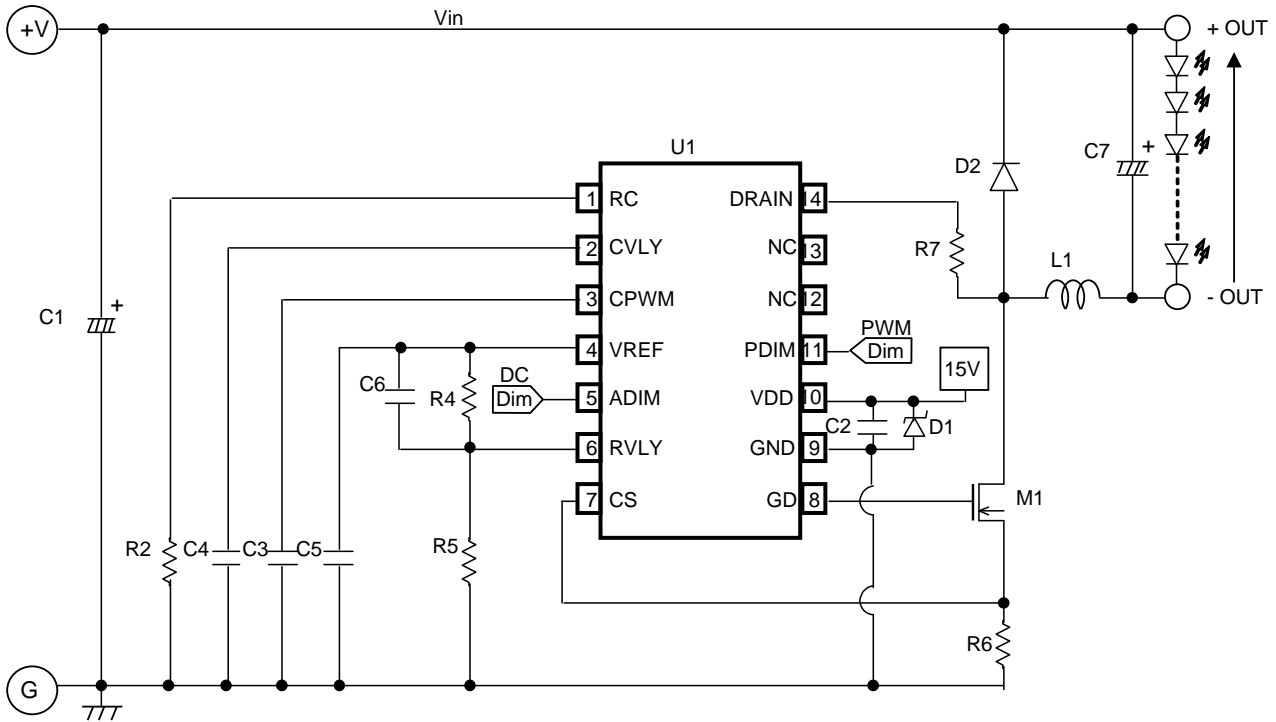
11. Recommended External Circuits

Figure 16. AP1651 External Circuit Example

Table 2. Recommended Parts List (200V_{DC} Input, 90V-700mA Output)

Ref Des	Qty	Description	Mfr	Mfr PN
U1	1	LED Driver IC	AKM	AP1651
L1	1	E30 Core/4.53mH	TDK	PC47EE30A200
M1	1	NMOS 500V/5A Ciss=360pF	ON	2SK4196LS
D1	1	ZENER 16V 200mW	Any	-
D2	1	FRD 50ns 600V/5A	ON	RD0506T
C1	1	47μF/450V	Rubycon	450PX47MEFC16X31.5
C2,C5	2	CER 10μF/25V X5R 0805	Any	-
C3	1	CER 0.022μF/50V X5R 0603	Any	-
C4	1	CER 2200pF/50V X5R 0603	Any	-
C6	1	CER 10000pF/50V X5R 0603	Any	-
C7	1	22μF/250V	Rubycon	250PX22MEFC10X16
R2	1	SMD 0603 2kΩ	Any	-
R4	1	SMD 0603 16kΩ	Any	-
R5	1	SMD 0603 24kΩ	Any	-
R6	3	SMD 0805 2Ω//2Ω//1.6Ω 1%	Any	-
R7	2	SMD 1206 150kΩ	Any	-

12. Typical Application Characteristics Examples

Examples of application characteristics with Figure 16 and Table 2 are shown below.
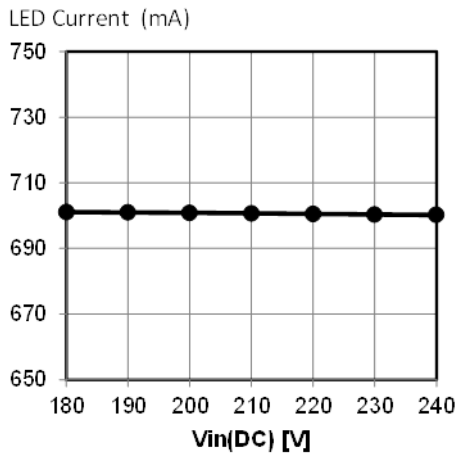
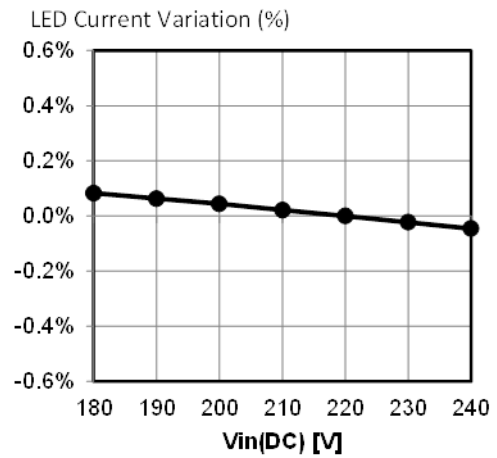Figure 17. LED Current vs. Vin(DC) (LED Vf=90V)

Figure 18. LED Current Ratio vs. Vin(DC)
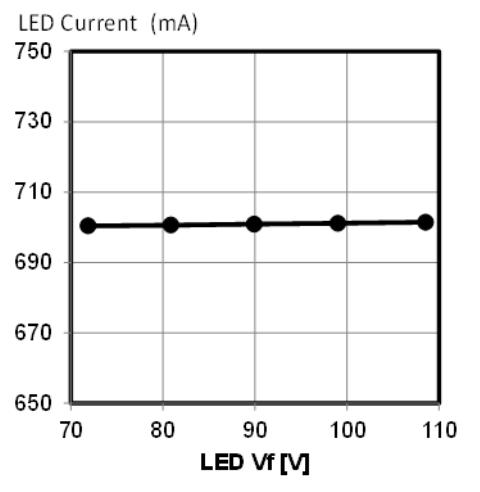(Reference: Vin=220V, LED Vf=90V)

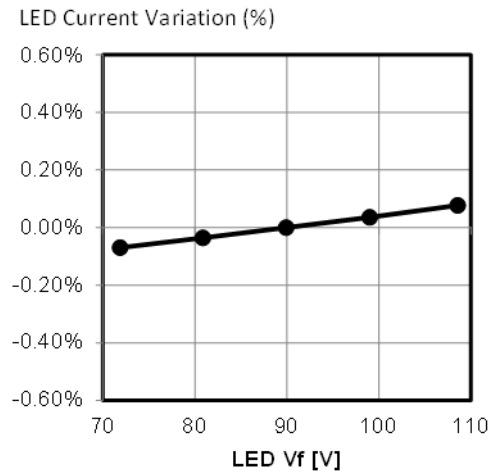Figure 19. LED Current vs. LED Vf (Vin(DC)=220V)

Figure 20. LED Current Ratio vs. LED Vf
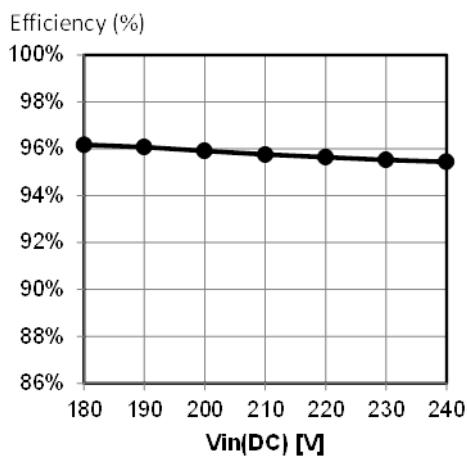(Reference: Vin=220V, LED Vf=90V)
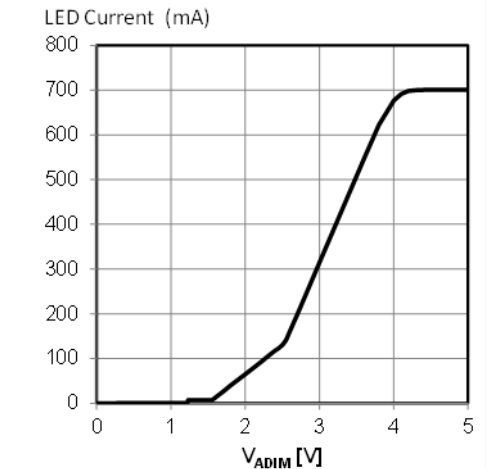
Figure 21. Efficiency vs. Vin(DC) (LED Vf=90V)

Figure 22. Complex Dimming Performance (VADIM)

13. Calculation for External Circuit Constants

Expressions here are based on a condition that assumes the LED current is 700mA, the Power Supply is 200V, the Vf for LED is 90V and the Operation frequency is 70kHz.

RVLY pin Setting (R_4, R_5)
V_{RVLY} has a range of 1.8V ~ 4.0V and normally operates at 3.5V. The hysteresis width of the CS pin (V_{CSHYS}) is determined by equation (17) using equation (4).

$$V_{CSHYS} = 0.0621 \times (V_{REF} - V_{RVLY}) \quad [V] \ldots(4)$$

$$V_{CSHYS} = (V_{REF} - V_{RVLY}) \times 0.0621 = (5 - 3.5) \times 0.0621 = 0.09315 \, [V] \quad \ldots(17)$$

And then, the hysteresis width ratio is determined by equation (18) using equation (7).

$$\frac{\Delta I_{L1}}{I_{L1\_Ave}} = \frac{1}{\dfrac{V_{SEN}}{V_{CSHYS}} - \dfrac{1}{2}} = \frac{1}{\dfrac{0.5}{0.09315} - 0.5} \approx 20.54 \, [\%] \quad \ldots(18)$$

V_{RRLY} is determined by a resistor divider at the VREF pin.

$$V_{RVLY} = V_{REF} \times \frac{R5}{R4 + R5} = 5 \times \frac{91 \, [k\Omega]}{39 \, [k\Omega] + 91 \, [k\Omega]} = 3.5 \, [V] \quad \ldots(19)$$

Connect a 0.01µF capacitor (C_6) between the RVLY pin and the VREF pin to stabilize V_{RVLY}.

CS pin Setting (R_6)
R_6 is determined by equation (20) using equation (6).

$$R_6 = \frac{V_{SEN} - \dfrac{V_{CSHYS}}{2}}{I_{L1\_Ave}} = \frac{500 \, [mV] - \dfrac{93.15 \, [mV]}{2}}{700 \, [mA]} \approx 0.6478 \, [\Omega] \quad \ldots(20)$$

The maximum peak current of the coil (except the spike noise when switching), the N-channel power MOSFET and a regenerative diode are equal to I_{L1peak} and it is determined by equation (21) using equation (5).

$$I_{L1\_peak} = \frac{0.5}{R_6} = \frac{0.5}{0.6478} \approx 0.772 \quad [A] \ldots(21)$$

Coil Inductance (L_1)
As mentioned in "2) Switching Frequency", the inductance value of the coil is determined by input/output voltage conditions and switching frequency [Fsw]. However, the setting calculations for the RVLY pin and the CS pin do not include group delay of the circuit. For example, ΔI_{L1} does not include group delay but T_{ON} includes group delay in equation (10). Therefore, a T_{ON} value without group delay must be calculated to determine the coil inductance by equation (10). Figure 23 shows a detailed time waveform of the GD pin voltage, the CS pin voltage and the coil current, which is shown in Figure 2, with group delay.
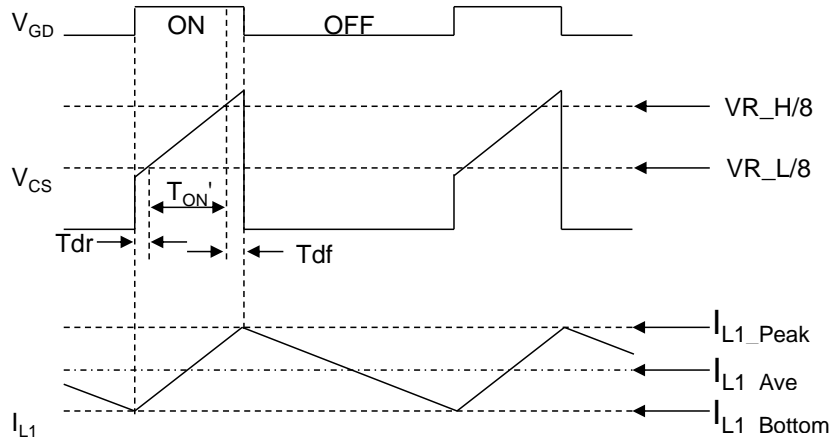
Figure 23. Time Waveform with Group Delay

In Figure 23, T_{dr} indicates group delay from a rising of the GD pin voltage to a falling of the A2 comparator. T_{df} indicates group delay from a peak current detection of the CS pin to a falling of the GD pin voltage. Although these values vary depending on the characteristics of M_1 and IC performance, group delays are approximately determined by following expressions.

Table 3. Group Delay

GD Falling Group Delay	$T_{df} \approx 200\,ns_{(typ)}$
GD Rising Group Delay	$T_{dr} \approx \left(210 + \dfrac{10^9}{101 \times F_{SW}}\right) ns_{(typ)}$

The time (T_{ON}'), which is from bottom limit setting value (VRL/8) to the upper limit setting value (VRH/8), is determined by equation (9') in consideration of group delay.

$$T_{ON}' = \frac{V_{out}}{V_{in} \times F_{SW}} - \left(T_{df} + T_{dr}\right) \quad \dots(9')$$

Calculation for T_{ON}' and inductance value L_1 from equation (9'), (10) and (4) are described as bellow.

$$T_{ON}' = \frac{90}{200 \times 70 \times 10^3} - \left(200 + 210 + \frac{10^9}{101 \times 70 \times 10^3}\right) \times 10^{-9} \approx 5.877 \times 10^{-6} \quad [s] \dots(22)$$

$$L_1 = \frac{(V_{in} - V_{out}) \times T_{ON}' \times R_6}{V_{CSHYS}} = \frac{(200 - 90) \times 5.877 \times 10^{-6} \times 0.6478}{0.09315} \approx 4.5 \times 10^{-3} \quad [H] \dots(23)$$

N-channel Power MOSFET Select (M_1)
The AP1651 executes bottom current detection on a timing of the gate voltage rising of an external N-channel power MOSFET (M_1). Use an N-channel power MOSFET that has a small gate capacitance C_{iss} to shorten the spike current period that is occurs at power-up of the MOSFET. For example, $C_{iss} \leq 500pF$ when the LED current = 700mA. The C_{iss} value should be in proportion to the LED current. Connect a heat sink if it is necessary for heat radiation.

Regenerative Diode Select (D_2)
Use a regenerative diode that has a breakdown voltage which is more than input voltage and an allowable current which is more than the maximum peak current I_{L1Peak}. A diode that has a short recovery time has high efficiency and is effective for reducing noises. Connect a heat sink if it is necessary for heat radiation.

Bottom Limit Value of Inductance (L_1) in "Peak + PWM" Operation by the ADIM pin
"Charging Period $T_{chg} \times 101 >$ Discharging Period T_{dis}" must be satisfied to keep a steady state of the CVLY voltage. If the charging period is shorter than this, LED current may be short to the setting value. Especially the bottom limit detection voltage will be in a lowest level if the ADIM pin voltage is $1.5V \leq V_{ADIM} \leq ADIM'$. The inductance and input/output voltage conditions should be determined carefully to ensure an enough charging time. Therefore the coil inductance value (L_1) must satisfy the formula below when using the complex dimming by the ADIM pin. This inductance should be determined in consideration of the variation in characteristics and temperature characteristics of the coil and LEDs.

$$L_1 \geq 81 \times 10^{-6} \times R_6 \times \frac{V_{in,MAX} - V_{out,MIN}}{Vbtm - V_{CSHYS}} \quad [\text{H}] \dots(24)$$

$$Vbtm = \frac{0.876 - 0.175 \times V_{RVLY}}{8} \times 100 \quad [\text{V}] \dots(25)$$

R_6 indicates the resistor (Ω) between the CS pin and the GND, $V_{in,MAX}$ indicates the maximum input voltage (V) of when the AP1651 is in operation, $V_{out,MIN}$ indicates the minimum output voltage (V) of when the AP1651 is in operation and V_{CSHYS} indicates the hysteresis width (V) that is detected by the CS pin.

The minimum necessary inductance value is described as shown below.

$$L_1 \geq 81 \times 10^{-6} \times 0.648 \times \frac{200 - 90}{3.294 - 0.093} \approx 1.80 \times 10^{-3} \quad [\text{H}] \dots(26)$$

Check if this value satisfies equation (23).

$$L_1 \approx 4.5 \times 10^{-3} {}_{(eq.23)} > 1.80 \times 10^{-3} {}_{(eq.25)} \quad \dots(27)$$

Formula (27) proves that the inductance value calculated by equation (23) can be used in all states of complex dimming by the ADIM pin.
On the other hand, if the inductance value does not satisfy formula (27), the ADIM pin operation in "Peak" state works normally when the ADIM voltage satisfies the expression below.

$$V_{ADIM,MIN} \geq 3.24 \times 10^{-6} \times R_6 \times \frac{V_{in,MAX} - V_{out,MIN}}{L_1} + 4.04 \times V_{CSHYS} + 2 \quad [\text{V}] \dots(28)$$

The LED current of the "Peak" state with the ADIM pin voltage that satisfies formula (28) is approximately calculated as below.

$$I_{LED} = \frac{1}{2 \times R_6} \times \left(\frac{V_{ADIM}}{2} - (V_{CSHYS} + 1) \right) \quad [\text{A}] \dots(29)$$

In this case, V_{ADIM} satisfies "$4V \geq V_{ADIM} \geq V_{ADIM,MIN}$".
For example, if the coil inductance L_1 is 1.5mH (which does not satisfy formula (27)), $V_{ADIM,MIN}$ becomes as shown below.

$$V_{ADIM,MIN} \geq 3.24 \times 10^{-6} \times 0.648 \times \frac{200 - 90}{1.5 \times 10^{-3}} + 4.04 \times 0.093 + 2 \approx 2.53 \quad [\text{V}] \dots(30)$$

In this case, the LED current I_{LED} is determined as shown below.

$$I_{LED} = \frac{1}{2 \times 0.648} \times \left(\frac{2.53}{2} - (0.093 + 1) \right) \approx 133 \quad [\text{mA}] \dots(31)$$

Therefore, the ADIM pin voltage can be set in a range of 0V to 1V or 2.53V to $V_{REF.}$

The maximum switching frequency of AP1651 is decided by the relation of input voltage, LED V_F voltage and current ripple amplitude. Following tables are guideline of maximum frequency and minimum coil value which is corresponds to maximum frequency at each LED current I_{LEDMAX} and LED V_F voltage when the V_{RVLY}=3.5V.

In addition, when the switching frequency is high, please take care of heat of external MOSFET.

Table 4. At Input Voltage DC400V

LED V_F	Maximum Frequency	I_{LED}				
		100mA	200mA	350mA	700mA	1000mA
25V	95kHz	L > 42.9mH	L > 21.5mH	L > 12.3mH	L > 6.2mH	L > 4.3mH
50V	154kHz	L > 40.1mH	L > 20.1mH	L > 11.5mH	L > 5.8mH	L > 4.0mH
75V	214kHz	L > 37.2mH	L > 18.6mH	L > 10.7mH	L > 5.4mH	L > 3.8mH
100V	273kHz	L > 34.3mH	L > 17.2mH	L > 9.8mH	L > 4.9mH	L > 3.5mH
125V	332kHz	L > 31.5mH	L > 15.8mH	L > 9.0mH	L > 4.5mH	L > 3.2mH
150V	392kHz	L > 28.6mH	L > 14.3mH	L > 8.2mH	L > 4.1mH	L > 2.9mH

Table 5. At Input Voltage DC200V

LED V_F	Maximum Frequency	I_{LED}				
		100mA	200mA	350mA	700mA	1000mA
25V	214kHz	L > 20.1mH	L > 10.1mH	L > 5.8mH	L > 2.9mH	L > 2.0mH
50V	332kHz	L > 17.2mH	L > 8.6mH	L > 4.9mH	L > 2.5mH	L > 1.8mH
75V	451kHz	L > 14.3mH	L > 7.2mH	L > 4.1mH	L > 2.1mH	L > 1.5mH
100V	569kHz	L > 11.5mH	L > 5.8mH	L > 3.3mH	L > 1.7mH	L > 1.2mH
125V	688kHz	L > 8.6mH	L > 4.3mH	L > 2.5mH	L > 1.3mH	L > 0.9mH
150V	806kHz	L > 5.8mH	L > 2.9mH	L > 1.7mH	L > 0.9mH	L > 0.6mH

14. Package

■ Outline Dimensions
・14-pin SOP   [Unit: mm]
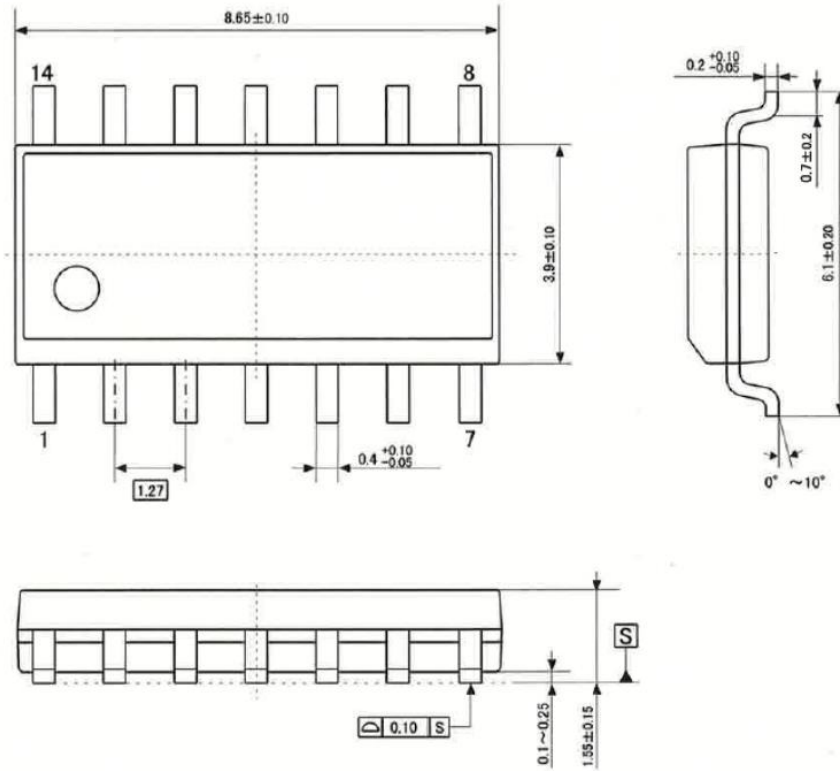
■ Recommended Pad Dimensions

Reference Mount Pad

■ **Marking**
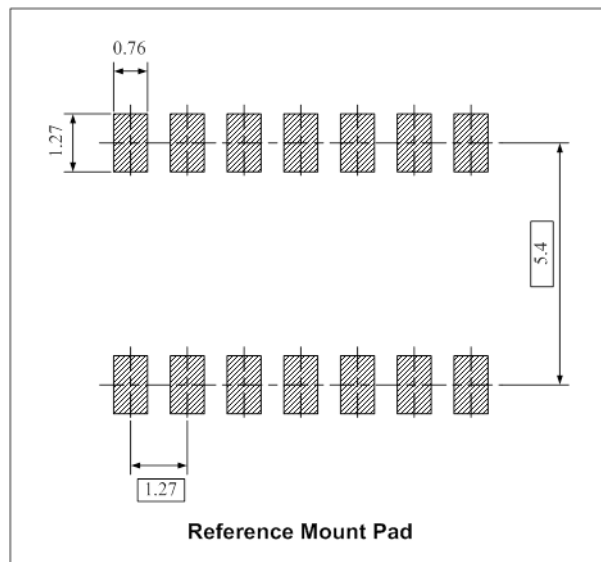
AP1651B
$X_1X_2X_3X_4X_5X_6X_7$
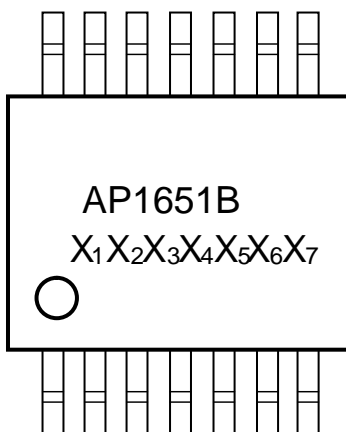
Upper	Product name：AP1651B
Lower	Date code: 7 digits 2 digits (Last 2 digits of year) +2 digits (weekly code) + 3 digits (production code)

15. Revision History

Date (Y/M/D)	Revision	Page	Contents
14/6/25	00		First edition
14/10/30	01	4	Correct ADIM range value from 4V~0.125V to 4 to 0.2V.
		6	Add min/max values into ADIM pin Pull-up Current
		8	Correct VADIM2 voltage range of Linear regulator mode from "0.13 to 1.0V" to "0.2 to 1.0V".
		14	Correct VADIM value from 0.125 to 0.05V in Figure.8
		14	Correct VADIM3 voltage range from "4V to 1.5V" to "VREF to 1.5V".
		14	Correct the sentence When the ADIM pin voltage is less than VADIM2(0.13 to 1V), ··· →When the ADIM pin voltage is less than 1V, ···
		14	Correct the sentence If the ADIM pin voltage is less than 0.1V(VADIM1), ··· →If the ADIM pin voltage is less than 0.05V,
15/05/28	02	6	Add min/max values into UVLO Hysteresis.
		6	Add min/max values into PDIM Pull Down.
		6	Add min/max values into GD Pull Down.
		6	Add min/max values into Gate Driver Rise Time and Fall Time.
15/11/2	03	16-17	Add the caution in case of turn off by the PDIM pin and shift the later page number

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