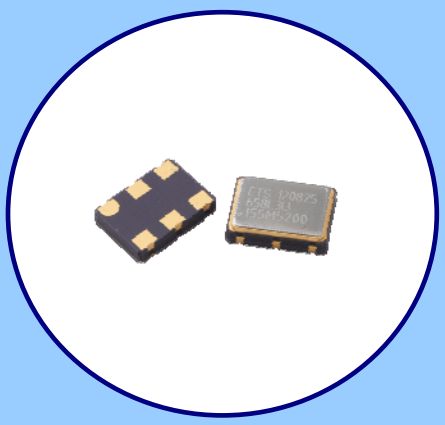
Model 635

Low Jitter
LVPECL or LVDS Clock Oscillator

FEATURES

- **Standard 7.0mm x 5.0mm, 6-Pad Surface Mount Package**
- **Low Phase Jitter, 0.7ps RMS Maximum**
- **LVPECL or LVDS Output**
- **Fundamental and 3rd Overtone Crystal Designs**
- Frequency Range 10 – 320 MHz
- Frequency Stability ±50 ppm Standard
- Operating Voltages +2.5Vdc or +3.3Vdc
- Operating Temperature to -40°C to +85°C
- Output Enable Standard
- Tape & Reel Packaging Standard, EIA-418
- **RoHS/Green Compliant [6/6]**



APPLICATIONS

Model 635 is ideal for applications such as broadband access, SerDes, Ethernet/Gigabit Ethernet, SONET/SDH and optical networking.

ORDERING INFORMATION

635 □ □ □ □ □ □ □ M □ □ □ □

OUTPUT TYPE
P = LVPECL - Pin 1 Enable [std]
L = LVDS - Pin 1 Enable [std]
E = LVPECL - Pin 2 Enable [opt]
V = LVDS - Pin 2 Enable [opt]

FREQUENCY STABILITY
6 = ± 20 ppm [1]
5 = ± 25 ppm
3 = ± 50 ppm
2 = ± 100 ppm

FREQUENCY IN MHz
M - indicates MHz and decimal point. [2]

SUPPLY VOLTAGE
2 = 2.5 Vdc
3 = 3.3 Vdc

OPERATING TEMPERATURE RANGE
A = -10°C to +60°C
C = -20°C to +70°C
I = -40°C to +85°C [2]

1] Consult factory for availability of 6I Stability/Temperature combination.
2] Frequency is recorded with 3 significant digits before the 'M' and 4 significant digits after the 'M' (including zeros).
See Table I for part number frequency codes that exceed 4 significant digits.
[Ex. XXXMXXXX (008M0000), XXXMXXXX (049M1520), XXXMXXXX (122M8800)]

Not all performance combinations and frequencies may be available.
Contact your local CTS Representative or CTS Customer Service for availability.

PACKAGING INFORMATION [reference]

Device quantity is 1k pcs. maximum per 180mm reel.

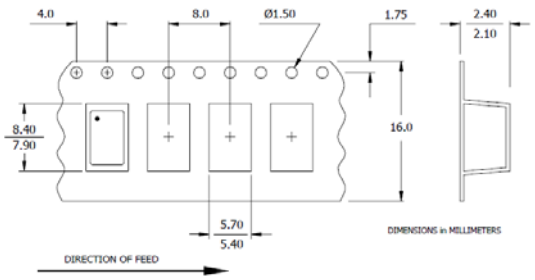


Table I

NOMINAL FREQUENCY [MHz]	CTS PART NUMBER FREQUENCY CODE
025.000625	025M0006
101.575694	101M5756
125.009375	125M0093
148.351648	148M351A
153.600770	153M6007
156.253906	156M2539
178.018970	178M0189

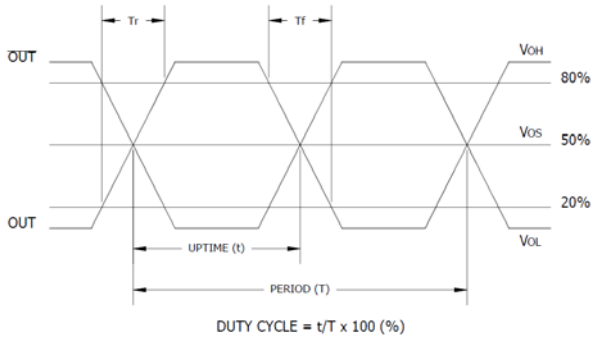
ELECTRICAL CHARACTERISTICS

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
ELECTRICAL PARAMETERS	Maximum Supply Voltage	V_{CC}	-	-0.5	-	5.0	V
	Storage Temperature	T_{STG}	-	-40	-	+100	°C
	Frequency Range						
	LVPECL	f_O	-	10.00	-	320	MHz
	LVDS			80.00	-	320	
	Frequency Stability	$\Delta f/f_O$	All Inclusive, see Note 1.	-	-	20, 25, 50, 100	± ppm
			1st year aging	-	-	3	
	Operating Temperature						
	Commercial	T_A	-	-20	25	+70	°C
	Industrial			-40		+85	
	Supply Voltage	V_{CC}	± 5 %	2.38	2.5	2.63	V
				3.14	3.3	3.47	
	Supply Current						
	LVPECL	I_{CC}	Maximum Load	-	-	88	mA
	LVDS			-	-	65	
	Start Up Time	T_S	Application of V_{CC}	-	2	5	ms
	Phase Jitter	tjrms	Bandwidth 12 kHz - 20 MHz	-	0.3	0.7	
	Period Jitter RMS	pjrms	-	-	2.6	-	ps
	Period Jitter Pk-Pk		-	-	25	-	
	Enable Function		Standby				
	Enable Input Voltage	V_{IH}	Pin 1 or 2 Logic '1', Output Enabled	0.7*V_{CC}	-	-	V
	Disable Input Voltage	V_{IL}	Pin 1 or 2 Logic '0', Output Disabled	-	-	0.3*V_{CC}	
	Disable Time	T_{PLZ}	Pin 1 or 2 Logic '0' , Output Disabled	-	-	200	ns
	Enable Time	T_{PLZ}	Pin 1 or 2 Logic '1', Output Enabled	-	-	2	ms
	LVPECL WAVEFORM						
	Output Load	R_L	Terminated to V_{CC} - 2.0V	-	50	-	Ohms
	Output Duty Cycle	SYM	@ V_{CC} - 1.3V	45	-	55	%
	Output Voltage Levels						
	Logic '1' Level	V_{OH}	PECL Load, -20°C to +70°C	V_{CC} - 1.025	-	V_{CC} - 0.880	V
	Logic '0' Level	V_{OL}	PECL Load, -20°C to +70°C	V_{CC} - 1.810	-	V_{CC} - 1.620	
	Logic '1' Level	V_{OH}	PECL Load, -40°C to +85°C	V_{CC} - 1.085	-	V_{CC} - 0.880	V
	Logic '0' Level	V_{OL}	PECL Load, -40°C to +85°C	V_{CC} - 1.830	-	V_{CC} - 1.555	
	Rise and Fall Time	T_R, T_F	@ 20% - 80% Levels	-	0.3	0.7	ns
	LVDS WAVEFORM						
	Output Load	R_L	Between Outputs	-	100	-	Ohms
	Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
	Differential Output Voltage	V_{OD}	R_L = 100 Ohms	247	350	454	mV
	Offset Voltage	V_{OS}	LVDS Load	1.125	1.25	1.375	V
	Output Voltage Levels						
	Logic '1' Level	V_{OH}	LVDS Load	-	1.43	1.60	V
	Logic '0' Level	V_{OL}	LVDS Load	0.90	1.10	-	
	Rise and Fall Time	T_R, T_F	@ 20% - 80% Levels	-	0.4	0.7	ns

Notes:

1. Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

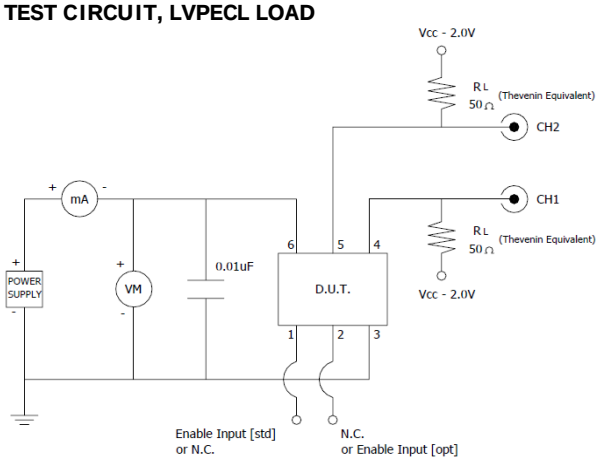
LVPECL/LVDS OUTPUT WAVEFORM



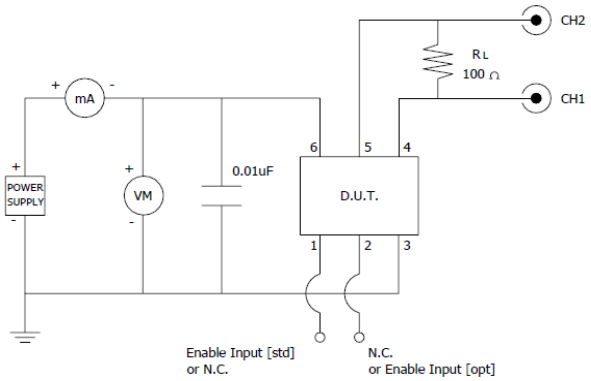
ENABLE TRUTH TABLE

PIN 1 or Pin 2	PIN 4 & 5
Logic '1'	Output
Open	Output
Logic '0'	High Z

TEST CIRCUIT, LVPECL LOAD

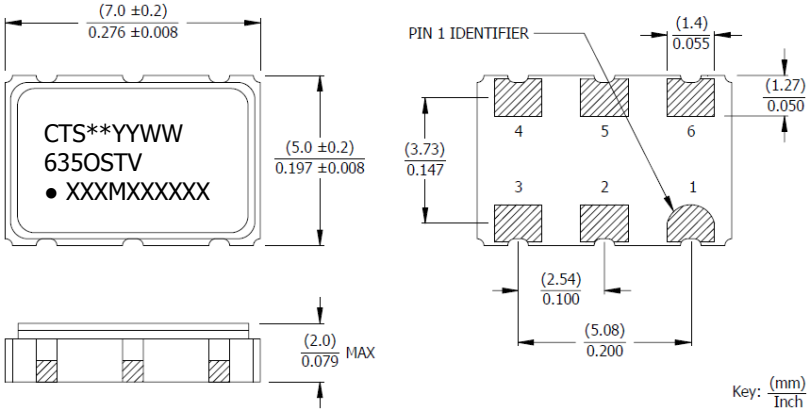


TEST CIRCUIT, LVDS LOAD



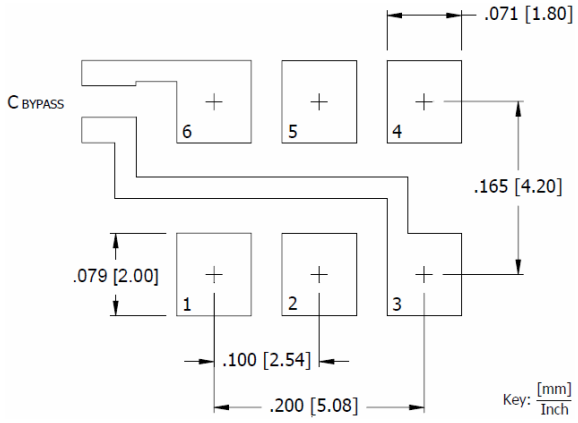
MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



SUGGESTED SOLDER PAD GEOMETRY

C_{BYPASS} should be ≥ 0.01 uF.



MARKING INFORMATION

1. ** - Manufacturing Site Code.
2. YYWW – Date code, YY – year, WW – week.
3. O – Output Type. P or E = LVPECL, L or V = LVDS.
4. ST – Frequency stability/temperature code. [Refer to Ordering Information.]
5. V – Voltage code. 3 = 3.3V, 2 = 2.5V
6. XXXMXXXXXX – Frequency is marked with only leading significant digits before the 'M' and 4 – 6 digits after the 'M' (including zeros).
   Ex. XXMXXXX [19M4400]
   XXXMXXXXX [153M60077]
   XXXMXXXXXX [148M351648]

NOTES

1. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.
2. Termination pads [e4]. Barrier-plating is nickel [Ni] with gold [Au] flash plate.
3. Reflow conditions per JEDEC J-STD-020; 260°C maximum, 20 seconds.
4. MSL = 1.

D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	EOH or N.C.	Enable [std] or No Connect
2	N.C. or EOH	No Connect or Enable [opt]
3	GND	Circuit & Package Ground
4	Output	RF Output
5	Output	Complimentary RF Output
6	V_{CC}	Supply Voltage