

## Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of <http://www.nxp.com>, <http://www.philips.com/> or <http://www.semiconductors.philips.com/>, use <http://www.nexperia.com>

Instead of [sales.addresses@www.nxp.com](mailto:sales.addresses@www.nxp.com) or [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com), use [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com) (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:

- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved

Should be replaced with:

- © **Nexperia B.V. (year). All rights reserved.**

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

# 74LVC162373A; 74LVCH162373A

16-bit D-type transparent latch; 30  $\Omega$  series termination resistors; 5 V tolerant inputs/outputs; 3-state

Rev. 4 — 14 May 2013

Product data sheet

## 1. General description

---

The 74LVC162373A and 74LVCH162373A are 16-bit D-type transparent latches with separate D-type inputs with bus hold (74LVCH162373A only) for each latch and 3-state outputs for bus-oriented applications. One latch enable (pin nLE) input and one output enable (pin n $\overline{OE}$ ) are provided for each octal. Inputs can be driven from either 3.3 V or 5 V devices. When disabled, up to 5.5 V can be applied to the outputs. These features allow the use of these devices in mixed 3.3 V and 5 V applications. The device consists of two sections of eight D-type transparent latches with 3-state true outputs. When pin nLE is HIGH, data at the corresponding data inputs (pins nDn) enter the latches. In this condition, the latches are transparent, that is, the latch output changes each time its corresponding data inputs changes. When pin nLE is LOW, the latches store the information that was present at the data inputs a set-up time preceding the HIGH to LOW transition of pin nLE. When pin n $\overline{OE}$  is LOW, the contents of the eight latches are available at the outputs. When pin n $\overline{OE}$  is HIGH, the outputs go to the high-impedance OFF-state. Operation of the n $\overline{OE}$  input does not affect the state of the latches.

The device is designed with 30  $\Omega$  series termination resistors in both HIGH and LOW output stages to reduce line noise. Bus hold on data inputs eliminates the need for external pull-up resistors to hold unused inputs.

## 2. Features and benefits

---

- 5 V tolerant inputs/outputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Multibyte flow-through standard pinout architecture
- Multiple low inductance supply pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (74LVCH162373A only)
- High-impedance when  $V_{CC} = 0$  V
- Complies with JEDEC standard:
  - ◆ JESD8-7A (1.65 V to 1.95 V)
  - ◆ JESD8-5A (2.3 V to 2.7 V)
  - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)



- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-B exceeds 200 V
  - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC162373ADGG 74LVCH162373ADGG	-40 °C to +125 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVC162373ADL 74LVCH162373ADL	-40 °C to +125 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1

### 4. Functional diagram

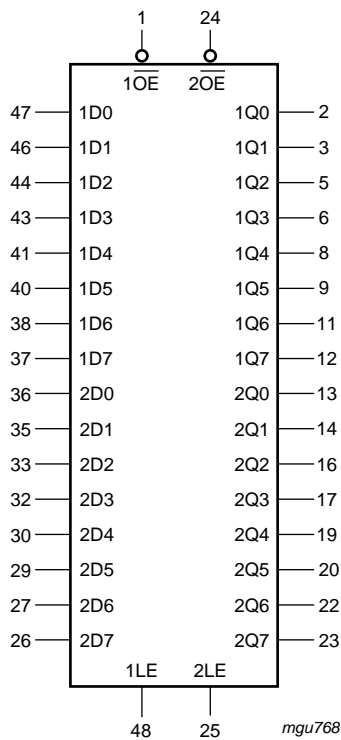


Fig 1. Logic symbol

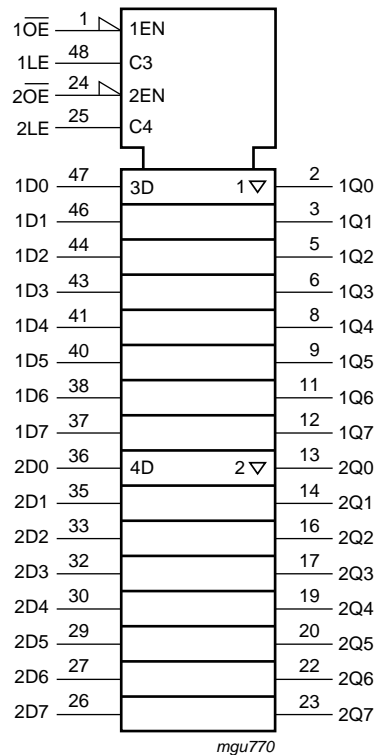


Fig 2. IEC logic symbol

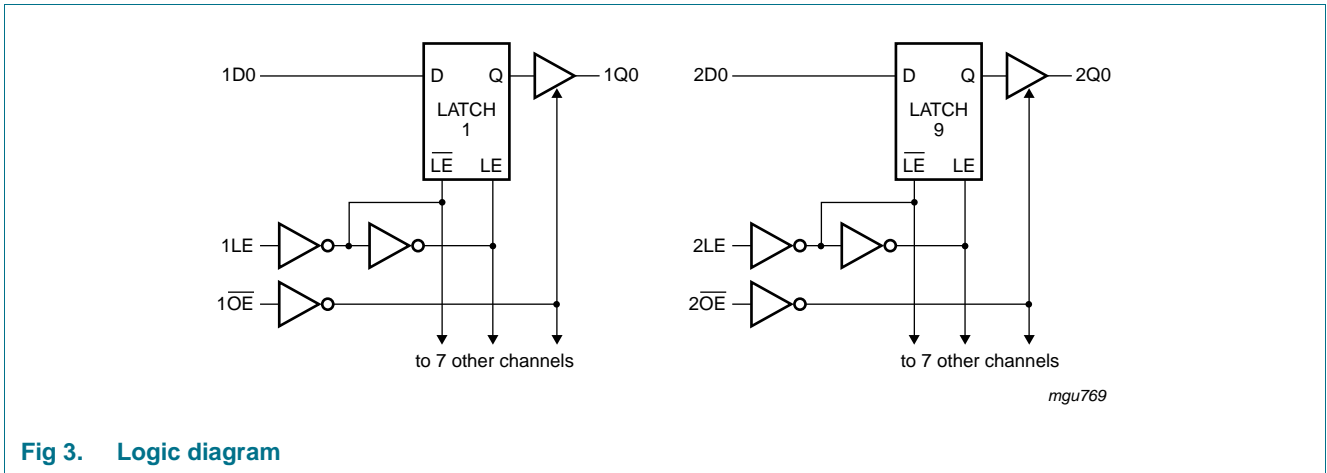


Fig 3. Logic diagram

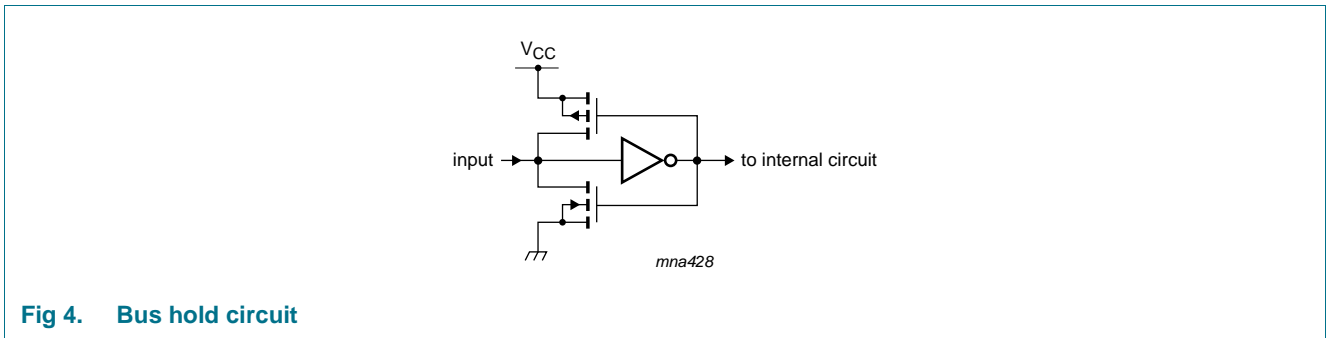


Fig 4. Bus hold circuit

## 5. Pinning information

### 5.1 Pinning

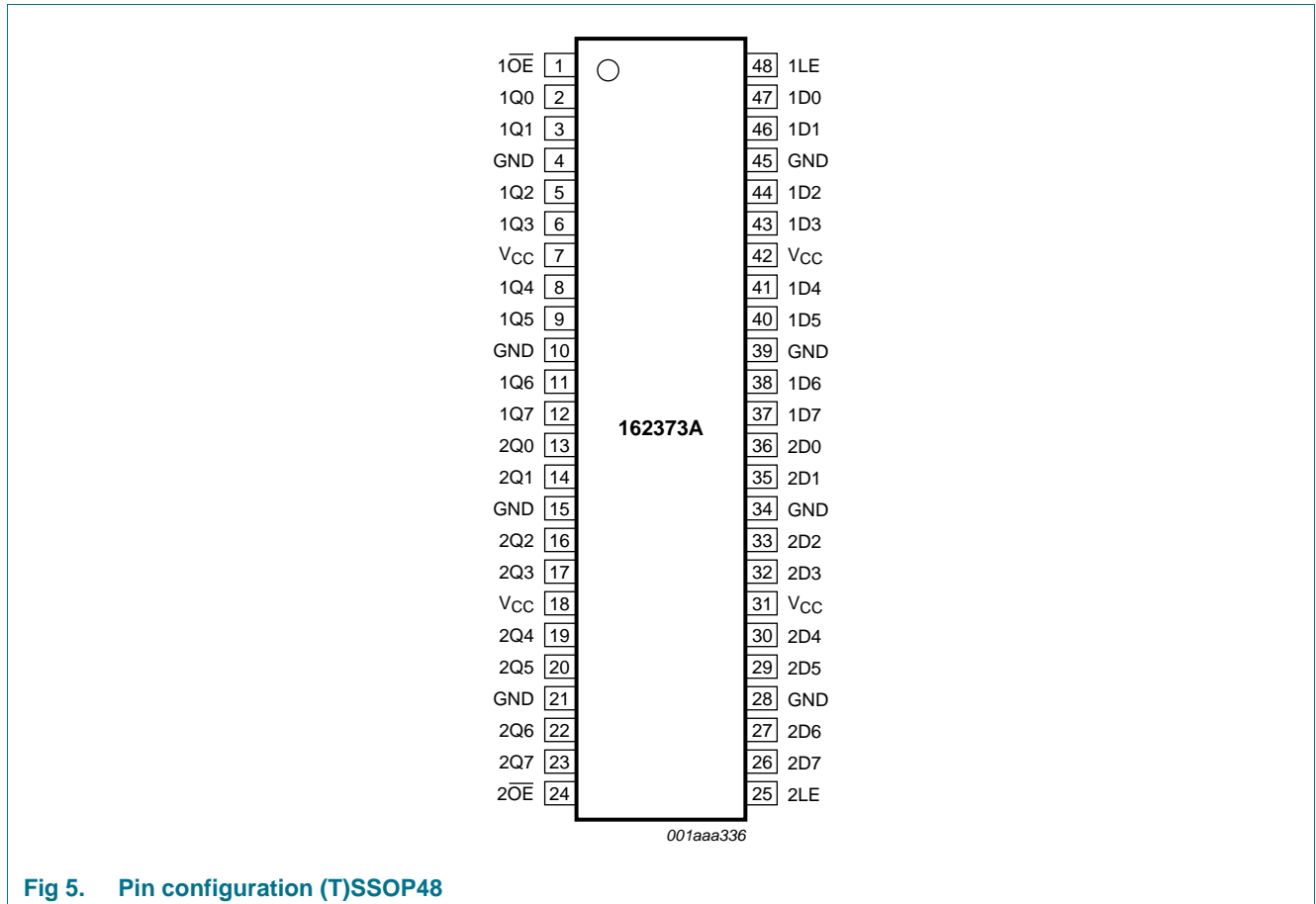


Fig 5. Pin configuration (T)SSOP48

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE	1	output enable input (active LOW)
2OE	24	output enable input (active LOW)
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
VCC	7, 18, 31, 42	supply voltage
1LE	48	latch enable input (active HIGH)
2LE	25	latch enable input (active HIGH)
1D[0:7]	47, 46, 44, 43, 41, 40, 38, 37	data input
2D[0:7]	36, 35, 33, 32, 30, 29, 27, 26	data input
1Q[0:7]	2, 3, 5, 6, 8, 9, 11, 12	data output
2Q[0:7]	13, 14, 16, 17, 19, 20, 22, 23	data output

## 6. Functional description

Table 3. Functional table (per section of 8 bits)<sup>[1]</sup>

Operating modes	Input			Internal Latch	Output nQn
	nOE	nLE	nDn		
Enable and read register (transparent mode)	L	H	L	L	L
	L	H	H	H	H
Latch and read register	L	L	l	L	L
	L	L	h	H	H
Latch register and disable outputs	H	L	l	L	Z
	H	L	h	H	Z

- [1] H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition  
 Z = high-impedance OFF-state

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	supply voltage		-0.5	+6.5	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		<sup>[1]</sup> -0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	$\pm 50$	mA
$V_O$	output voltage	output HIGH or LOW state	<sup>[2]</sup> -0.5	$V_{CC} + 0.5$	V
		output 3-state	<sup>[2]</sup> -0.5	+6.5	V
$I_O$	output current	$V_O = 0$ V to $V_{CC}$	-	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	$^{\circ}$ C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ $^{\circ}$ C to +125 $^{\circ}$ C	<sup>[3]</sup> -	500	mW

- [1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.  
 [2] The output voltage ratings may be exceeded if the output current ratings are observed.  
 [3] Above 60  $^{\circ}$ C, the value of  $P_{tot}$  derates linearly with 5.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
$V_I$	input voltage		0	-	5.5	V
$V_O$	output voltage	output HIGH or LOW state	0	-	$V_{CC}$	V
		output 3-state	0	-	5.5	V
$T_{amb}$	ambient temperature	in free air	-40	-	+125	$^{\circ}\text{C}$
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65 \text{ V to } 2.7 \text{ V}$	0	-	20	ns/V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$			-40 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$V_{CC} = 1.2 \text{ V}$	1.08	-	-	1.08	-	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	-	-	$0.65 \times V_{CC}$	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	-	-	1.7	-	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2.0	-	-	2.0	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC} = 1.2 \text{ V}$	-	-	0.12	-	0.12	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	-	-	0.8	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$						
		$I_O = -100 \mu\text{A}$ ; $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	$V_{CC} - 0.2$	$V_{CC}$	-	$V_{CC} - 0.3$	-	V
		$I_O = -2 \text{ mA}$ ; $V_{CC} = 1.65 \text{ V}$	1.2	-	-	1.05	-	V
		$I_O = -4 \text{ mA}$ ; $V_{CC} = 2.3 \text{ V}$	1.7	-	-	1.55	-	V
		$I_O = -6 \text{ mA}$ ; $V_{CC} = 2.7 \text{ V}$	2.2	-	-	2.05	-	V
		$I_O = -12 \text{ mA}$ ; $V_{CC} = 3.0 \text{ V}$	2.2	-	-	2.0	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$						
		$I_O = 100 \mu\text{A}$ ; $V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	-	-	0.2	-	0.3	V
		$I_O = 2 \text{ mA}$ ; $V_{CC} = 1.65 \text{ V}$	-	-	0.45	-	0.65	V
		$I_O = 4 \text{ mA}$ ; $V_{CC} = 2.3 \text{ V}$	-	-	0.6	-	0.8	V
		$I_O = 6 \text{ mA}$ ; $V_{CC} = 2.7 \text{ V}$	-	-	0.4	-	0.6	V
		$I_O = 12 \text{ mA}$ ; $V_{CC} = 3.0 \text{ V}$	-	-	0.55	-	0.8	V
$I_I$	input leakage current	$V_{CC} = 3.6 \text{ V}$ ; $V_I = 5.5 \text{ V}$ or GND <sup>[2]</sup>	-	$\pm 0.1$	$\pm 5$	-	$\pm 20$	$\mu\text{A}$

**Table 6. Static characteristics ...continued**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	−40 °C to +85 °C			−40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>CC</sub> = 3.6 V; V <sub>O</sub> = 5.5 V or GND <sup>[2]</sup>	-	0.1	±5	-	±20	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 5.5 V	-	0.1	±10	-	±20	μA
I <sub>CC</sub>	supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	-	0.1	20	-	80	μA
ΔI <sub>CC</sub>	additional supply current	per input pin; V <sub>CC</sub> = 2.7 V to 3.6 V; V <sub>I</sub> = V <sub>CC</sub> − 0.6 V; I <sub>O</sub> = 0 A	-	5	500	-	5000	μA
C <sub>I</sub>	input capacitance	V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = GND to V <sub>CC</sub>	-	5.0	-	-	-	pF
I <sub>BHL</sub>	bus hold LOW current	V <sub>CC</sub> = 1.65; V <sub>I</sub> = 0.58 V <sup>[3][4]</sup>	10	-	-	10	-	μA
		V <sub>CC</sub> = 2.3; V <sub>I</sub> = 0.7 V	30	-	-	25	-	μA
		V <sub>CC</sub> = 3.0; V <sub>I</sub> = 0.8 V	75	-	-	60	-	μA
I <sub>BHH</sub>	bus hold HIGH current	V <sub>CC</sub> = 1.65; V <sub>I</sub> = 1.07 V <sup>[3][4]</sup>	−10	-	-	−10	-	μA
		V <sub>CC</sub> = 2.3; V <sub>I</sub> = 1.7 V	−30	-	-	−25	-	μA
		V <sub>CC</sub> = 3.0; V <sub>I</sub> = 2.0 V	−75	-	-	−60	-	μA
I <sub>BHLO</sub>	bus hold LOW overdrive current	V <sub>CC</sub> = 1.95 V <sup>[3][5]</sup>	200	-	-	200	-	μA
		V <sub>CC</sub> = 2.7 V	300	-	-	300	-	μA
		V <sub>CC</sub> = 3.6 V	500	-	-	500	-	μA
I <sub>BHHO</sub>	bus hold HIGH overdrive current	V <sub>CC</sub> = 1.95 V <sup>[3][5]</sup>	−200	-	-	−200	-	μA
		V <sub>CC</sub> = 2.7 V	−300	-	-	−300	-	μA
		V <sub>CC</sub> = 3.6 V	−500	-	-	−500	-	μA

[1] All typical values are measured at V<sub>CC</sub> = 3.3 V (unless stated otherwise) and T<sub>amb</sub> = 25 °C.

[2] The bus hold circuit is switched off when V<sub>I</sub> > V<sub>CC</sub> allowing 5.5 V on the input pin.

[3] Valid for data inputs (74LVCH162373A) only; control inputs do not have a bus hold circuit.

[4] The specified sustaining current at the data inputs holds the input below the specified V<sub>I</sub> level.

[5] The specified overdrive current at the data input forces the data input to the opposite logic input state.



## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 10](#).

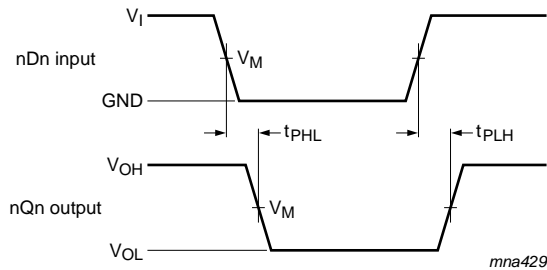
Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ <sup>[1]</sup>	Max	Min	Max	
t <sub>pd</sub>	propagation delay	nDn to nQn; see <a href="#">Figure 6</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	12	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.5	6.6	15.0	1.5	17.2	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	3.5	7.4	1.0	8.5	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.5	6.7	1.5	8.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.0	3.0	5.9	1.0	7.5	ns
		nLE to nQn; see <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 1.2 V	-	14	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.4	7.6	16.0	2.4	18.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	4.0	7.9	1.7	9.1	ns
t <sub>en</sub>	enable time	nOE to nQn; see <a href="#">Figure 8</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	18	-	-	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.7	7.1	15.6	1.7	17.9	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.5	4.0	8.2	1.5	9.4	ns
		V <sub>CC</sub> = 2.7 V	1.5	4.2	7.5	1.5	9.5	ns
t <sub>dis</sub>	disable time	nOE to nQn; see <a href="#">Figure 8</a> <sup>[2]</sup>						
		V <sub>CC</sub> = 1.2 V	-	11	-	-	-	ns
		V <sub>CC</sub> = 1.65 V	2.5	4.2	8.5	2.5	9.8	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.3	4.6	1.0	5.3	ns
		V <sub>CC</sub> = 2.7 V	1.5	3.2	4.8	1.5	6.0	ns
t <sub>w</sub>	pulse width	nLE HIGH; see <a href="#">Figure 7</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	5.0	-	-	5.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	4.0	-	-	4.0	-	ns
		V <sub>CC</sub> = 2.7 V	3.0	-	-	3.0	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	3.0	2.0	-	3.0	-	ns
t <sub>su</sub>	set-up time	nDn to nLE; see <a href="#">Figure 9</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	3.0	-	-	3.0	-	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	2.5	-	-	2.5	-	ns
		V <sub>CC</sub> = 2.7 V	2.0	-	-	2.0	-	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	1.0	-	2.0	-	ns

**Table 7. Dynamic characteristics ...continued**  
 Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 10](#).

Symbol	Parameter	Conditions	T <sub>amb</sub> = -40 °C to +85 °C			-40 °C to +125 °C		Unit	
			Min	Typ <sup>[1]</sup>	Max	Min	Max		
t <sub>h</sub>	hold time	nDn to nLE; see <a href="#">Figure 9</a>							
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.5	-	-	2.5	-	ns	
		V <sub>CC</sub> = 2.3 V to 2.7 V	2.0	-	-	2.0	-	ns	
		V <sub>CC</sub> = 2.7 V	0.9	-	-	0.9	-	ns	
		V <sub>CC</sub> = 3.0 V to 3.6 V	+0.9	-1.0	-	+0.9	-	ns	
t <sub>sk(o)</sub>	output skew time	V <sub>CC</sub> = 3.0 V to 3.6 V	<a href="#">[3]</a>	-	-	1.0	-	1.5	ns
C <sub>PD</sub>	power dissipation capacitance	per input; V <sub>I</sub> = GND to V <sub>CC</sub>	<a href="#">[4]</a>						
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	10.8	-	-	-	pF	
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	13.0	-	-	-	pF	
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	15.0	-	-	-	pF	

- [1] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.8 V, 2.5 V, 2.7 V and 3.3 V respectively.
- [2] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.  
 t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.  
 t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.
- [3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [4] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz  
 C<sub>L</sub> = output load capacitance in pF  
 V<sub>CC</sub> = supply voltage in Volts  
 N = number of inputs switching  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs

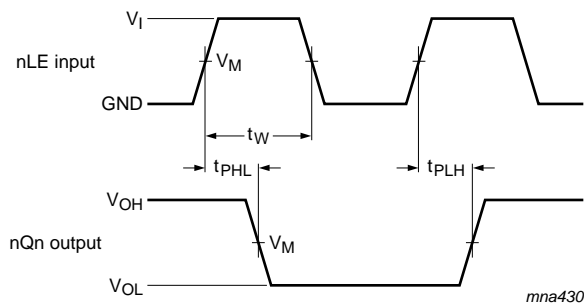
## 11. AC waveforms



Measurement points are given in [Table 8](#).

$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

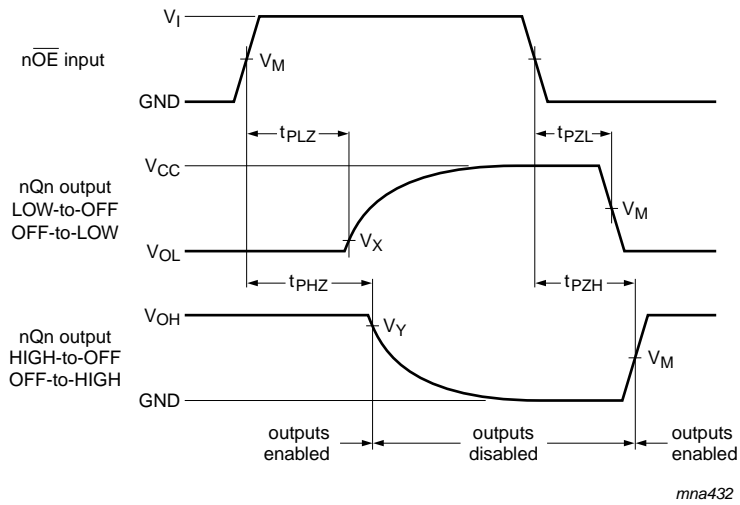
**Fig 6. Input (nDn) to output (nQn) propagation delays**



Measurement points are given in [Table 8](#).

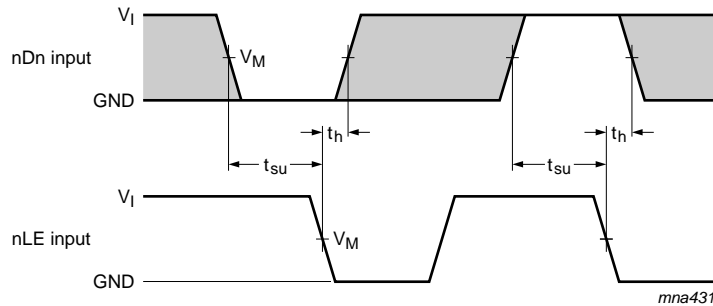
$V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 7. Latch enable (nLE) pulse width, and the latch enable input to output (nQn) propagation delays**



Measurement points are given in [Table 8](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 8. 3-state enable and disable times**

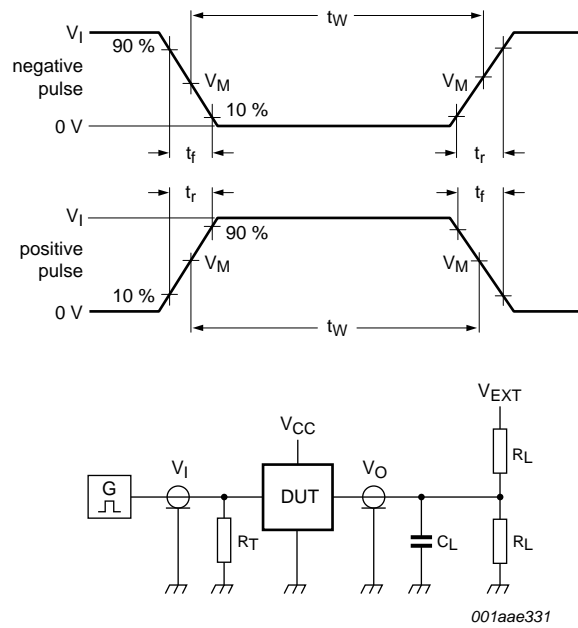


Measurement points are given in [Table 8](#). The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig 9. Data set-up and hold times for the nDn input to the nLE input**

**Table 8. Measurement points**

Supply voltage	Input		Output		
	$V_I$	$V_M$	$V_M$	$V_X$	$V_Y$
1.2 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.65 V to 1.95 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	$V_{CC}$	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 10. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 kΩ	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	$\leq 2.5$ ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	$\leq 2.5$ ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

## 12. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1

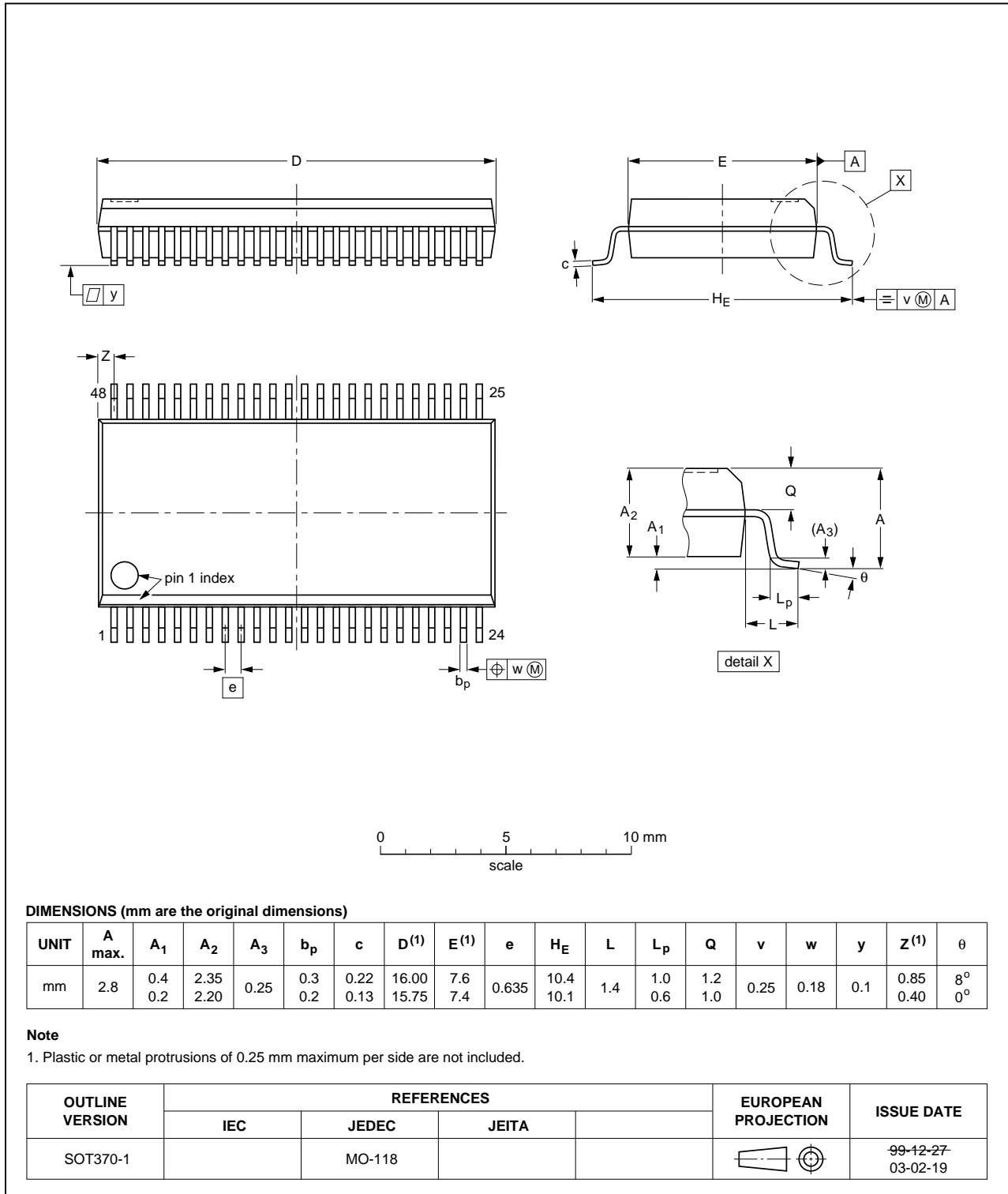


Fig 11. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

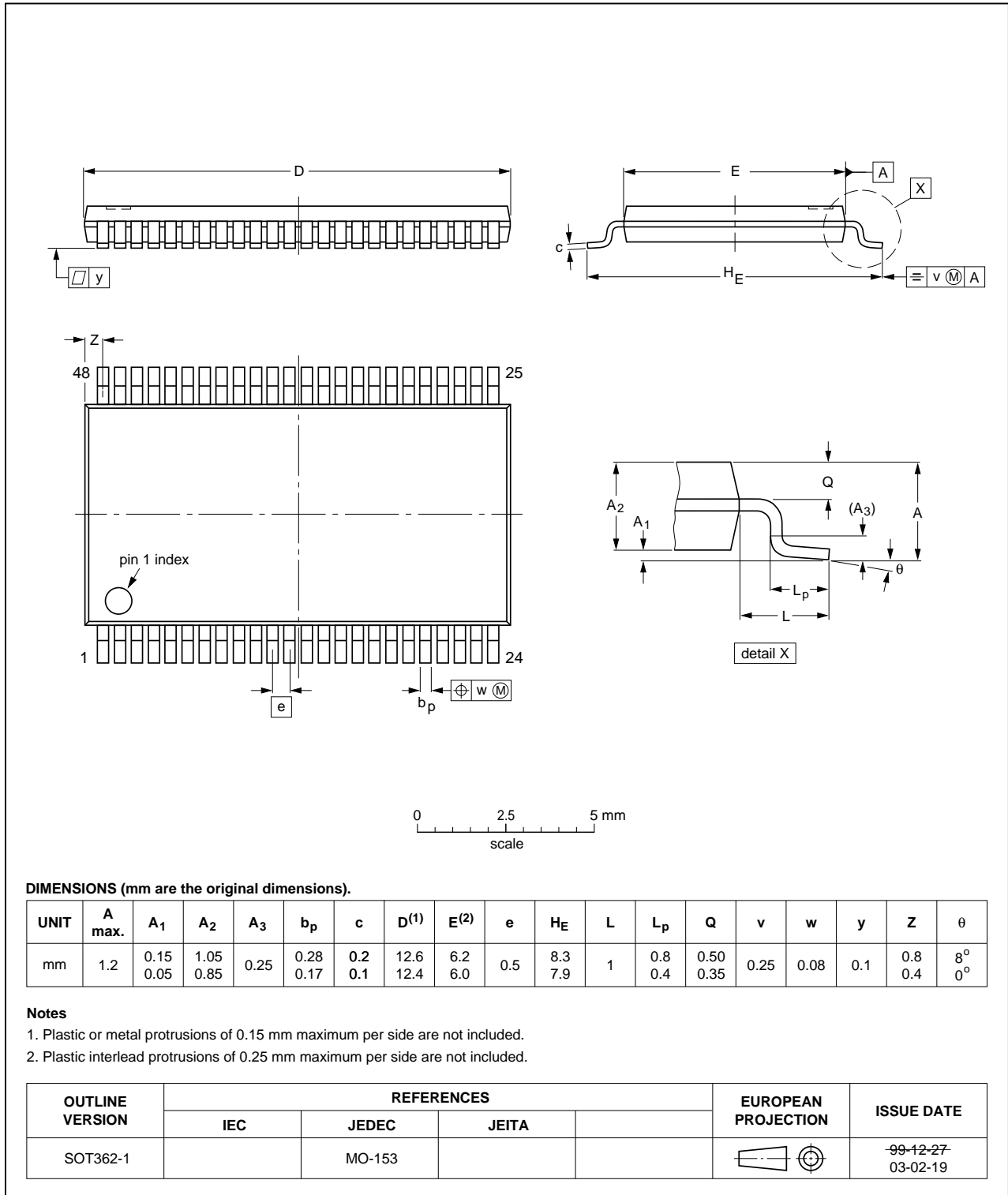


Fig 12. Package outline SOT362-1 (TSSOP48)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC_LVCH162373A v.4	20130514	Product data sheet	-	74LVC_LVCH162373A v.3
Modifications:	<ul style="list-style-type: none"> <li>• Typenumbers: 74LVC162373ADGG and 74LVC162373ADL added.</li> </ul>			
74LVC_LVCH162373A v.3	20130118	Product data sheet	-	74LVC_LVCH162373A v.2
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Table 5</a>, <a href="#">Table 6</a>, <a href="#">Table 7</a>, <a href="#">Table 8</a> and <a href="#">Table 9</a>: values added for lower voltage ranges.</li> </ul>			
74LVC_LVCH162373A v.2	20040205	Product specification	-	74LVC_LVCH162373A v.1
74LVC_LVCH162373A v.1	19980805	Product specification	-	-



## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 15.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 15.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 16. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 17. Contents

<b>1</b>	<b>General description</b> .....	<b>1</b>
<b>2</b>	<b>Features and benefits</b> .....	<b>1</b>
<b>3</b>	<b>Ordering information</b> .....	<b>2</b>
<b>4</b>	<b>Functional diagram</b> .....	<b>2</b>
<b>5</b>	<b>Pinning information</b> .....	<b>4</b>
5.1	Pinning .....	4
5.2	Pin description .....	4
<b>6</b>	<b>Functional description</b> .....	<b>5</b>
<b>7</b>	<b>Limiting values</b> .....	<b>5</b>
<b>8</b>	<b>Recommended operating conditions</b> .....	<b>6</b>
<b>9</b>	<b>Static characteristics</b> .....	<b>6</b>
<b>10</b>	<b>Dynamic characteristics</b> .....	<b>8</b>
<b>11</b>	<b>AC waveforms</b> .....	<b>10</b>
<b>12</b>	<b>Package outline</b> .....	<b>13</b>
<b>13</b>	<b>Abbreviations</b> .....	<b>15</b>
<b>14</b>	<b>Revision history</b> .....	<b>15</b>
<b>15</b>	<b>Legal information</b> .....	<b>16</b>
15.1	Data sheet status .....	16
15.2	Definitions .....	16
15.3	Disclaimers .....	16
15.4	Trademarks .....	17
<b>16</b>	<b>Contact information</b> .....	<b>17</b>
<b>17</b>	<b>Contents</b> .....	<b>18</b>

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2013.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 14 May 2013

Document identifier: 74LVC\_LVCH162373A