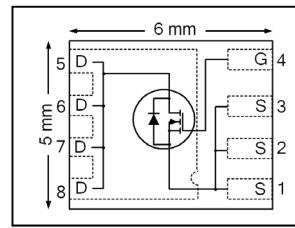


**Application**

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

HEXFET® Power MOSFET



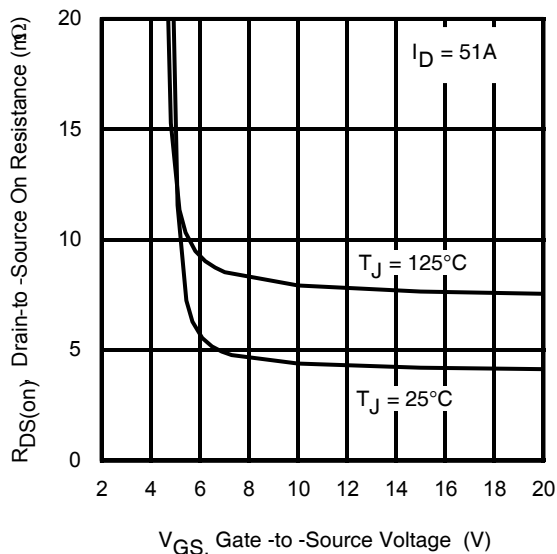
<b>V<sub>DSS</sub></b>	<b>60V</b>
<b>R<sub>DS(on)</sub> typ.</b>	<b>4.3mΩ</b>
	<b>max</b>
<b>I<sub>D</sub></b>	<b>85A</b>

**Benefits**

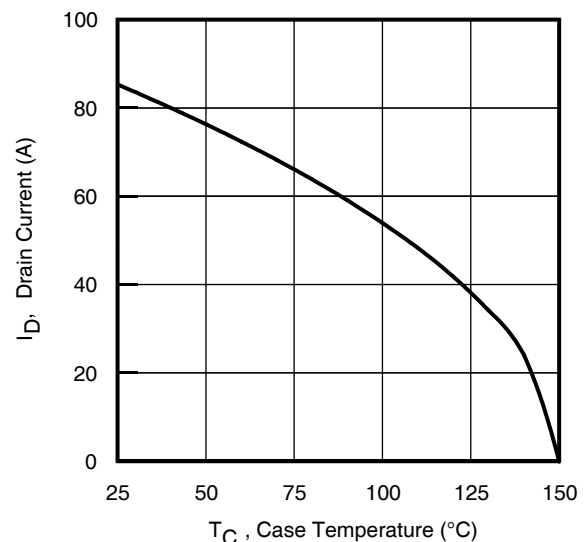
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant



Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFH7545PbF	PQFN 5mm x 6mm	Tape and Reel	4000	IRFH7545TRPbF



**Fig 1.** Typical On-Resistance vs. Gate Voltage



**Fig 2.** Maximum Drain Current vs. Case Temperature

**Absolute Maximum Rating**

Symbol	Parameter	Max.	Units
$I_D @ T_{C(Bottom)} = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	85	A
$I_D @ T_{C(Bottom)} = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	54	
$I_{DM}$	Pulsed Drain Current ①	340	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	83	W
	Linear Derating Factor	0.67	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	°C

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ②	102	mJ
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ③	160	
$I_{AR}$	Avalanche Current ①	See Fig 15, 16, 23a, 23b	A
$E_{AR}$	Repetitive Avalanche Energy ①		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ⑦	—	1.5	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ⑦	—	22	
$R_{\theta JA}$	Junction-to-Ambient ⑨	—	34	
$R_{\theta JA}$ (<10s)	Junction-to-Ambient ⑨	—	23	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	49	—	mV/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	4.3	5.2	mΩ	$V_{GS} = 10\text{V}, I_D = 51\text{A}$
		—	6.0	—		$V_{GS} = 6.0\text{V}, I_D = 26\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.1	—	3.7	V	$V_{DS} = V_{GS}, I_D = 100\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 60\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
$R_G$	Gate Resistance	—	2.5	—	Ω	

**Notes:**

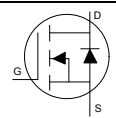
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 78\mu\text{H}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 51\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ③  $I_{SD} \leq 51\text{A}$ ,  $di/dt \leq 1212\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑧ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 18\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ⑨ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:

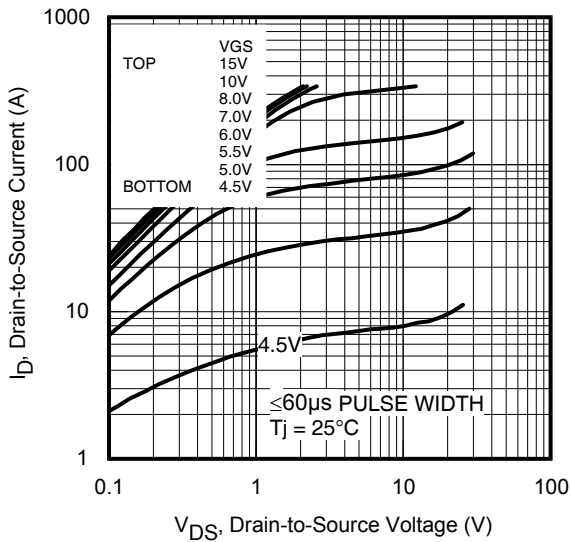
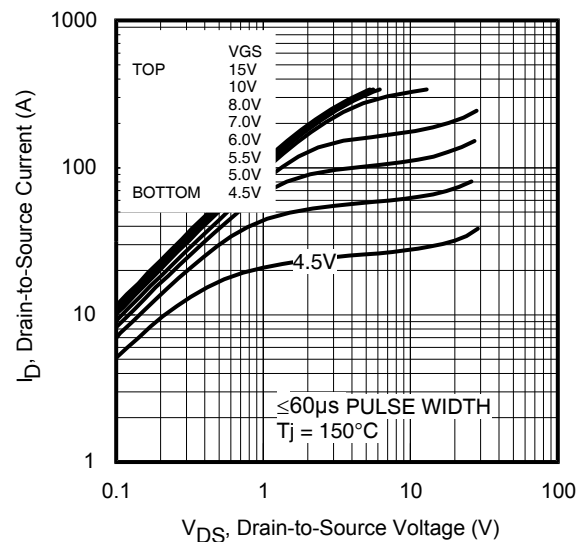
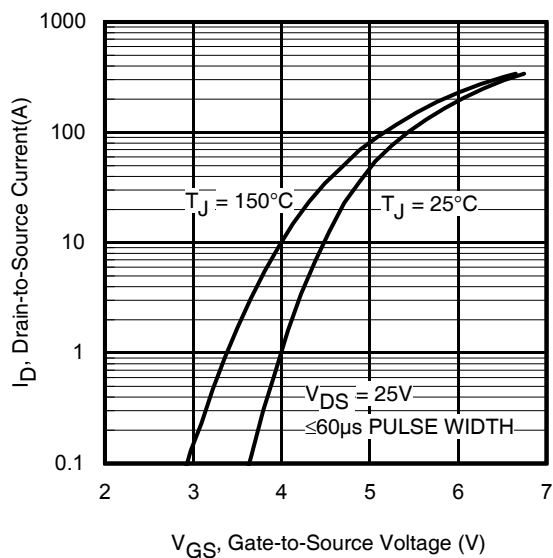
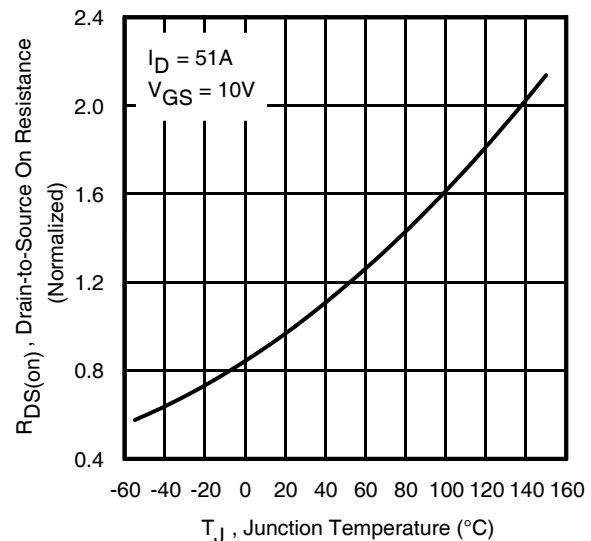
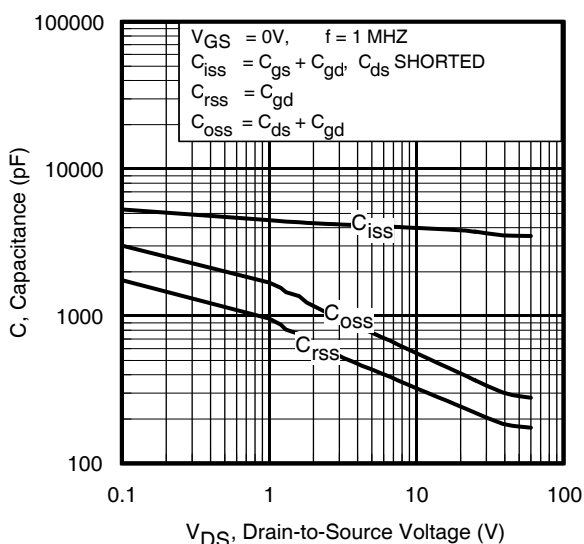
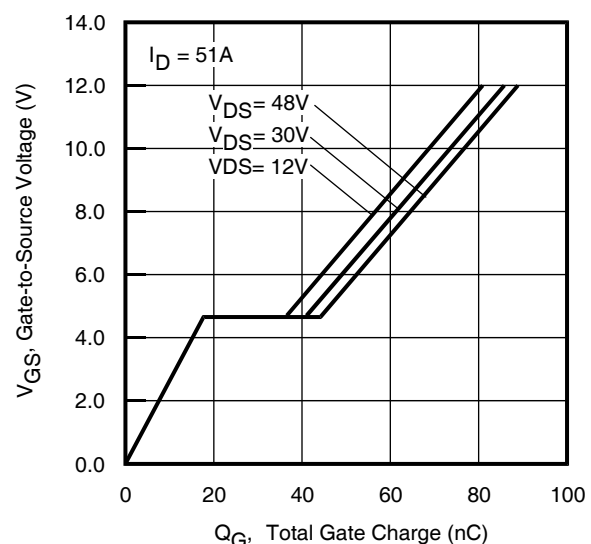
<http://www.irf.com/technical-info/appnotes/an-994.pdf>

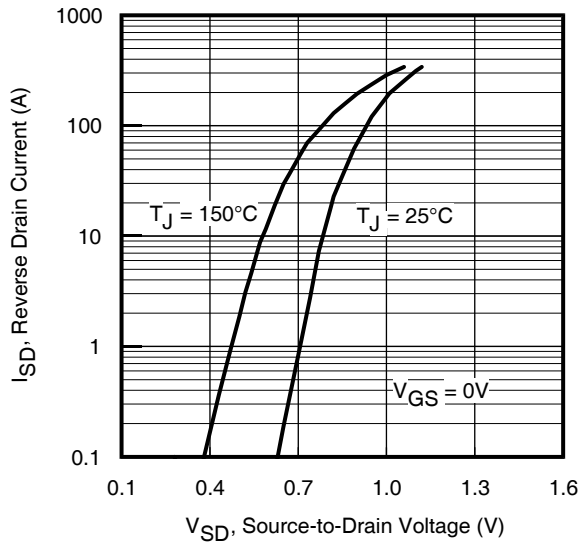
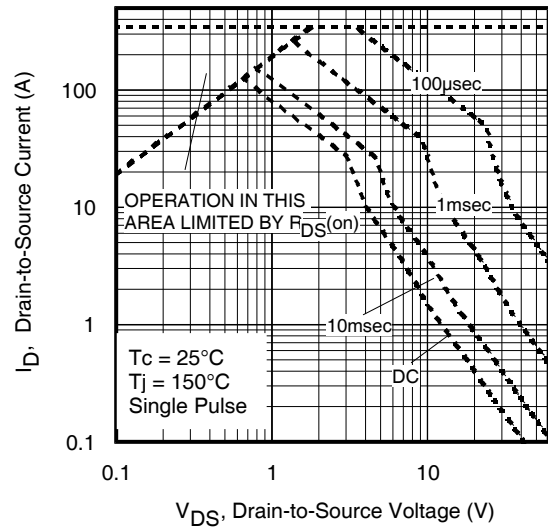
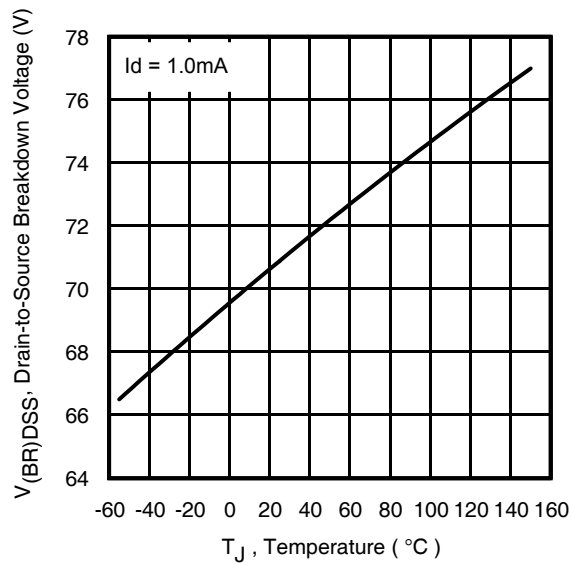
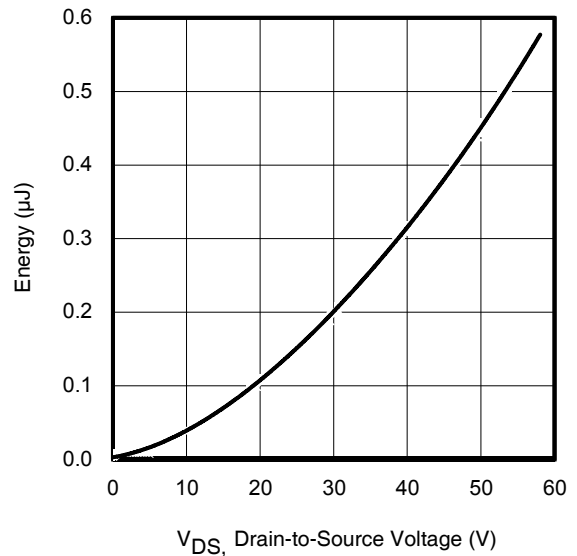
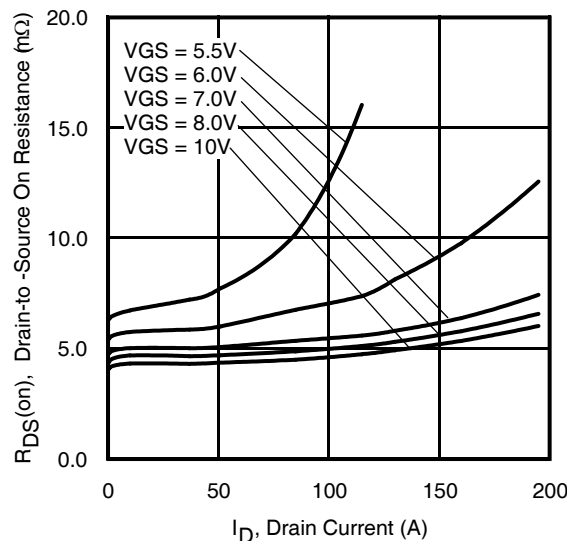
**Dynamic Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

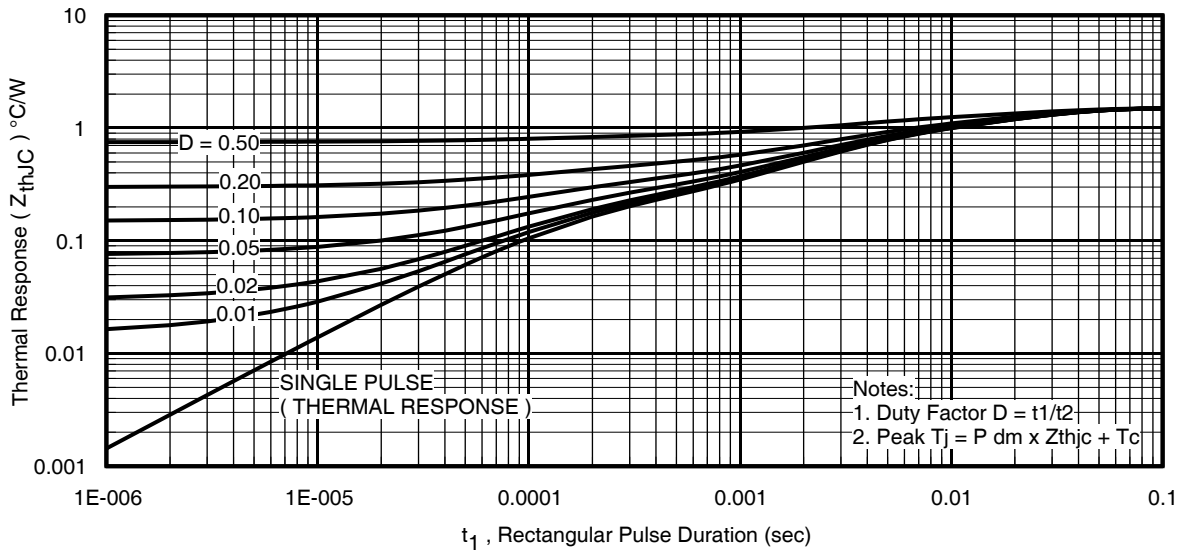
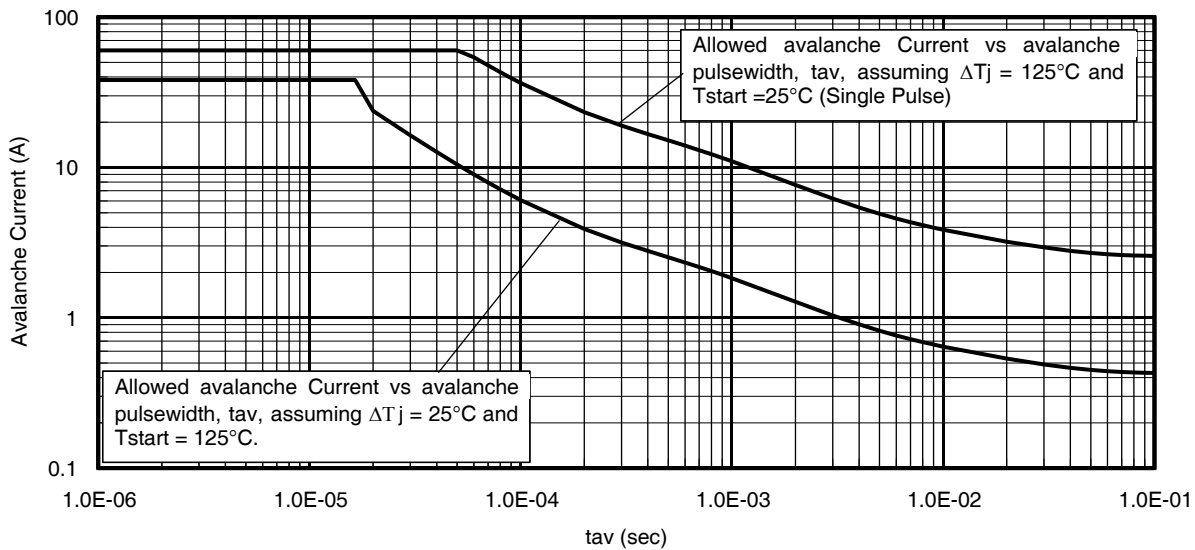
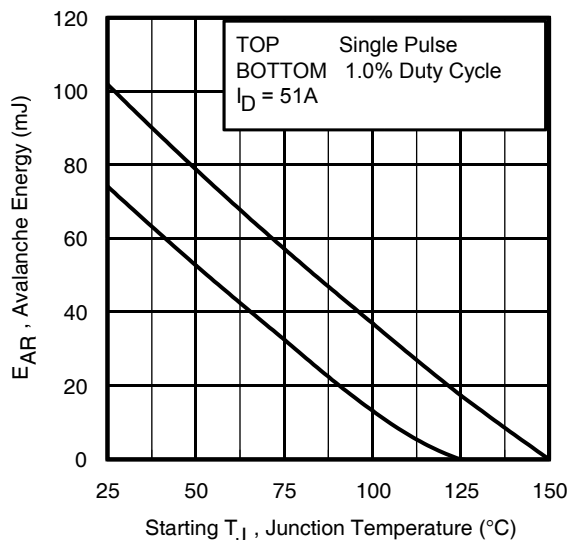
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	140	—	—	S	$V_{DS} = 10\text{V}, I_D = 51\text{A}$
$Q_g$	Total Gate Charge	—	73	110	nC	$I_D = 51\text{A}$ $V_{DS} = 30\text{V}$ $V_{GS} = 10\text{V}$
$Q_{gs}$	Gate-to-Source Charge	—	19	—		
$Q_{gd}$	Gate-to-Drain Charge	—	22	—		
$Q_{sync}$	Total Gate Charge Sync. ( $Q_g - Q_{gd}$ )	—	51	—		
$t_{d(on)}$	Turn-On Delay Time	—	8.6	—	ns	$V_{DD} = 30\text{V}$ $I_D = 51\text{A}$ $R_G = 2.7\Omega$ $V_{GS} = 10\text{V}$ ④
$t_r$	Rise Time	—	26	—		
$t_{d(off)}$	Turn-Off Delay Time	—	43	—		
$t_f$	Fall Time	—	16	—		
$C_{iss}$	Input Capacitance	—	3890	—	pF	$V_{GS} = 0\text{V}$ $V_{DS} = 25\text{V}$ $f = 1.0\text{MHz}$ , See Fig.7 $V_{GS} = 0\text{V}, V_{DS} = 0\text{V to } 48\text{V}$ ⑥ $V_{GS} = 0\text{V}, V_{DS} = 0\text{V to } 48\text{V}$ ⑤
$C_{oss}$	Output Capacitance	—	365	—		
$C_{riss}$	Reverse Transfer Capacitance	—	220	—		
$C_{oss\text{ eff.}(ER)}$	Effective Output Capacitance (Energy Related)	—	370	—		
$C_{oss\text{ eff.}(TR)}$	Output Capacitance (Time Related)	—	470	—		

**Diode Characteristics**

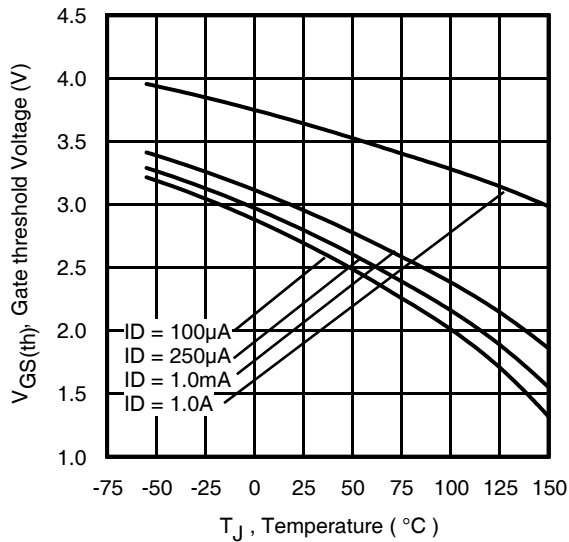
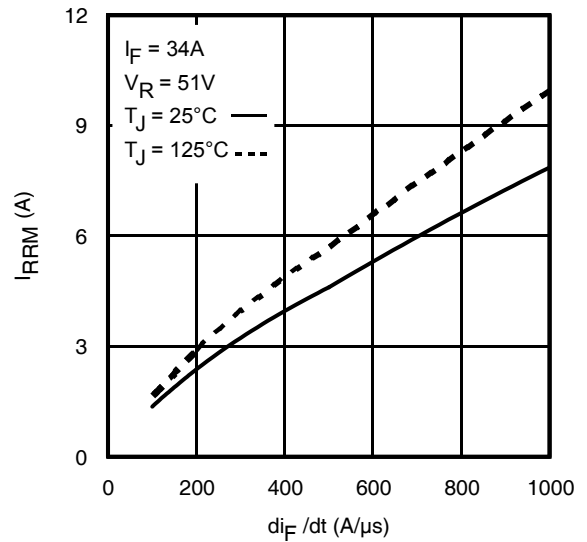
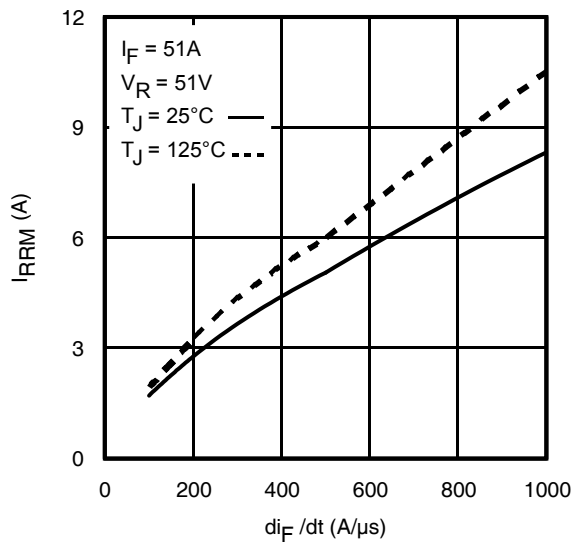
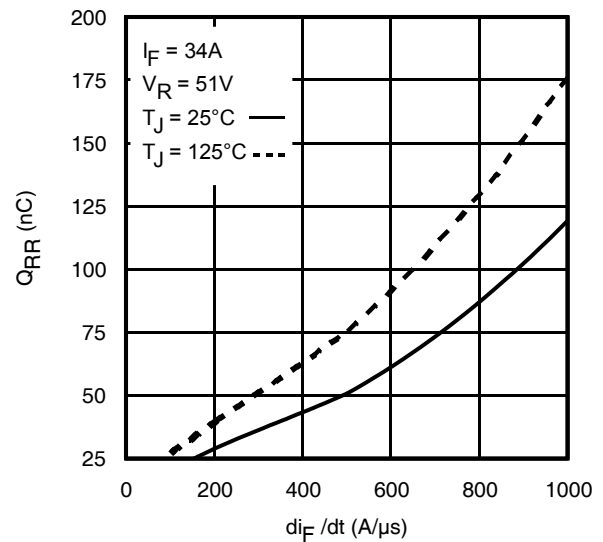
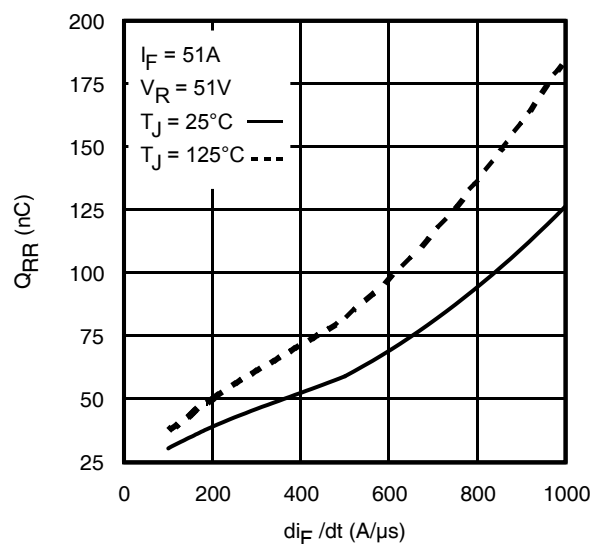
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	85	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	340		
$V_{SD}$	Diode Forward Voltage	—	—	1.2	V	$T_J = 25^\circ\text{C}, I_S = 51\text{A}, V_{GS} = 0\text{V}$ ④
$dv/dt$	Peak Diode Recovery $dv/dt$ ④	—	8.1	—	V/ns	$T_J = 150^\circ\text{C}, I_S = 51\text{A}, V_{DS} = 60\text{V}$ ④
$t_{rr}$	Reverse Recovery Time	—	32	—	ns	$T_J = 25^\circ\text{C}$ $V_{DD} = 51\text{V}$ $T_J = 125^\circ\text{C}$ $I_F = 51\text{A}$ , $T_J = 25^\circ\text{C}$ $di/dt = 100\text{A}/\mu\text{s}$ ④ $T_J = 125^\circ\text{C}$
		—	34	—		
$Q_{rr}$	Reverse Recovery Charge	—	30	—	nC	$T_J = 25^\circ\text{C}$ $T_J = 125^\circ\text{C}$
		—	38	—		
$I_{RRM}$	Reverse Recovery Current	—	1.7	—	A	$T_J = 25^\circ\text{C}$

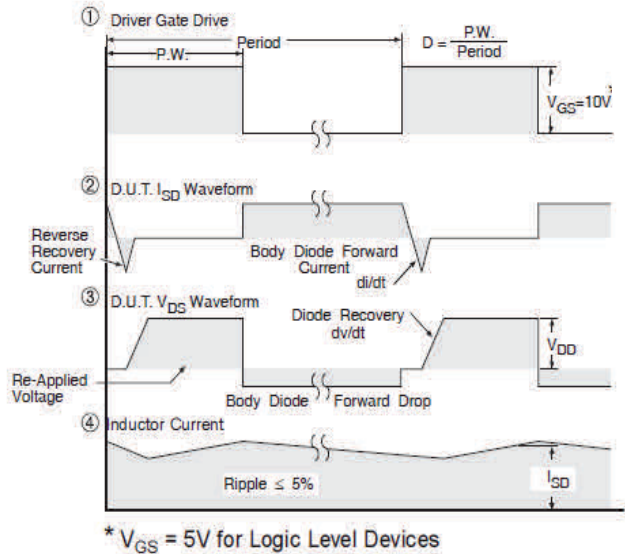
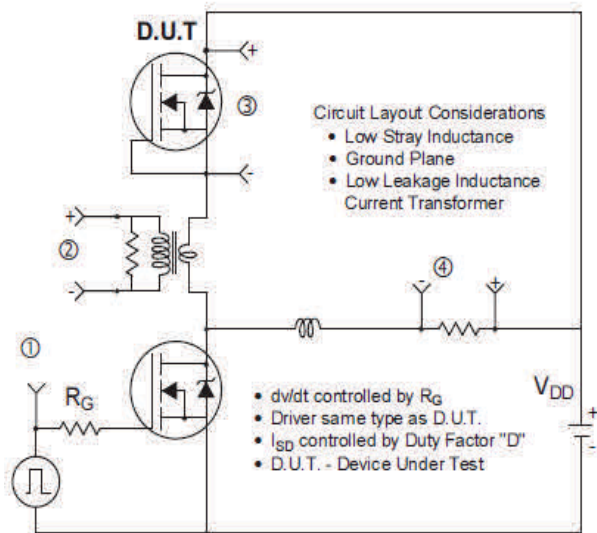
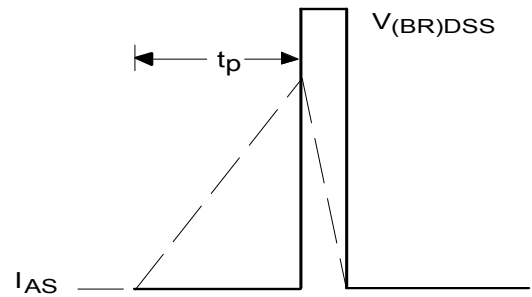
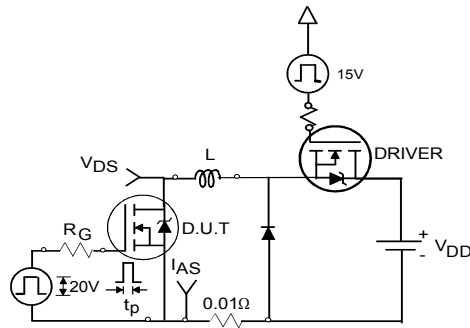
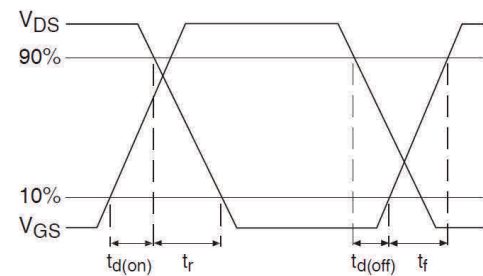
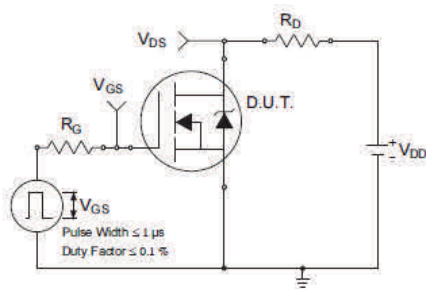
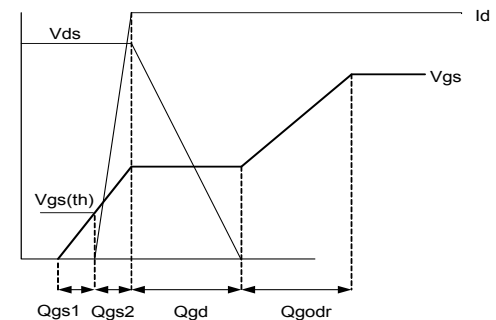
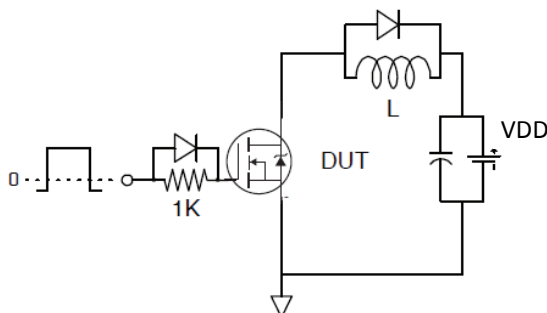

**Fig 3. Typical Output Characteristics**

**Fig 4. Typical Output Characteristics**

**Fig 5. Typical Transfer Characteristics**

**Fig 6. Normalized On-Resistance vs. Temperature**

**Fig 7. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 9.** Typical Source-Drain Diode Forward Voltage

**Fig 10.** Maximum Safe Operating Area

**Fig 11.** Drain-to-Source Breakdown Voltage

**Fig 12.** Typical  $C_{oss}$  Stored Energy

**Fig 13.** Typical On-Resistance vs. Drain Current

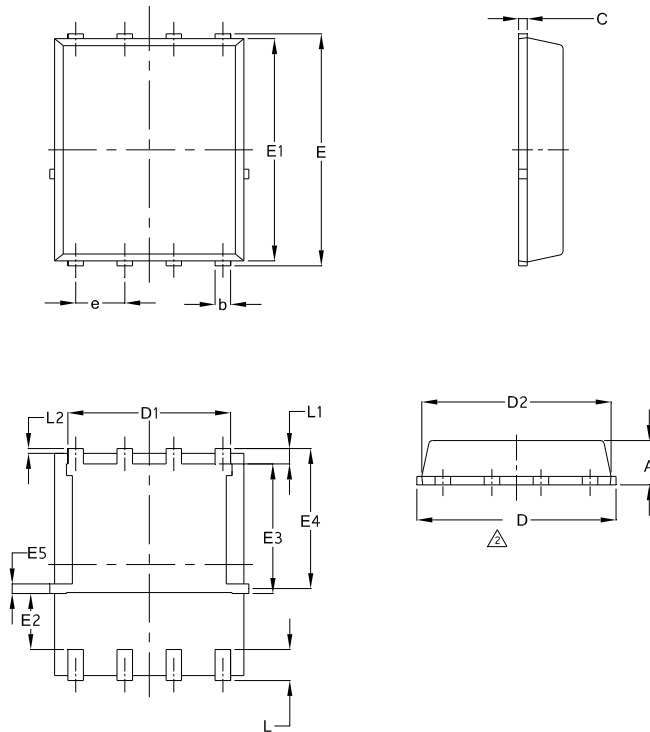

**Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 15. Avalanche Current vs. Pulse Width**

**Fig 16. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)  
 $P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$   
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$   
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$


**Fig 17.** Threshold Voltage vs. Temperature

**Fig 18.** Typical Recovery Current vs.  $di_F/dt$ 

**Fig 19.** Typical Recovery Current vs.  $di_F/dt$ 

**Fig 20.** Typical Stored Charge vs.  $di_F/dt$ 

**Fig 21.** Typical Stored Charge vs.  $di_F/dt$


**Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs**

**Fig 23a. Unclamped Inductive Test Circuit**
**Fig 23b. Unclamped Inductive Waveforms**

**Fig 24a. Switching Time Test Circuit**
**Fig 24b. Switching Time Waveforms**

**Fig 25a. Gate Charge Test Circuit**
**Fig 25b. Gate Charge Waveform**

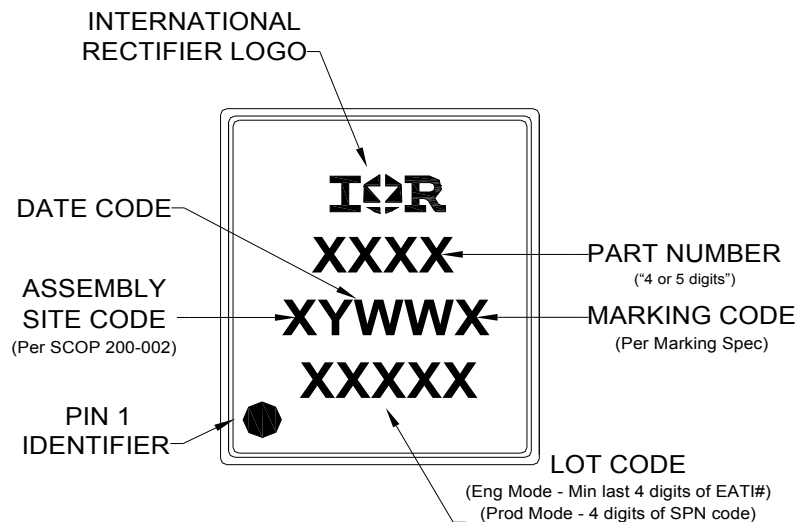


**PQFN 5x6 Outline "E" Package Details**


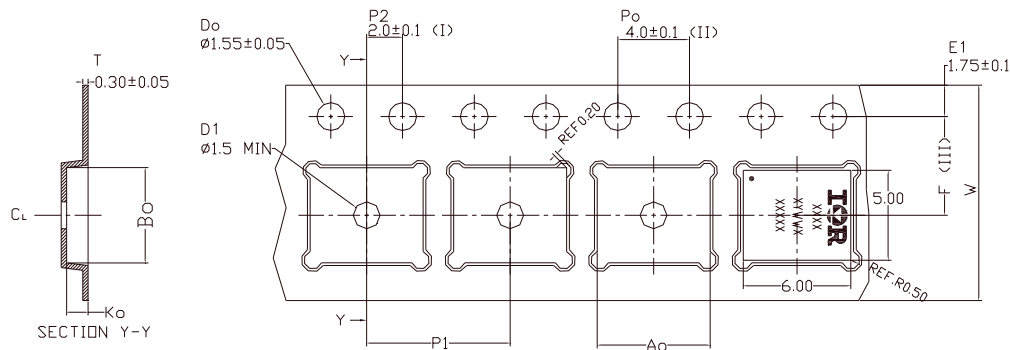
SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	0.90	1.17	0.0354	0.0461
b	0.31	0.51	0.0130	0.0189
C	0.195	0.300	0.0077	0.0118
D	4.80	5.25	0.1890	0.2028
D1	3.91	4.31	0.1539	0.1697
D2	4.80	5.10	0.1890	0.1968
E	5.90	6.25	0.2323	0.2421
E1	5.65	6.15	0.2224	0.2362
E2	1.10	—	0.0594	—
E3	3.32	3.78	0.1307	0.1480
E4	3.52	3.72	0.1346	0.1409
E5	0.13	0.32	0.0071	0.0126
e	1.27	BSC	0.050	BSC
L	0.51	0.86	0.0200	0.0098
L1	0.38	0.71	0.0150	0.0260
L2	0.05	0.25	0.0201	0.0339
l	0	0.18	0	0.0071

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

**PQFN 5x6 Outline "E" Part Marking**


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**PQFN Tape and Reel**


Ao	6.30 +/- 0.1
Bo	5.30 +/- 0.1
Ko	1.20 +/- 0.1
F	5.50 +/- 0.1
P1	8.00 +/- 0.1
W	12.00 +/- 0.3

- (I) Measured from centerline of sprocket hole to centerline of pocket.
- (II) Cumulative tolerance of 10 sprocket hole is ±0.20.
- (III) Measured from centerline of sprocket hole to centerline of pocket.
- (IV) Other material available.
- (V) Typical SR of Form tape Max 10<sup>9</sup> DHM/SQ.

ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE STATED.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F <sup>††</sup> guidelines)	
<b>Moisture Sensitivity Level</b>	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D <sup>††</sup> )
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability>

†† Applicable version of JEDEC standard at the time of product release.

**Revision History**

Date	Comments
8/21/2014	• Updated data sheet with latest PQFN Tape and Reel on page 10.
11/7/2014	• Updated E <sub>AS</sub> (L=1mH) = 160mJ on page 2 • Updated note 8 "Limited by T <sub>Jmax</sub> , starting T <sub>J</sub> = 25°C, L = 1mH, R <sub>G</sub> = 50Ω, I <sub>AS</sub> = 18A, V <sub>GS</sub> = 10V" on page 2