AT91SAM9G20-EK Evaluation Board

User Guide

6413C–ATARM–18-Feb-09

Table of Contents

Section 1

Overview

1.1 Scope

The AT91SAM9G20-EK Evaluation Kit enables the evaluation of and code development for applications running on an AT91SAM9G20 device. This guide focuses on the AT91SAM9G20-EK board as an evaluation platform. The board supports the AT91SAM9G20 in a 217-ball LFBGA RoHS-compliant Package.

1.2 Deliverables

The AT91SAM9G20-EK package contains the following items:

- an AT91SAM9G20-EK board
- a universal input AC/DC power supply with US and Europe plug adapter
- one A/B-type USB cable
- one serial RS232 cable
- one RJ45 crossed Ethernet cable
- one CD-ROM that allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly
- one 3V Lithium battery

1.3 AT91SAM9G20-EK Evaluation Board

The board is equipped with an AT91SAM9G20 microcontroller together with the following:

- 64 Mbytes of SDRAM memory
- 256 Mbytes of NAND Flash memory
- one Atmel® serial DataFlash®
- one Atmel TWI serial EEPROM
- one USB Device port interface
- two USB Host port interfaces
- one DBGU serial communication port
- one complete MODEM serial communication port
- one additional serial communication port with RTS/CTS handshake control
- JTAG/ICE debug interface
- one PHY Ethernet 100-base TX with three status LEDs
- one on-board Audio DAC
- one Power LED and one general-purpose LED

- two user-input push buttons
- one Wakeup-input push button
- one reset push button
- two DataFlash SD/MMC card slots
- four expansion connectors (PIOA, PIOB, PIOC, IMAGE SENSOR)
- one BGA-like EBI expansion footprint connector
- one Lithium Coin Cell Battery Retainer for 12 mm cell size

Section 2

Setting Up the AT91SAM9G20-EK Board

2.1 Electrostatic Warning

The AT91SAM9G20-EK evaluation board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

In order to set up the AT91SAM9G20-EK evaluation board, the following items are needed:

- the AT91SAM9G20-EK evaluation board itself,
- AC/DC power adapter (5V at 2A), 2.1 mm by 5.5 mm.

2.3 Layout

Figure 2-1. Top View

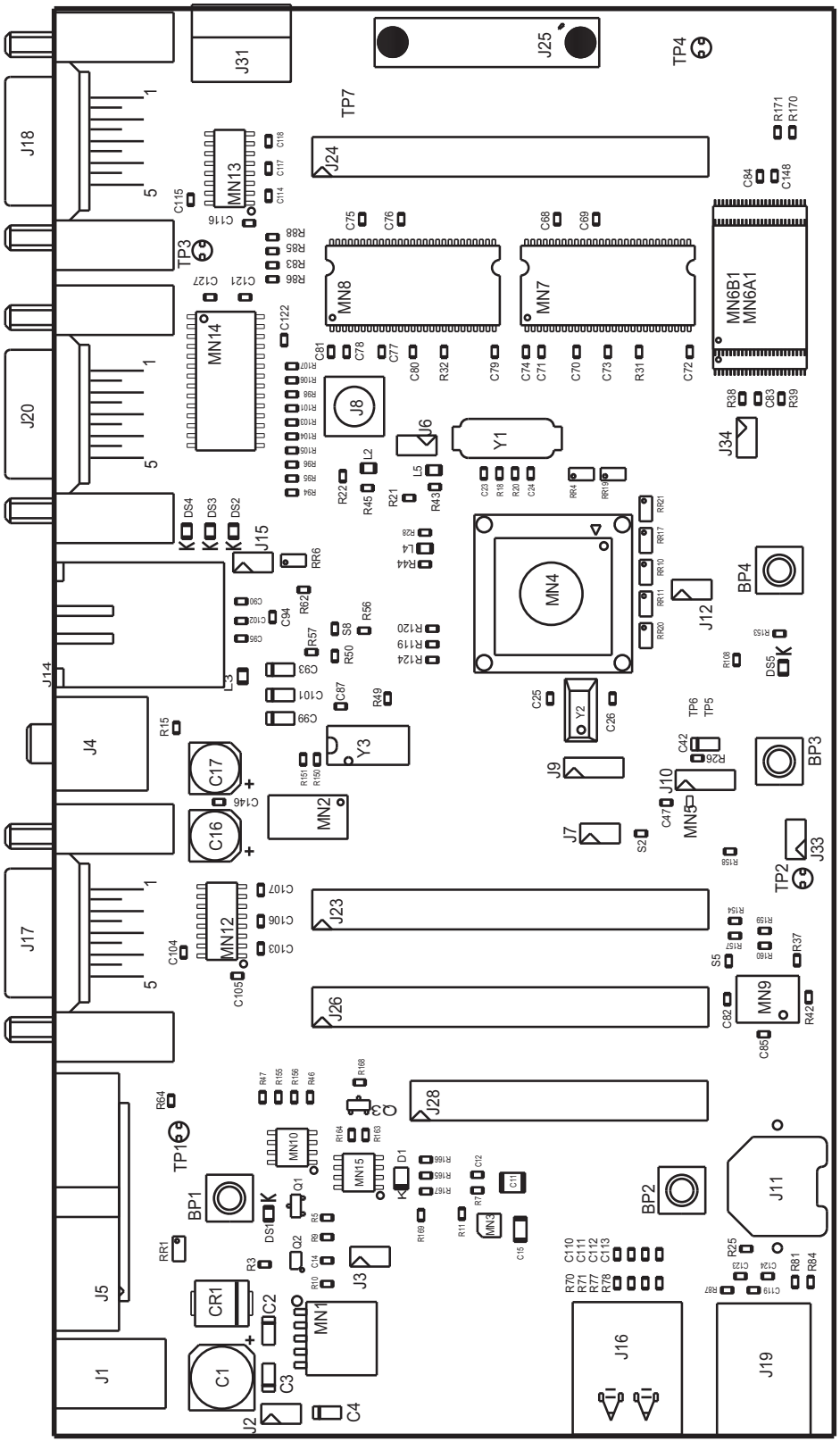
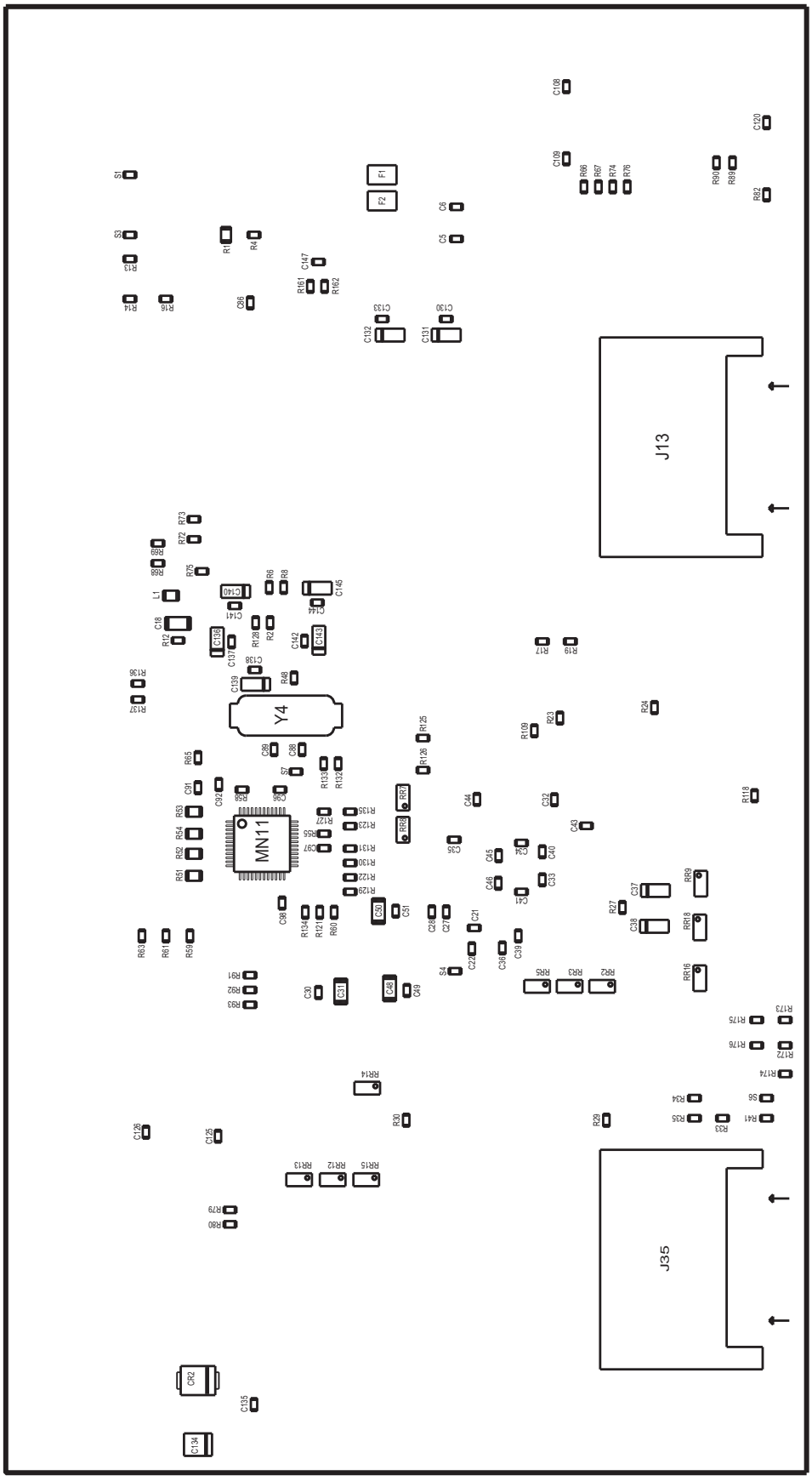


Figure 2-2. Bottom View



2.4 Powering Up the Board

The AT91SAM9G20-EK requires 5V DC (±5%). DC power is supplied to the board via the 2.1 mm by 5.5 mm socket J1. Coaxial plug center positive standard.

2.5 Backup Power Supply

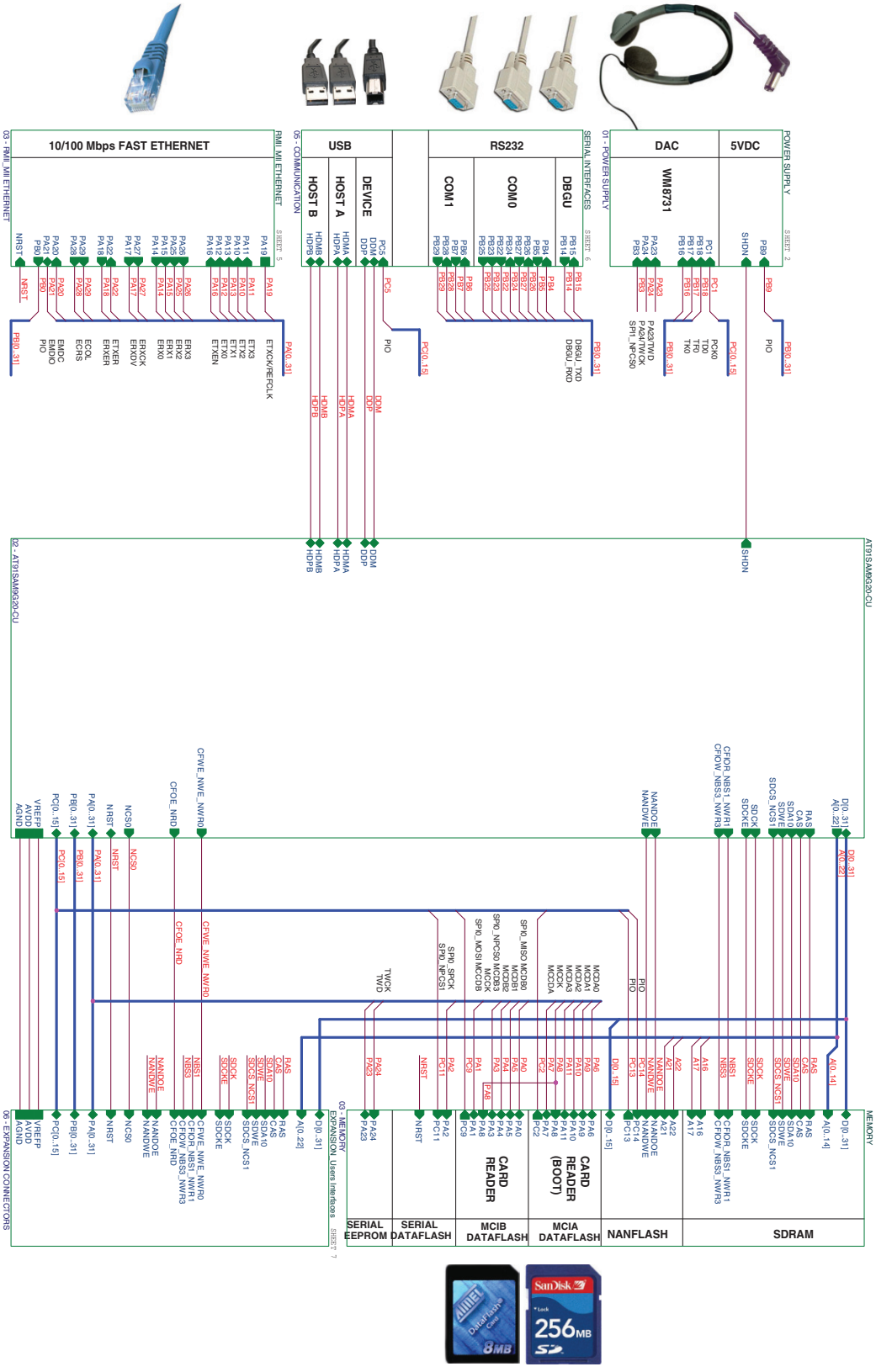
The user can plug in a battery (3V Lithium Battery CR1225 or equivalent) in order to permanently power the backup part of the device. In this case, J10 configuration must be set in position 1, 2. Refer to Section 4.1 ”Jumpers”.

2.6 Getting Started

The AT91SAM9G20-EK evaluation board is delivered with a CD-ROM containing all necessary information and step-by-step procedures for working with the most common development tools.

2.7 AT91SAM9G20-EK Block Diagram

Figure 2-3. AT91SAM9G20-EK Block Diagram



Section 3

Board Description

3.1 AT91SAM9G20 Microcontroller

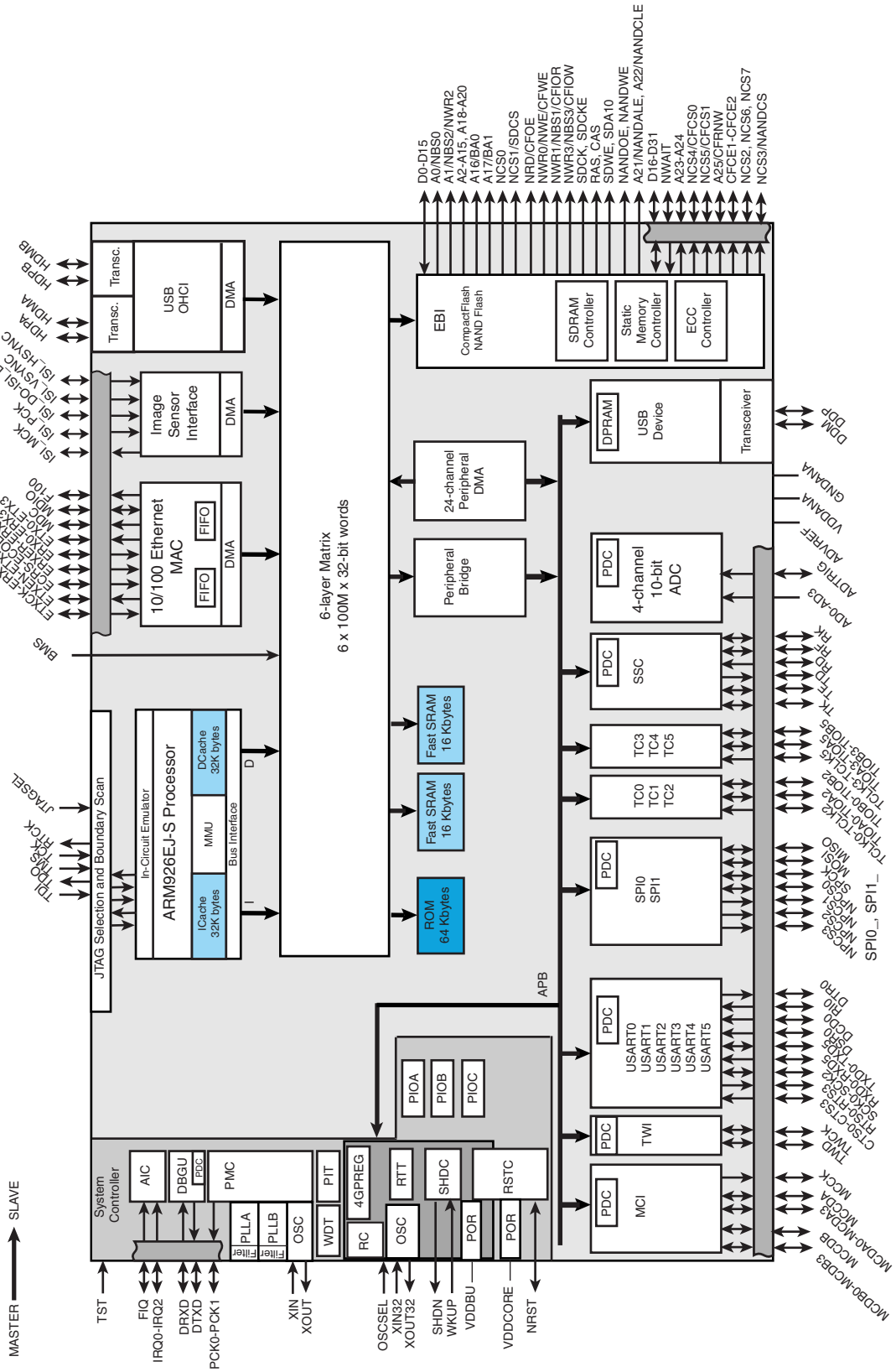
- Incorporates the ARM926EJ-S™ ARM® Thumb® Processor
  - DSP Instruction Extensions, ARM Jazelle® Technology for Java® Acceleration
  - 32-KByte Data Cache, 32-KByte Instruction Cache, Write Buffer
  - CPU Frequency 400 MHz
  - Memory Management Unit
  - EmbeddedICE™, Debug Communication Channel Support
- Additional Embedded Memories
  - One 64-KByte Internal ROM, Single-cycle Access at Maximum Matrix Speed
  - Two 16-KByte Internal SRAM, Single-cycle Access at Maximum Matrix Speed
- External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, ECC-enabled NAND Flash and CompactFlash®
- USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, 2,432-byte Configurable Integrated DPRAM
- USB 2.0 Full Speed (12 Mbits per second) Host and Double Port
  - Single or Dual On-chip Transceivers
  - Integrated FIFOs and Dedicated DMA Channels
- Ethernet MAC 10/100 Base T
  - Media Independent Interface or Reduced Media Independent Interface
  - 128-byte FIFOs and Dedicated DMA Channels for Receive and Transmit
- Image Sensor Interface
  - ITU-R BT. 601/656 External Interface, Programmable Frame Capture Rate
  - 12-bit Data Interface for Support of High Sensibility Sensors
  - SAV and EAV Synchronization, Preview Path with Scaler, YCbCr Format
- Bus Matrix
  - Six 32-bit-layer Matrix
  - Boot Mode Select Option, Remap Command
- Fully-featured System Controller, including
  - Reset Controller, Shutdown Controller
  - Four 32-bit Battery Backup Registers for a Total of 16 Bytes
  - Clock Generator and Power Management Controller
  - Advanced Interrupt Controller and Debug Unit
  - Periodic Interval Timer, Watchdog Timer and Real-time Timer
- Reset Controller (RSTC)
  - Based on a Power-on Reset Cell, Reset Source Identification and Reset Output Control
- Clock Generator (CKGR)
  - Selectable 32,768 Hz Low-power Oscillator or Internal Low Power RC Oscillator on Battery Backup Power Supply, Providing a Permanent Slow Clock
  - 3 to 20 MHz On-chip Oscillator, One up to 800 MHz PLL and One up to 100 MHz PLL

- Power Management Controller (PMC)
  - Very Slow Clock Operating Mode, Software Programmable Power Optimization Capabilities
  - Two Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Three External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - 2-wire UART and Support for Debug Communication Channel, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - 20-bit Interval Timer plus 12-bit Interval Counter
- Watchdog Timer (WDT)
  - Key-protected, Programmable Only Once, Windowed 16-bit Counter Running at Slow Clock
- Real-time Timer (RTT)
  - 32-bit Free-running Backup Counter Running at Slow Clock with 16-bit Prescaler
- One 4-channel 10-bit Analog-to-Digital Converter
- Three 32-bit Parallel Input/Output Controllers (PIOA, PIOB, PIOC)
  - 96 Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
  - All I/O Lines are Schmitt Trigger Inputs
- Peripheral DMA Controller Channels (PDC)
- One Two-slot MultiMedia Card Interface (MCI)
  - SDCard/SDIO and MultiMediaCard™ Compliant
  - Automatic Protocol Control and Fast Automatic Data Transfers with PDC
- One Synchronous Serial Controller (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Four Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation, Manchester Encoding/Decoding
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Full Modem Signal Control on USART0
- Two 2-wire UARTs
- Two Master/Slave Serial Peripheral Interfaces (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
  - Synchronous Communications
- Two Three-channel 16-bit Timer/Counters (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
  - High-Drive Capability on Outputs TIOA0, TIOA1, TIOA2
- One Two-wire Interface (TWI)
  - Compatible with Standard Two-wire Serial Memories
  - One, Two or Three Bytes for Slave Address
  - Sequential Read/Write Operations
  - Master, Multi-master and Slave Mode Operation
  - Bit Rate: Up to 400 Kbits
  - General Call Supported in Slave Mode
  - Connection to Peripheral DMA Controller (PDC) Channel Capabilities Optimizes Data Transfers in Master Mode

- **IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins**
- **Required Power Supplies**
  - **0.9V to 1.1V for VDDBU, VDDCORE, VDDPLL**
  - **1.65 to 3.6V for VDDOSC**
  - **1.65V to 3.6V for VDDIOP (Peripheral I/Os)**
  - **3.0V to 3.6V for VDDUSB**
  - **3.0V to 3.6V VDDANA (Analog-to-digital Converter)**
  - **Programmable 1.65V to 1.95V or 3.0V to 3.6V for VDDIOM (Memory I/Os)**
- **Available in a 217-ball LFBGA RoHS-compliant Package**

3.2 AT91SAM9G20 Block Diagram

Figure 3-1. Block Diagram



3.3 Microcontroller

- One 217-ball LFBGA fitted on board

3.4 Memory

- 32 Kbytes of Internal ROM
- Two 4-KByte Internal SRAMs
- Atmel serial DataFlash
- 64 Mbytes of SDRAM memory (32-bit bus width)
- 256 Mbytes of NAND Flash memory (8-bit bus width)
- TWI serial EEPROM

3.5 Clock Circuitry

- 18.432 MHz standard crystal for the embedded oscillator
- Selectable 32,768Hz Low-power external standard crystal Oscillator or Internal Low Power RC Oscillator

3.6 Reset Circuitry

- Internal reset controller with bi-directional reset pin
- External reset pushbutton

3.7 Shutdown Controller

- Programmable shutdown and Wake-Up
- Wake-up push button

3.8 Power Supply Circuitry

- On-board 1.0V High Efficiency step-down charge pump regulator with shutdown control
- On-board 3.3V linear regulator with shutdown control
- On-board power sequencer

3.9 Remote Communication

- One serial interface (DBGU COM Port) via RS-232 DB9 male socket
- One complete modem serial interface (COM Port 0) via RS-232 DB9 male socket
- One additional serial interface (COM Port 1) with RTS/CTS handshake control via
- RS-232 DB9 male socket
- USB V2.0 full-speed compliant, 12 Mbits per second (UDP)
- Two USB Host ports V2.0 full-speed compliant, 12 Mbits per second (UHP)

- One Ethernet 100-base TX with three status LEDs

3.10 Audio Stereo Interface

- Stereo Audio Codec with Integrated Headphone Driver (50 mW on 16W @ 3.3V)
- One Headset output (J4) with master volume and mute controls

3.11 User Interface

- Two user input push buttons
- One user green LED
- One yellow power LED (can be also software controlled)
- Debug Interface
- All I/Os of the AT91SAM9G20 are routed to peripheral extension connectors
- All I/Os of the AT91SAM9G20 Image Sensor Interface are routed to peripheral extension connectors
- All EBI Signals of the AT91SAM9G20 are routed to extension footprint connectors (J25)

3.12 Debug Interface

- 20-pin JTAG/ICE interface connector
- DBGU COM port

3.13 Expansion Slot

- One on-board DataFlash device
- Two SD/MMC card slots, the system can boot from slot J35
- All I/Os of the AT91SAM9G20 are routed to peripheral extension connectors
- All I/Os of the AT91SAM9G20 Image Sensor Interface are routed to peripheral extension connectors
- All EBI Signals of the AT91SAM9G20 are routed to extension footprint connectors (J25)

This allows the developer to check the integrity of the components and to extend the features of the board by adding external hardware components or boards.

3.14 PIO Usage

Table 3-1. I/O Peripheral Controller A

I/O Line	Peripheral A	Peripheral B	Comments	Function
PA0	SPI0_MISO	MCDB0		SPI DataFlash, SPI/MCI SD/MMC/DataFlash Slot
PA1	SPI0_MOSI	MCCDB		(PA0..PA5)
PA2	SPI0_SPCK			
PA3	SPI0_NPCS0	MCDB3		
PA4	RTS2	MCDB2		
PA5	CTS2	MCDB1		
PA6	MCDA0			Boot SD Card Slot (DAT0)
PA7	MCCDA			Boot SD Card Slot (CMD)
PA8	MCCK			MCI SD/MMC/DataFlash Slot (CLK)
PA9	MCDA1			Boot SD Card Slot (DAT1)
PA10	MCDA2	ETX2		1- Boot SD Card Slot (DAT2), 2- ETHERNET DM9161A MII Interface (disconnected by default, see R120)
PA11	MCDA3	ETX3		1- Boot SD Card Slot (DAT3), 2- ETHERNET DM9161A MII Interface (disconnected by default, see R119)
PA12	ETX0			ETHERNET DM9161A RMII Interface (PA12..PA19)
PA13	ETX1			
PA14	ERX0			
PA15	ERX1			
PA16	ETXEN			
PA17	ERXDV			
PA18	ERXER			
PA19	ETXCK			
PA20	EMDC			ETHERNET DM9161A MII/RMII Interface (PA20..PA21)
PA21	EMDIO			
PA22	ADTRG	ETXER		ETHERNET DM9161A MII Interface
PA23	TWD	ETX2		SERIAL EEPROM (SDA), WM8731 audio DAC
PA24	TWCK	ETX3		SERIAL EEPROM (SCL), WM8731 audio DAC
PA25	TCLK0	ERX2		ETHERNET DM9161A MII Interface (PA25..PA29)
PA26	TIOA0	ERX3	High-Drive	
PA27	TIOA1	ERXCK	High-Drive	
PA28	TIOA2	ECRS	High-Drive	
PA29	SCK1	ECOL		
PA30	SCK2	RXD4		(BP3) User's interface Push Button
PA31	SCK0	TXD4		(BP4) User's interface Push Button

Table 3-2. I/O Peripheral Controller B

I/O Line	Peripheral A	Peripheral B	Comments	Function
PB0	SPI1_MISO	TIOA3		ETHERNET DM9161A MII/RMII (IRQ)
PB1	SPI1_MOSI	TIOB3		Audio DAC WM8731 (MOSI)
PB2	SPI1_SPCK	TIOA4		Audio DAC WM8731 (SPCK)
PB3	SPI1_NPCS0	TIOB4		Audio DAC WM8731 (Chip Select)
PB4	TXD0			COM PORT 0 (TXD)
PB5	RXD0			COM PORT 0 (RXD)
PB6	TXD1	TCLK1		COM PORT 1 (TXD)
PB7	RXD1	TCLK2		COM PORT 1 (RXD)
PB8	TXD2			User LED
PB9	RXD2			Power LED
PB10	TXD3	ISI_D8		(J28) IMAGE SENSOR CONNECTOR (PB10..PB13)
PB11	RXD3	ISI_D9		
PB12	TXD5	ISI_D10		
PB13	RXD5	ISI_D11		
PB14	DRXD			SERIAL DEBUG PORT(RXD)
PB15	DTXD			SERIAL DEBUG PORT(TXD)
PB16	TK0	TCLK3		Audio DAC WM8731 (BCLK)
PB17	TF0	TCLK4		Audio DAC WM8731 (LRFS)
PB18	TD0	TIOB4		Audio DAC WM8731 (SDIN)
PB19	RD0	TIOB5		(J28) IMAGE SENSOR CONNECTOR (CTRL2)
PB20	RK0	ISI_D0		(J28) IMAGE SENSOR CONNECTOR (PB20..PB31)
PB21	RF0	ISI_D1		
PB22	DSR0	ISI_D2		Warning: Shared with COM PORT 0 (PB22..PB27)
PB23	DCD0	ISI_D3		
PB24	DTR0	ISI_D4		
PB25	RI0	ISI_D5		
PB26	RTS0	ISI_D6		
PB27	CTS0	ISI_D7		
PB28	RTS1	ISI_PCK		Warning: Shared with COM PORT 1 (PB28..PB29)
PB29	CTS1	ISI_VSYNC		
PB30	PCK0	ISI_HSYNC		
PB31	PCK1	ISI_MCK		

Table 3-3. I/o Peripheral Controller C

I/O Line	Peripheral A	Peripheral B	**Comments**	**Function**
PC0	AD0	SCK3		
PC1	AD1	PCK0		Audio DAC WM8731 (MCLK)
PC2	AD2	PCK1		
PC3	AD3	SPI1_NPCS3		
PC4	A23	SPI1_NPCS2		(J28) IMAGE SENSOR CONNECTOR (CTRL1)
PC5	A24	SPI1_NPCS1		USB_CNX (VBUS DETECT)
PC6	TIOB2	CFCE1		
PC7	TIOB1	CFCE2		
PC8	NCS4/CFCS0	RTS3		
PC9	NCS5/CFCS1	TIOB0		
PC10	A25/CFRNW	CTS3		
PC11	NCS2	SPI0_NPCS1		SPI DataFlash memory (Chip Select)
PC12	IRQ0	NCS7		
PC13	FIQ	NCS6		NAND Flash (RDYBSY)
PC14	NCS3/NANDCS	IRQ2		NAND Flash (NANDCS)
PC15	NWAIT	IRQ1		
PC16	D16	SPI0_NPCS2		EBI Data Bus (PC16..PC31)
PC17	D17	SPI0_NPCS3		
PC18	D18	SPI1_NPCS1		
PC19	D19	SPI1_NPCS2		
PC20	D20	SPI1_NPCS3		
PC21	D21	EF100		
PC22	D22	TCLK5		
PC23	D23			
PC24	D24			
PC25	D25			
PC26	D26			
PC27	D27			
PC28	D28			
PC29	D29			
PC30	D30			
PC31	D31			

Section 4

Configuration

4.1 Jumpers

Table 4-1. Jumpers Configuration

Designation	Default Setting	Feature
J2	Closed	3.3V Jumper[1]
J3	Closed	Forces power on. To use the software shutdown control: • J3 must be opened, • 3V battery backup must be present, • J10 jumper set in position 1-2
J6	Closed	VDDPLL Jumper[1]
J7	Open	Enables boot on the internal ROM
	Closed	Enables boot on the NCS0
J9	2-3	Slow Clock OSCSEL 1-2: Internal RC Oscillator 2-3: External Crystal Oscillator
J10	2-3	VDDBU Jumper select[1] 1-2: Lithium 3V Battery 2-3: 1.0V from VDDCORE
J12	Closed	VDDCORE Jumper[1]
J15	Closed	Enables Ethernet Auto MDIX control
J33	Closed	Serial DataFlash chip select enable
J34	Closed	NAND Flash chip select enable

Note: 1. These jumpers are provided for power consumption measurement. By default, they are closed. To use this feature, the user has to open the strap and insert an ampere meter.

4.2 JTAG/ICE

Table 4-2. JTAG/ICE Configuration

Designation	Default Setting	Feature
S1	Opened	Disables the ICE NTRST input
S2	Opened	Selects ICE Debug Mode or JTAG Boundary Scan Mode
S3	Opened	Disables TCK <-> RTCK local loop. If S3 is closed, R13 must be unsoldered.
R13	Soldered	Enables the ICE RTCK return. S3 must be opened
R14	Soldered	Enables the ICE RTCK return. S3 must be opened

4.3 Microcontroller Clock

Table 4-3. Microcontroller Clock Configuration

Designation	Default Setting	Feature
R18/R20	Soldered	Enables the use of 18.432MHz crystal. If external clock is used, R18/R20 must be unsoldered and S4 closed.
S4	Opened	
J9		Slow Clock Setting. See Table 4-1.

4.4 Memory

Table 4-4. Memory Configuration

Designation	Default Setting	Feature
SDRAM		
R31 R32	Soldered Soldered	Enables MN7 Chip select access Enables MN8 Chip select access
NAND Flash (MN6+x)		
J34 R34 S6	Closed Soldered Opened	Enables the use of NAND Flash (MN6x) Enables the use of Ready Busy signal Disables write protect
SERIAL DataFlash (MN9)		
J33 S5	Soldered Opened	Enable the use of the Serial DataFlash®(MN9) Disables write protect
TWI SERIAL EEPROM (MN10)		
R46 R47	Soldered Soldered	Enables SCL access Enables SDA access

4.5 Ethernet

RMII is the factory default mode. To evaluate the MII mode, the user has to unsolder R49, R50, R127 and close S7 and S8. When the RMII mode is used, the user can use the specific MII signals as PIO, but the following resistors must be unsoldered (R119 to R126).

Note that, by default, resistors R112 and R120 are not populated in order to avoid contention between the MII signals and the SD Card slot J35. If the Ethernet MII mode is implemented on the board, then you must not insert any card into slot J35. Otherwise, signal conflicts could occur and damage both the Ethernet controller and the SD Card.

4.6 Miscellaneous

Refer to “Board Layout - Top View” in Section 5.1 ”Schematics” for the PIO Usage.

Section 5

Schematics

5.1 Schematics

This section contains the following schematics:

- Board Layout - Top View
- Power Supply and Audio
- AT91SAM9G20-CU
- Memory
- Ethernet
- Serial Interface
- Expansion and User Interface

POWER SUPPLY SHEET 2

5VDC

PB9 — PB[0..31] — PIO

SHDN

DAC — WM8731

PC1, PB18, PB17, PB16 — PC[0..15] — PCK0, TD0, TF0, TK0

PA23, PA24, PB3 — PB[0..31] — PA23/TWD, PA24/TWCK, SPI1_NPCS0

01 - POWER SUPPLY

SERIAL INTERFACES SHEET 6

RS232

DBGU — PB15, PB14 — PB[0..31] — DBGU_TXD, DBGU_RXD

COM0 — PB4, PB5, PB26, PB27, PB24, PB22, PB23, PB25

COM1 — PB6, PB7, PB28, PB29

USB

DEVICE — PC5, DDM, DDP — PC[0..15] — PIO

HOST A — HDMA, HDPA

HOST B — HDMB, HDPB

05 - COMMUNICATION

RMII_MII ETHERNET SHEET 5

10/100 Mbps FAST ETHERNET

PA19 — ETXCK/REFCLK

PA11, PA10, PA13, PA12, PA16 — ETX3, ETX2, ETX1, ETX0, ETXEN

PA26, PA25, PA15, PA14 — ERX3, ERX2, ERX1, ERX0

PA27, PA17 — ERXCK, ERXDV

PA22, PA18 — ETXER, ERXER

PA29, PA28 — ECOL, ECRS

PA20, PA21, PB0 — EMDC, EMDIO, PIO

NRST — PA[0..31]

03 - RMII_MII ETHERNET

AT91SAM9G20-CU

SHDN

DDM, DDP

HDMA, HDPA

HDMB, HDPB

D[0..31], A[0..22]

RAS, CAS, SDA10, SDWE, SDCS_NCS1

SDCK, SDCKE

CFIOR_NBS1_NWR1, CFIOW_NBS3_NWR3

NANDOE, NANDWE

PIO, PIO

CFWE_NWE_NWR0

CFOE_NRD

NCS0

NRST

PA[0..31]

PB[0..31]

PC[0..15]

VREFP, AVDD, AGND

02 - AT91SAM9G20-CU

MEMORY SHEET 4

SDRAM

NANFLASH

D[0..15]

CARD READER (BOOT) — MCIA DATAFLASH

MCDA0, MCDA1, MCDA2, MCDA3, MCCK, MCCDA — PA6, PA9, PA10, PA11, PA8, PA7, PC2

CARD READER — MCIB DATAFLASH

SPI0_MISO MCDB0, MCDB1, MCDB2, SPI0_NPCS0 MCDB3, MCCK, SPI0_MOSI MCCDB — PA0, PA5, PA4, PA3, PA8, PA1, PC9

SERIAL DATAFLASH

SPI0_SPCK, SPI0_NPCS1 — PA2, PC11

NRST

SERIAL EEPROM

TWCK, TWD — PA24, PA23

03 - MEMORY

EXPANSION_Users Interfaces SHEET 7

D[0..31], A[0..22]

RAS, CAS, SDA10, SDWE, SDCS_NCS1

SDCK, SDCKE

CFWE_NWE_NWR0, NBS1, NBS3, CFIOR_NBS1_NWR1, CFIOW_NBS3_NWR3, CFOE_NRD

NANDOE, NANDWE

NCS0, NRST, PA[0..31], PB[0..31], PC[0..15]

VREFP, AVDD, AGND

06 - EXPANSION CONNECTORS

PIO MUXING

PIOA	USAGE	PIOA	USAGE	PIOB	USAGE	PIOB	USAGE	PIOC	USAGE	PIOC	USAGE
PA0	DAT0_B/MISO	PA16	TX_EN	PB0	MDINTR	PB16	BCLK	PC0	--	PC16	D16
PA1	CMD_B/MOSI	PA17	RX_DV	PB1	--	PB17	LRFS	PC1	MCLK	PC17	D17
PA2	SCK	PA18	RX_ER	PB2	--	PB18	SDIN	PC2	CD_A	PC18	D18
PA3	DAT3_B	PA19	TX_CLK	PB3	CS	PB19	PIO_CNTRL2	PC3	--	PC19	D19
PA4	DAT2_B	PA20	MDC	PB4	TXD0	PB20	ISI_DATA[0]	PC4	PIO_CNTRL1/ A23	PC20	D20
PA5	DAT1_B	PA21	MDIO	PB5	RXD0	PB21	ISI_DATA[1]	PC5	USBCNX/ A24	PC21	D21
PA6	DAT0_A	PA22	TX_ER	PB6	TXD1	PB22	DSR0/ ISI_DATA[2]	PC6	CFCE1	PC22	D22
PA7	CMD_A	PA23	SDA/ DIN/ TWD	PB7	RXD1	PB23	DCD0/ ISI_DATA[3]	PC7	CFCE2	PC23	D23
PA8	CLK_B/CLK_A	PA24	SCL/CLK/TWCK	PB8	USER LED	PB24	DTR0/ ISI_DATA[4]	PC8	CFCS0_NCS4	PC24	D24
PA9	DAT1_A	PA25	RXD2	PB9	POWERLED	PB25	RI0/ ISI_DATA[5]	PC9	CD_B/ CFCS1_NCS5	PC25	D25
PA10	DAT2_A/ TXD2	PA26	RXD3	PB10	ISI_DATA[8]	PB26	RTS0/ ISI_DATA[6]	PC10	A25_CFRNW	PC26	D26
PA11	DAT3_A/ TXD3	PA27	RX_CLK	PB11	ISI_DATA[9]	PB27	CTS0/ ISI_DATA[7]	PC11	CS/ NCS2	PC27	D27
PA12	TXD0	PA28	CRS	PB12	ISI_DATA[10]	PB28	RTS1/ ISI_PCK	PC12	NCS7	PC28	D28
PA13	TXD1	PA29	COL	PB13	ISI_DATA[11]	PB29	CTS1/ ISI_VSYNC	PC13	RDYBSY/ NCS6	PC29	D29
PA14	RXD0	PA30	BP3	PB14	DRXD	PB30	ISI_HSYNC	PC14	NANDCS_NCS3	PC30	D30
PA15	RXD1	PA31	BP4	PB15	DTXD	PB31	ISI_MCK	PC15	NWAIT	PC31	D31

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B		PP	02/07/08		
A	INIT EDIT	TVT	15/04/08		

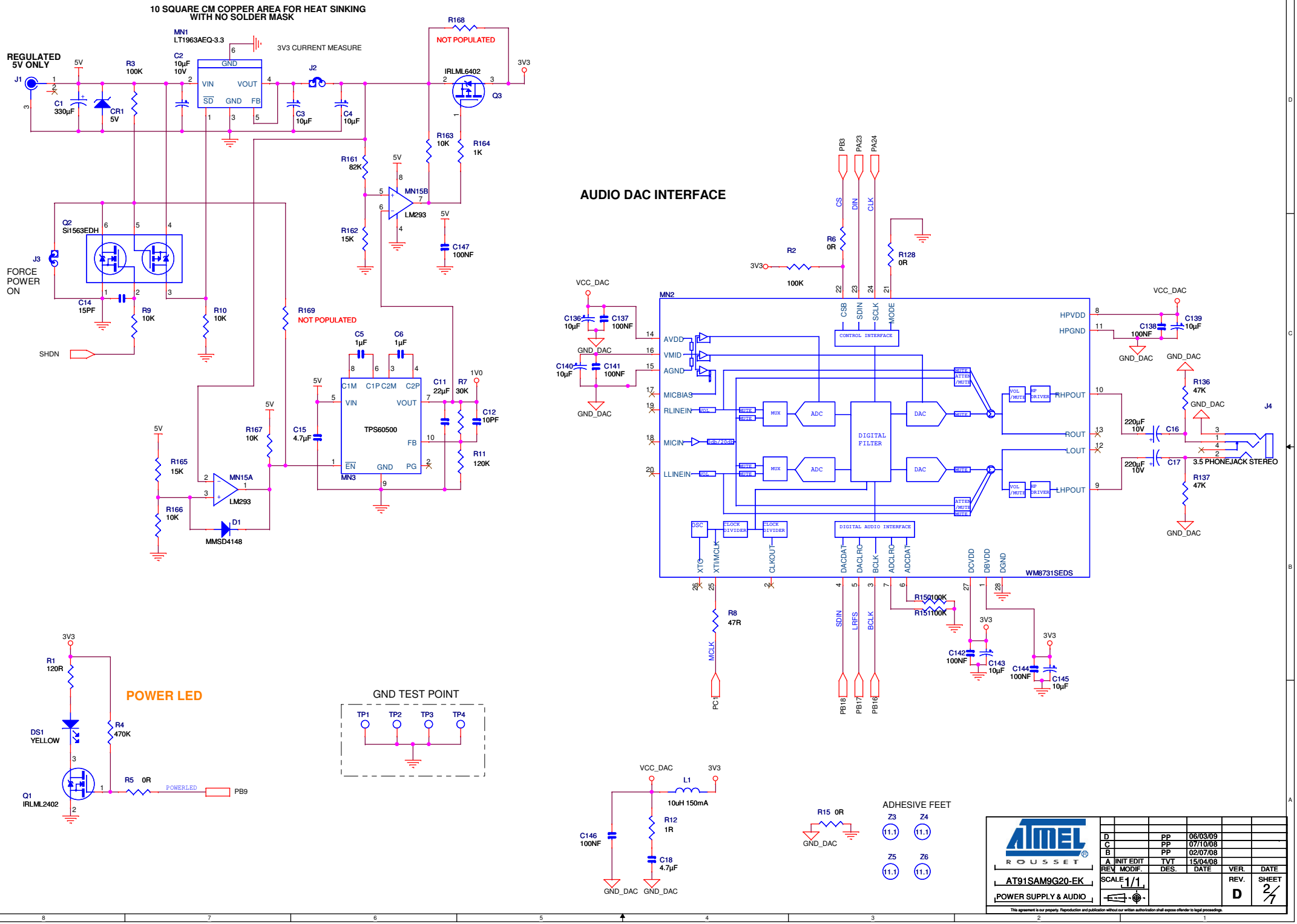
AT91SAM9G20-EK

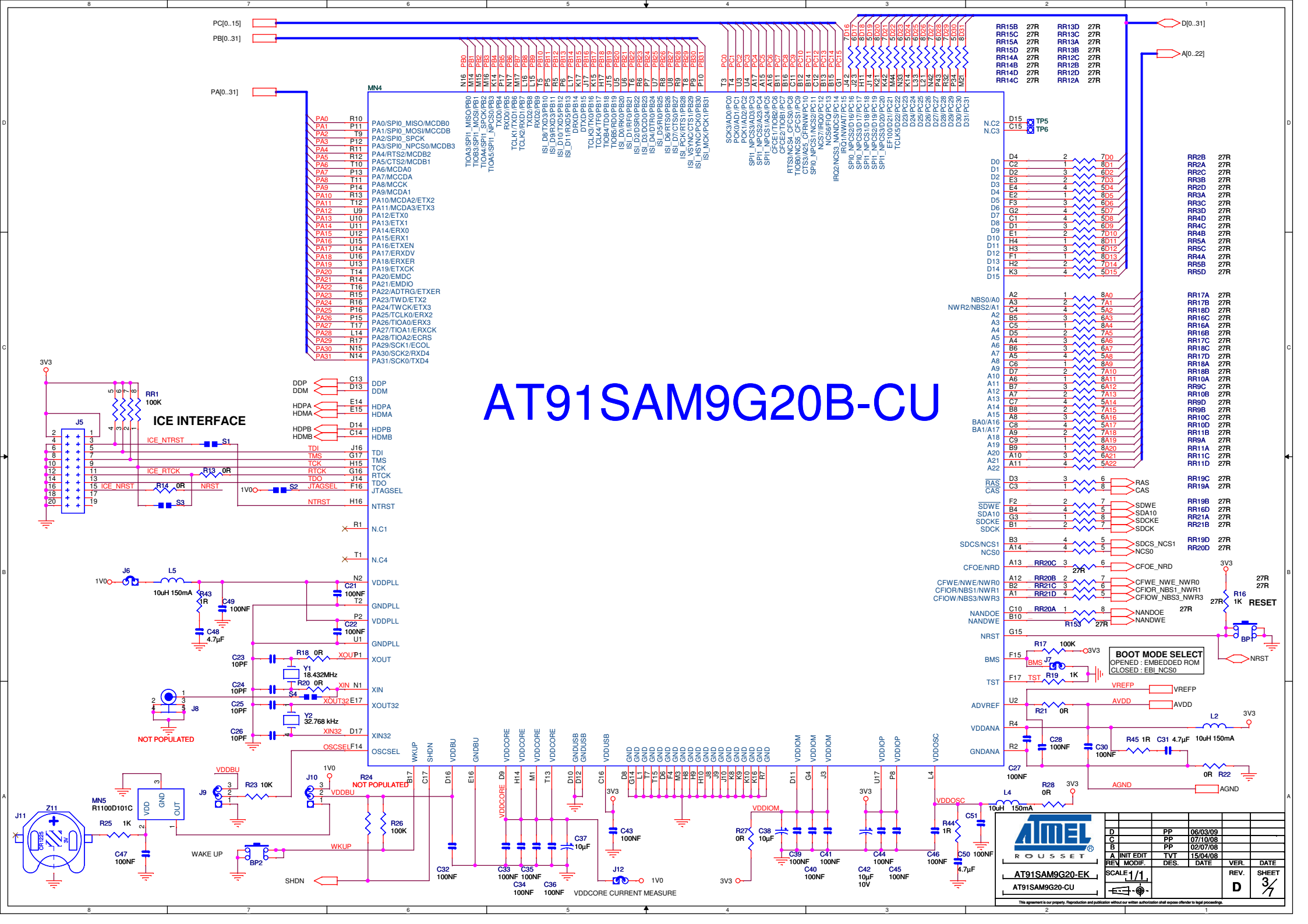
DIAGRAM

SCALE 1/1

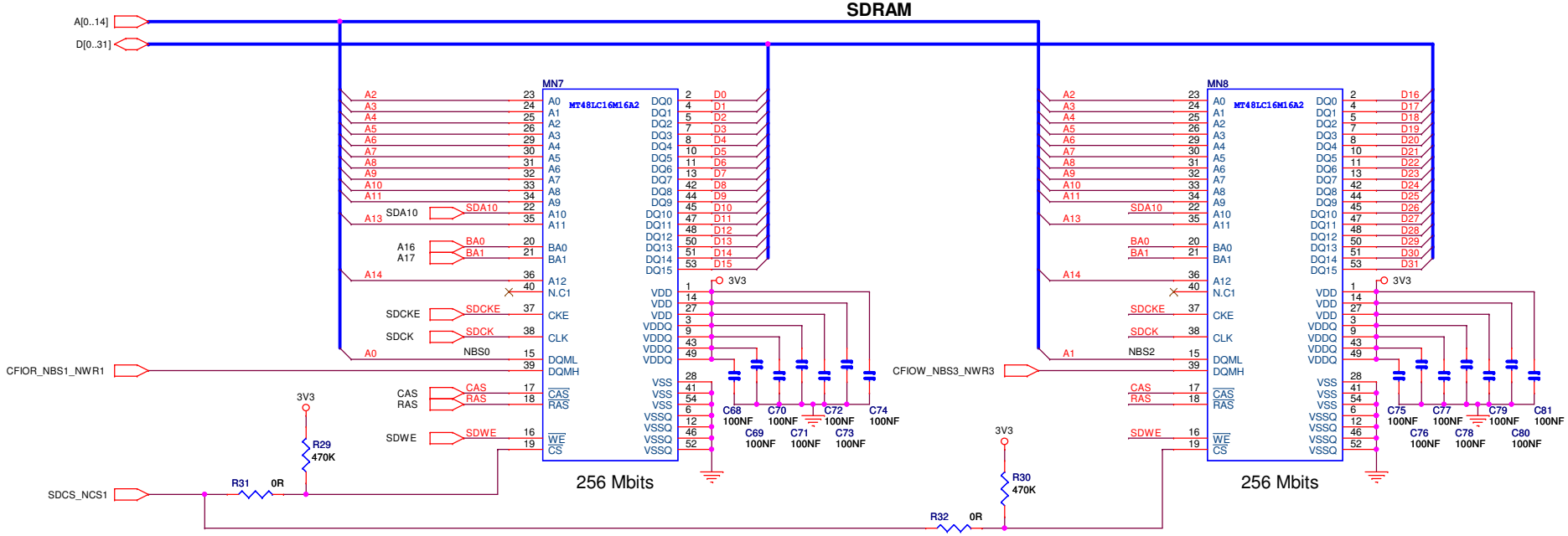
REV. D

SHEET 1/7

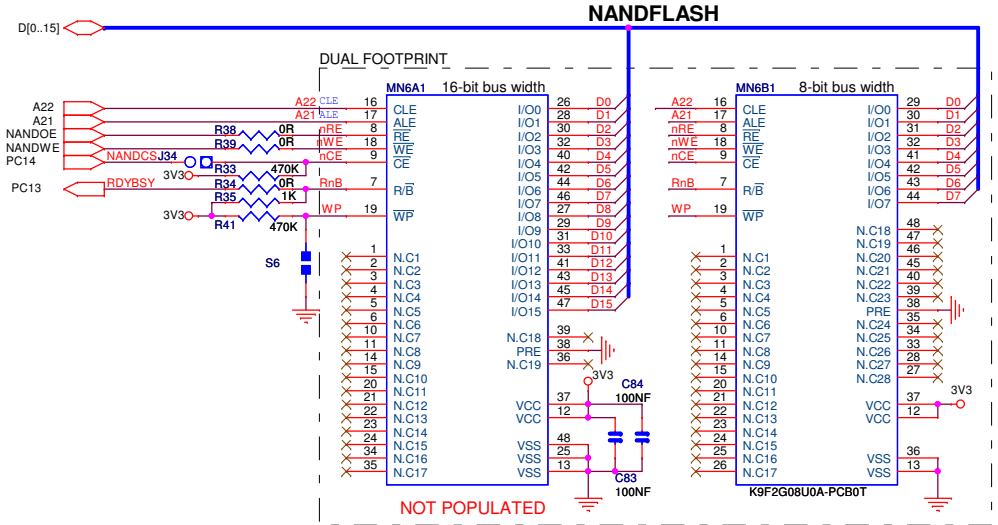

10 SQUARE CM COPPER AREA FOR HEAT SINKING
WITH NO SOLDER MASK
REGULATED
5V ONLY
MN1
LT1963AEQ-3.3
3V3 CURRENT MEASURE
R168
NOT POPULATED
IRLML6402
Q3
3V3
J1
R3
100K
C2
10µF
10V
GND
VIN
VOUT
SD
GND
FB
J2
C1
330µF
CR1
5V
C3
10µF
C4
10µF
R163
10K
R164
1K
R161
82K
MN15B
LM293
R162
15K
C147
100NF
Q2
Si1563EDH
J3
FORCE
POWER
ON
C14
15PF
R9
10K
R10
10K
SHDN
R169
NOT POPULATED
C5
1µF
C6
1µF
C1M
C1P
C2M
C2P
VIN
VOUT
C11
22µF
R7
30K
1V0
C12
10PF
TPS60500
FB
EN
GND
PG
MN3
C15
4.7µF
R11
120K
R167
10K
R165
15K
MN15A
LM293
R166
10K
D1
MMSD4148
AUDIO DAC INTERFACE
VCC_DAC
R2
100K
R6
0R
R128
0R
PB3
PA23
PA24
CS
DIN
CLK
MN2
CSB
SDIN
SCLK
MODE
CONTROL INTERFACE
C136
10µF
C137
100NF
C140
10µF
C141
100NF
GND_DAC
AVDD
VMID
AGND
MICBIAS
RLINEIN
MICIN
LLINEIN
MUX
ADC
DAC
DIGITAL
FILTER
HPVDD
HPGND
C139
10µF
C138
100NF
RHPOUT
LHPOUT
ROUT
LOUT
R136
47K
R137
47K
220µF
10V
C16
C17
J4
3.5 PHONEJACK STEREO
OSC
CLOCK
DIVIDER
DIGITAL AUDIO INTERFACE
XTO
XTI/MCLK
CLKOUT
DACDAT
DACLRO
BCLK
ADCLRO
ADCDAT
DCVDD
DBVDD
DGND
WM8731SEDS
R8
47R
MCLK
PC1
SDIN
LRFS
BCLK
PB18
PB17
PB16
R150100K
R151100K
C142
100NF
C143
10µF
C144
100NF
C145
10µF
POWER LED
R1
120R
DS1
YELLOW
R4
470K
Q1
IRLML2402
R5 0R
POWERLED
PB9
GND TEST POINT
TP1
TP2
TP3
TP4
L1
10uH 150mA
R12
1R
C146
100NF
C18
4.7µF
R15 0R
ADHESIVE FEET
Z3
Z4
Z5
Z6
11.1
ATMEL
ROUSSET
AT91SAM9G20-EK
POWER SUPPLY & AUDIO
SCALE 1/1
REV. D
SHEET 2/7
D PP 06/03/09
C PP 07/10/08
B PP 02/07/08
A INIT EDIT TVT 15/04/08
REV. MODIF. DES. DATE VER. DATE


AT91SAM9G20B-CU
ICE INTERFACE
BOOT MODE SELECT
OPENED : EMBEDDED ROM
CLOSED : EBI_NCS0
RESET
NOT POPULATED
WAKE UP
VDDCORE CURRENT MEASURE
AT91SAM9G20-EK
AT91SAM9G20-CU
ATMEL ROUSSET
SCALE 1/1
REV. D
SHEET 3/7

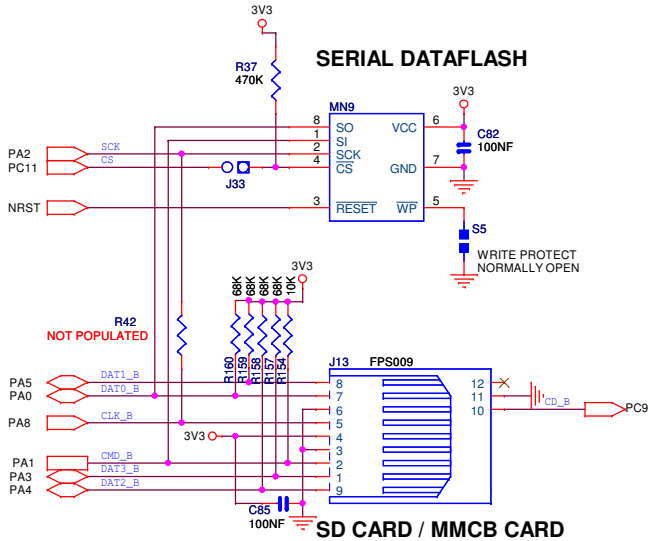
SDRAM



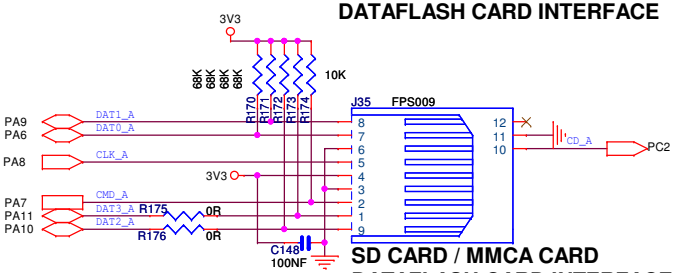
NANDFLASH



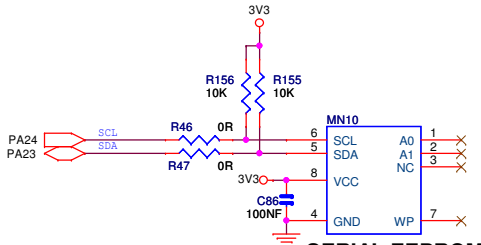
SERIAL DATAFLASH



SD CARD / MMCB CARD DATAFLASH CARD INTERFACE



SD CARD / MMCA CARD DATAFLASH CARD INTERFACE (BOOTABLE)



SERIAL EEPROM

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A	INIT EDIT	TVT	15/04/08		

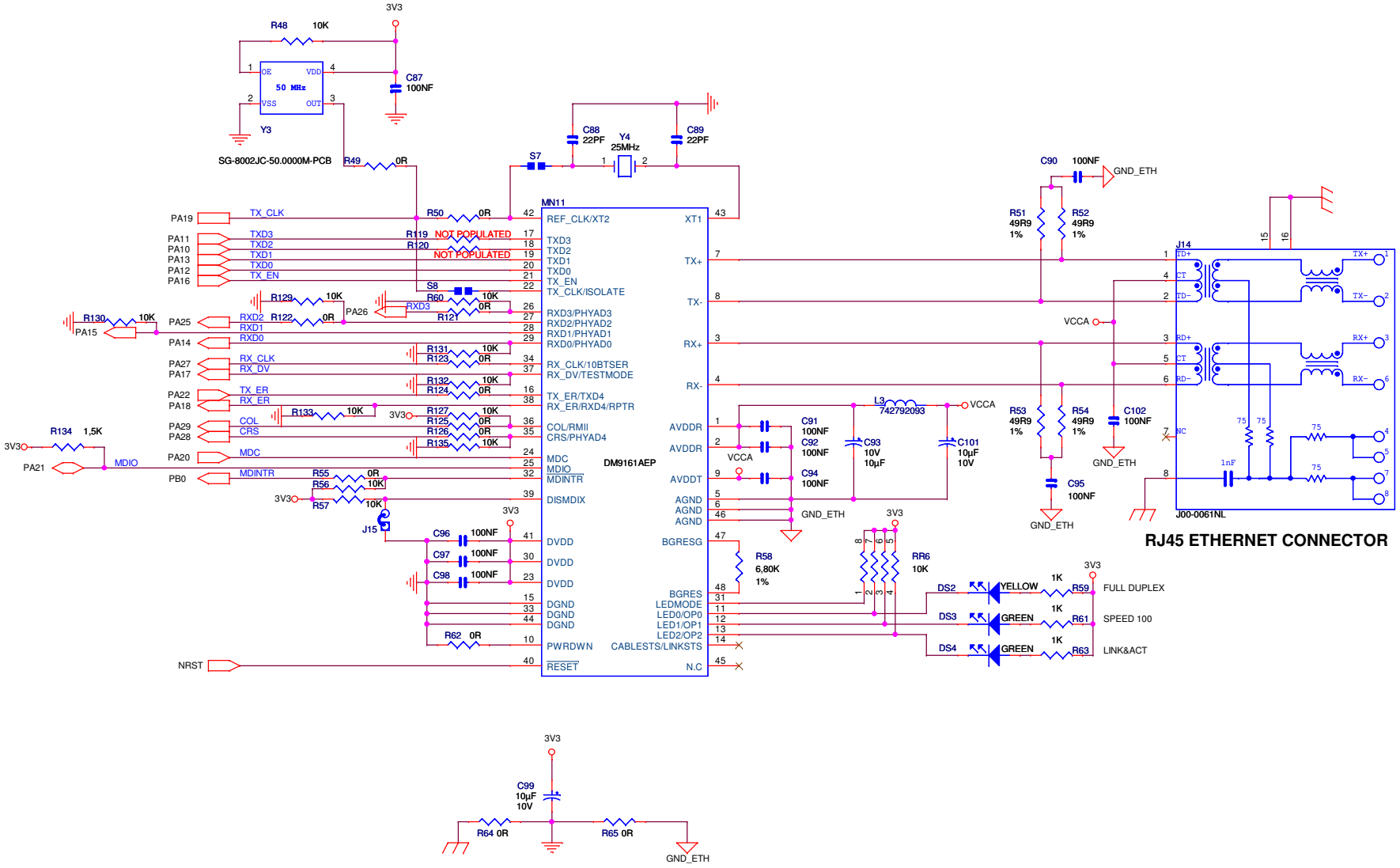
AT91SAM9G20-EK

MEMORY

SCALE 1/1

REV. D

SHEET 4/7



REV	MODIF.	DES.	DATE	VER.	DATE
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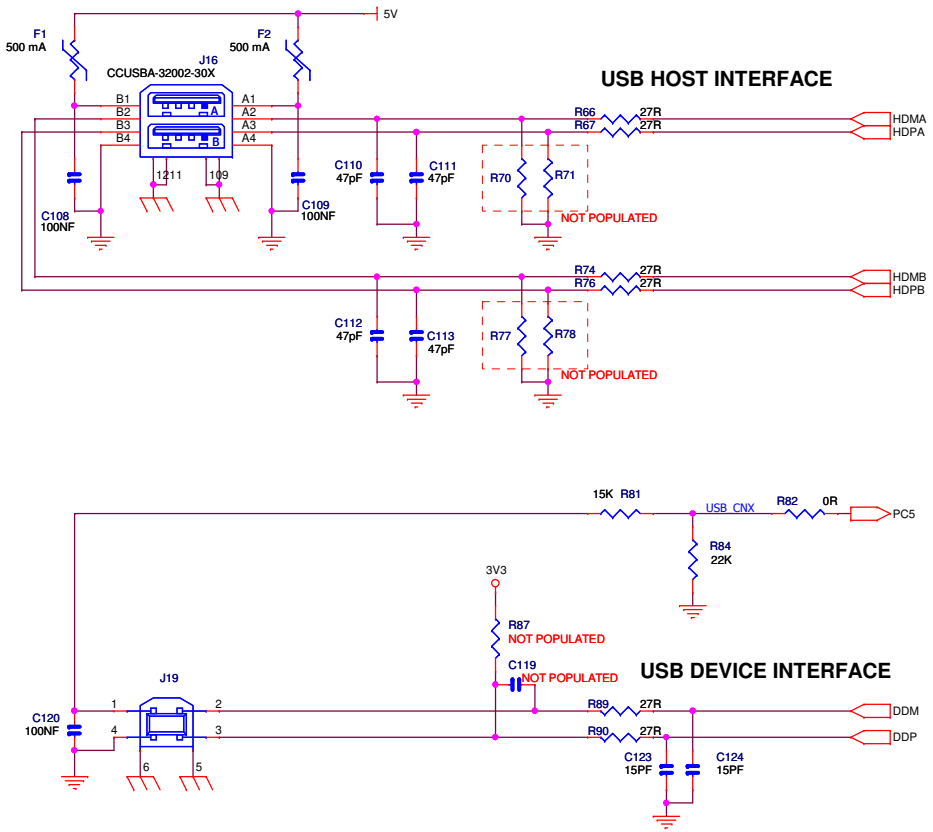
AT91SAM9G20-EK

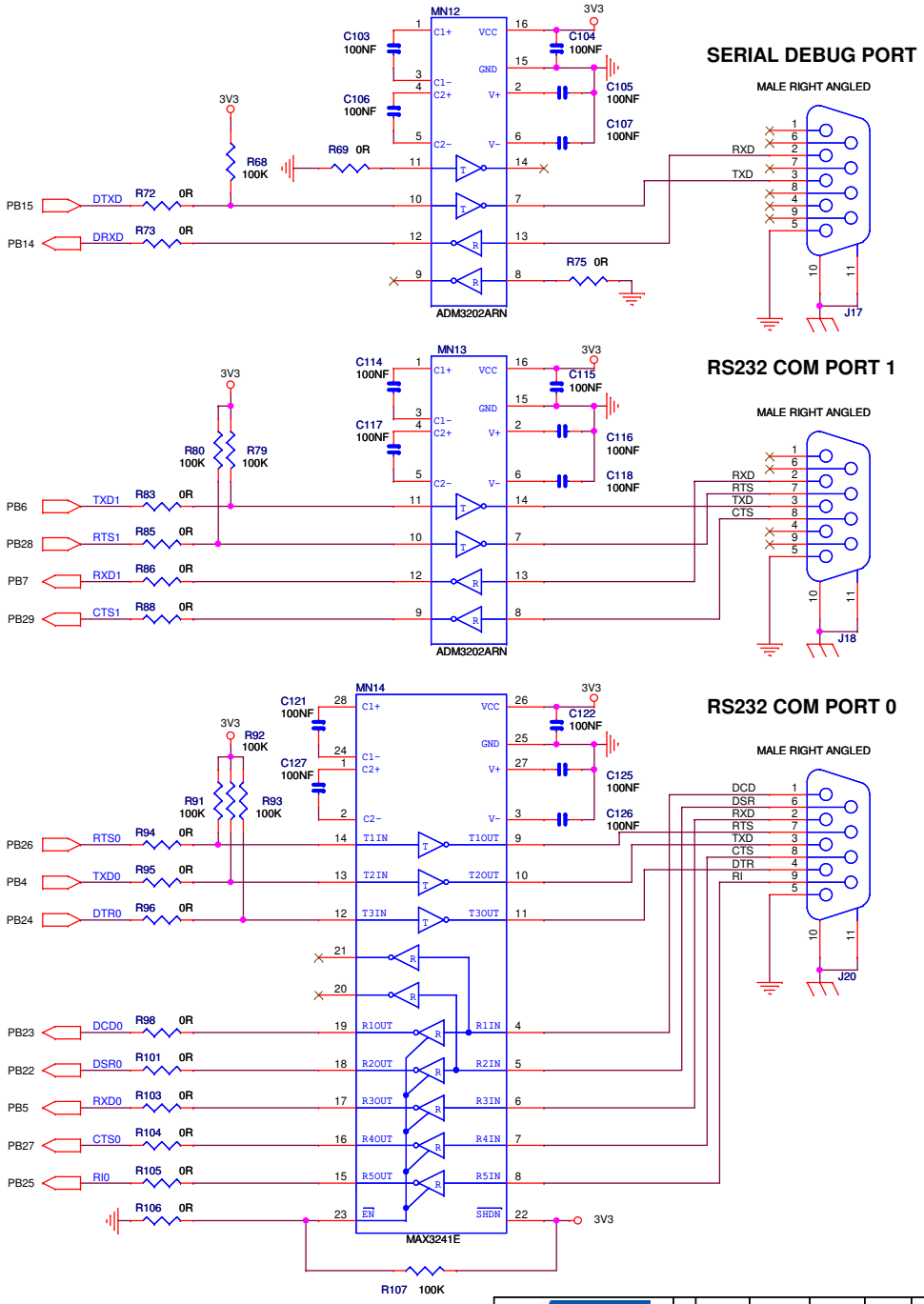
ETHERNET

SCALE 1/1

REV. D

SHEET 5/7





REV.	MODIF.	DES.	DATE
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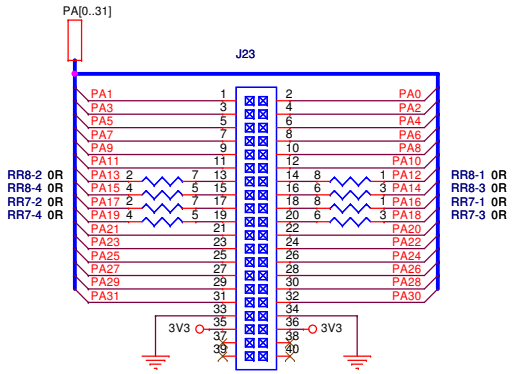
AT91SAM9G20-EK

SERIAL INTERFACES

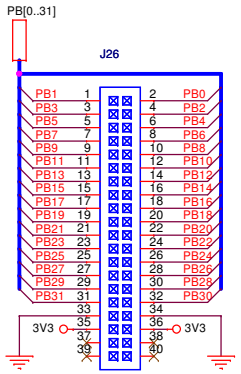
SCALE 1/1

REV. D

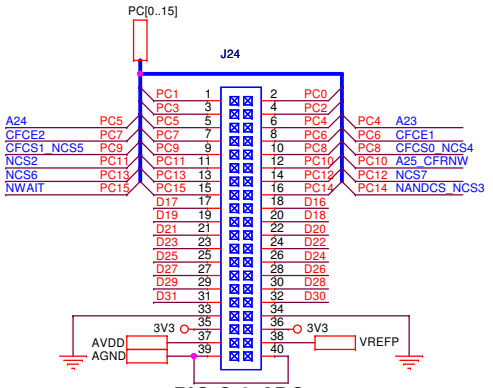
SHEET 6/7



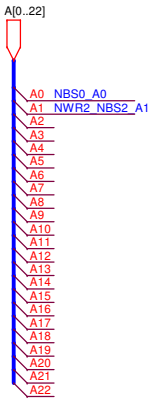
PIO A



PIO B



PIO C & ADC



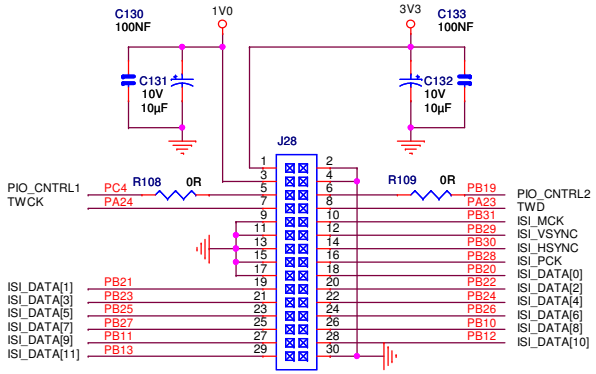
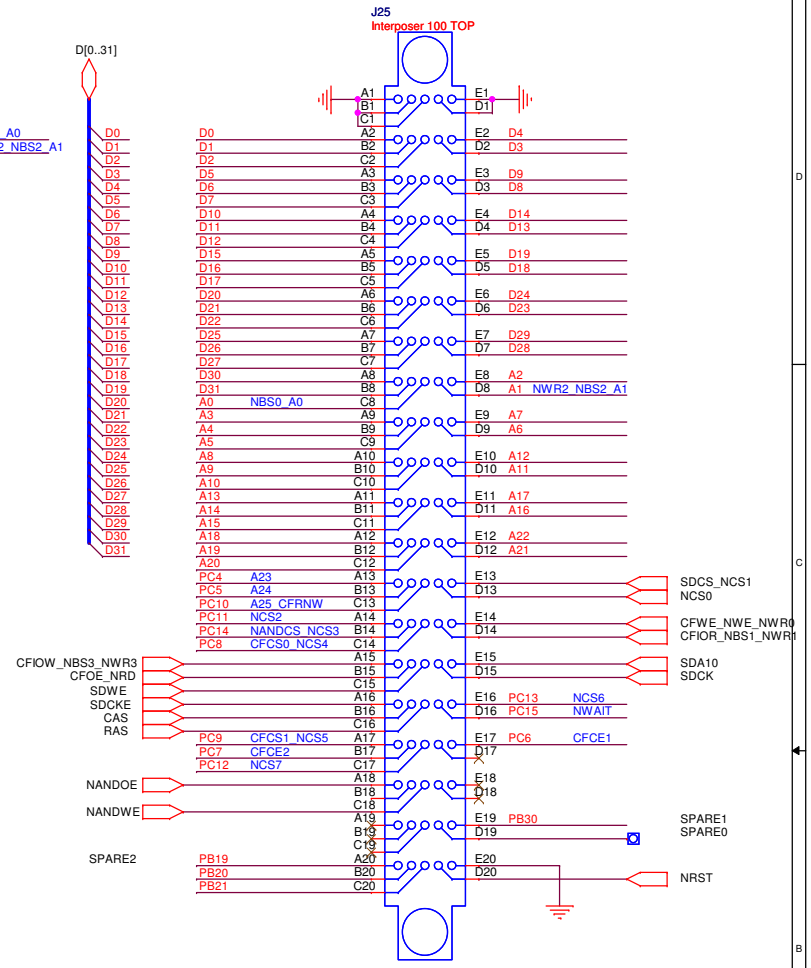
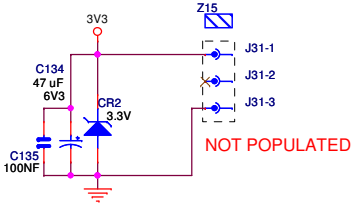


IMAGE SENSOR CONNECTOR



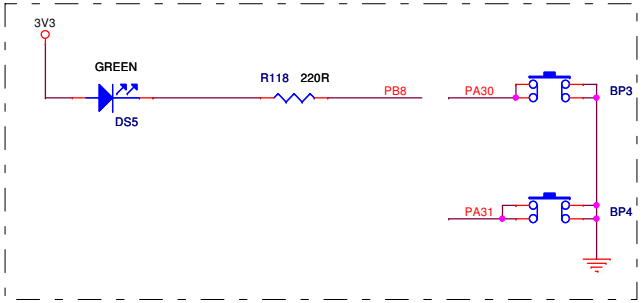
EBI CONNECTORS

NOT POPULATED



NOT POPULATED

USER INTERFACE



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AT91SAM9G20-EK

EXPANSION_UI

SCALE 1/1

REV. D

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Section 6

Errata

6.1 Wrong Silkscreen of BB and 1.0V on the Board

There is a silkscreen reversion on the board, for the selection of the VDDBU source:

- On J10 position 1-2, the marking should be ‘BB’ for Battery Backup instead of ‘1.0V’
- On J10 position 2-3, the marking should be ‘1.0V’ instead of ‘BB’.

This erratum is not applicable for AT91SAM9G20-EK Rev. C and later versions.

6.2 Choice of an Oscillator Capacitance

For many reasons at the manufacturing level, Atmel does not specify any crystal references at the board design stage.

Because of that, the user can find an inconsistency in the value of the used capacitance of the 18.432 MHz crystal on each pin (C23, C24), and the nominal load capacitance of the crystal.

As a reminder, here is the way to select these values.The electrical parameter allows you to fit the right values provided by the crystal manufacturer - and not by Atmel. They are called "Load Capacitance" of the crystal. You have to take stray capacitances (package, socket, trace) into account in order to be close enough to the equivalent nominal Load Capacitance.

With the on-board HCM49-18.432MABJT crystal reference, 10 pF capacitances have been fitted on the 18.432 MHz crystal for a nominal 27 pF load capacitance.

6.3 SD Card Slots and Booting Capability

On the board, Slot J13 is incorrectly marked with a “bootable” mention (solder side). This should be applied to J35 instead. However, the schematic entitled ” Memory” attached to this User Guide, in Section 5.1 ”Schematics” does represent the correct location and marking.

Section 7

Revision History

7.1 Revision History

Table 7-1.

Document	Comments	Change Request Ref
6413C	Section 6.3 ”SD Card Slots and Booting Capability”, added to errata	6874
6413B	Errata section created with Section 6.1 ”Wrong Silkscreen of BB and 1.0V on the Board”	5413
	Section 6.2 ”Choice of an Oscillator Capacitance” added to errata	6392
	New schematics pdf file (at91sam9g20-ek revc.pdf) attached to Section 5.1 ”Schematics”	5936
	- Section 1.2 ”Deliverables” on page 1-1, last bullet added - Section 3.8 ”Power Supply Circuitry” on page 3-5, last bullet added - PA23-24 rows edited in Table 3-1 on page 3-7 - 2 rows (J33-34) added to Table 4-1 on page 4-1	5851
	- Section 1.3 ”AT91SAM9G20-EK Evaluation Board” on page 1-1: ‘one’ DataFlash changed to ‘two’ - 3 figures changed: Figure 2-1 on page 2-2, Figure 2-2 on page 2-3, and Figure 2-3 on page 2-5 - Typo in Section 2.6 ”Getting Started” on page 2-4: ‘tools’ instead of ‘tool’ - 4 bullets removed from Section 3.11 ”User Interface” on page 3-6 - 2 bullets edited in Section 3.13 ”Expansion Slot” on page 3-6 - PA6 to PA11 rows edited in Table 3-1 on page 3-7 - PB0 and PB8-9 rows edited in Table 3-2 on page 3-8 - A paragraph added at the end of Section 4.5 ”Ethernet” on page 4-3	RFO
6413A	First Issue	

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