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SN8000CMK



User Guide

Revision History

Revision	Date	Author	Change Description
1.0	June 6, 2015	RF PD Department	Initial Release

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1 Introduction

SN8000 is a FCC/IC/ETSI certified IEEE 802.11b/g/n Wi-Fi module. It integrates Wi-Fi SoC, RF front end, clock, and on-board antenna or U.FL connector. The SN8000 CM Kit can serve as a software development platform to design IP-enabled WiFi systems for Freescale iMX6 platform. This document provides the information for setting up the CMK.

The SN8000CM Kit consists of a SN8000CM board, a SN8000UFLCM board and a Murata i.MX Interconnect board. The only difference between SN8000 and SN8000UFL is the RF interface. SN8000 contains an on-board antenna, while SN8000UFL provides an UFL connector for use with an external antenna. The following antennas are included for SN8000UFL, Microchip TRF1002 (+5dBi) and Pulse Electronics W1049B050 (+2dBi)^[1]. The 2dBi antenna must be used for ETSI compliant applications.

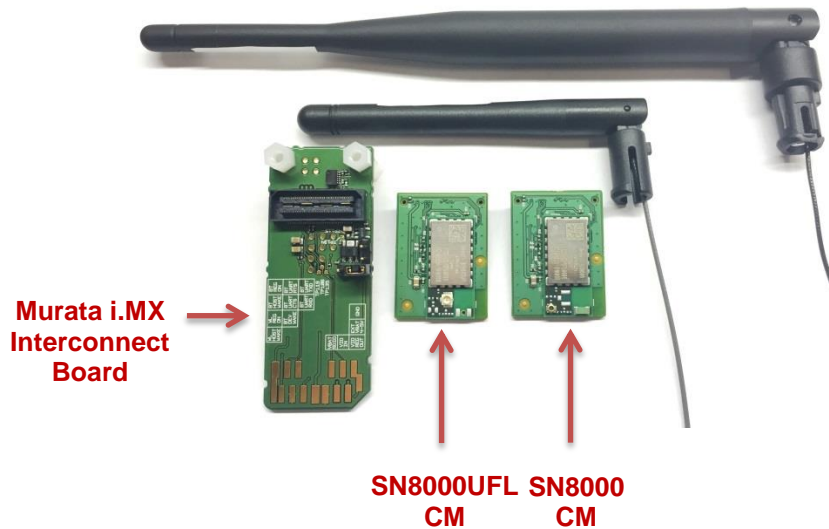


Figure 1 SN8000CM Kit Content

This application note applies to following SN8000 modules.

Model #	P/N	Antenna Configure
SN8000	88-00153-00	On-board antenna
SN8000UFL	88-00153-02	U.FL connector

Table 1: SN8000 Wi-Fi Module Family

1.1 Acronyms

Acronym	Meaning
API	Application Programming Interface
EVB	Evaluation Board
EVK	Evaluation Kit
FW	Firmware
GPIO	General Purpose Input/Output
PC	Personal Computer
SW	Software
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

1.2 References

- [1] Murata, SN8000/SN8000UFL WiFi Module Datasheet, "sn8000-8000ufl_ds_112513.pdf"
- [2] Murata, SN8000 CM schematic, "SN8000_CM_JZ154_SCH_Rev0R3_20130315.pdf"
- [3] Murata, Murata i.MX Interconnect schematic, "Murata_SD_BCM_Adapter_Rev5.pdf"
- [4] Samtec Inc., QTH Datasheet

2 SN8000/SN8000UFL CM Configuration

The hardware of SN8000 Carrier Module (SN8000CM) consists of a single printed circuit board module mounted with SN8000 and a 64-pin connector. **Figure 2** shows the picture of the SN8000CM board. The SN8000UFL CM board is configured the same except mounted with SN8000UFL module.

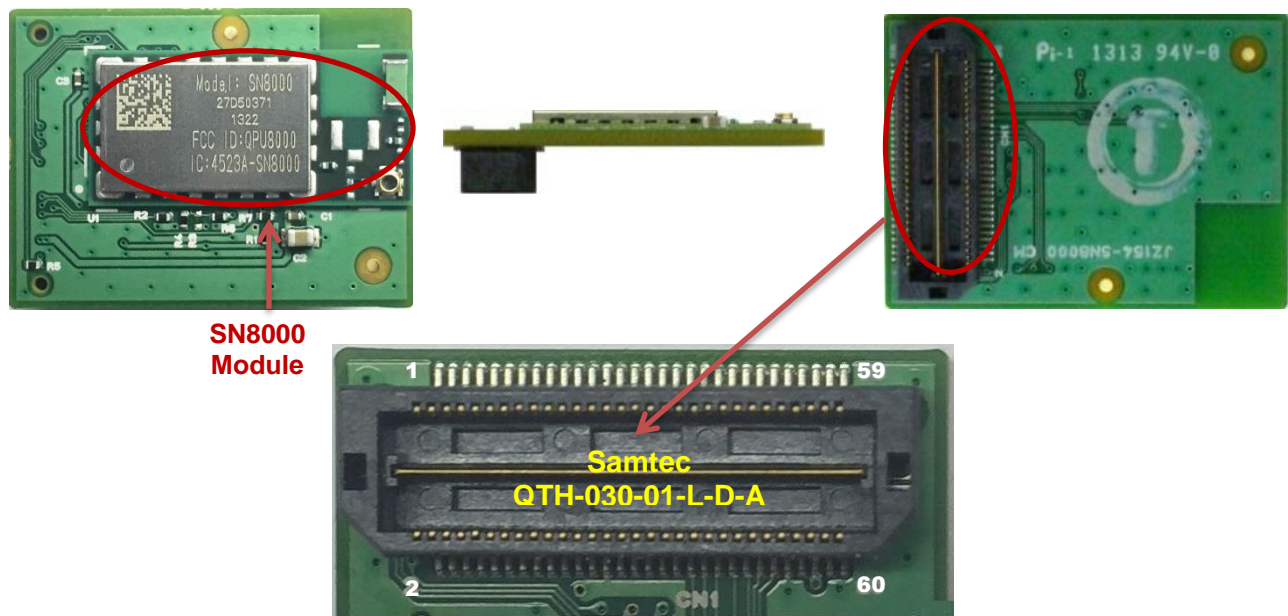


Figure 2 SN8000 CM Board

Samtec QTH-030-01-L-D-A 60-pin connector is used to connect to Murata i.MX Interconnect board. **Table 2** below lists the pin-out information ^[1,2].

Connector pin #	SN8000 Pin#	SN8000 Pin	Description
2		GND	Ground
3		GND	Ground
9		GND	Ground
12		GND	Ground
14	2	SDIO_DATA_2	SDIO data line 2 with internal weak pull-up that can be disabled. It is forced on for SPI mode.
15	5	BTCX_FREQ/GPIO_1	GPIO/Coexistence output signal indicating Bluetooth transmission in restricted channel. Hi-Z at power-up and reset.
16	34	SDIO_DATA_1/ SPI_IRQ	SDIO data line 1 with internal weak pull-up that can be disabled.
17	10	RST_N	Active low WLAN reset signal with internal 200K pulldown.
18	38	SDIO_DATA_3/ SPI_CSX	SDIO data line 3 with internal weak pull-up that can be disabled.
20	36	SDIO_CLK/ SPI_CLK	SDIO clock.
21	45	JTAG_TCK	JTAG pin.

Connector pin #	SN8000 Pin#	SN8000 Pin	Description
22	35	SDIO_DATA_0/ SPI_MISO	SDIO data line 0 with internal weak pull-up that can be disabled.
23		GND	Ground
24	37	SDIO_CMD/ SPI_MOSI	SDIO command line with internal weak pull-up that can be disabled.
25	47	JTAG_TMS	JTAG pin.
26		GND	Ground
27	4	JTAG_TDO	JTAG pin/UART_TX.
29	3	JTAG_TDI	JTAG pin/UART_RX.
31		JTAG_TRS_L	JTAG pin.
38	30	BTCX_RF_ACTIVE/GPIO_5	GPIO/Coexistence signal indicating Bluetooth is active. Hi-Z at power-up and reset.
40	29	BTCX_TXCONF/GPIO_3	GPIO/Coexistence output giving Bluetooth permission to transmit. Hi-Z at power-up and reset.
42	28	BTCX_STATUS/GPIO_4	GPIO/Coexistence signal indicating Bluetooth priority status and TX/RX direction. Hi-Z at power-up and reset.
44	11	VDD3V3_EN	Enables internal 3.3V LDO. Has 100K PU.
46	7	ANT_SEL2	Auxiliary antenna select line (RFSW_CONTROL3). Default low.
48	8	ANT_SEL1	Main antenna select line (RFSW_CONTROL0). Default high.
49		GND	Ground
50	6	GPIO0	GPIO/Strapping option for SDIO (pull low) or SPI mode (pull high). Has 10K PD
52		GND	Ground
53	12	VDD_BAT	Module power supply
55	12	VDD_BAT	Module power supply
56	33	VDD_IO	Power for IO and SDIO pads
57		GND	Ground
58		GND	Ground
59	31	SLEEP_CLK	Optional external 32KHz sleep clock. Tie to GND if not used.

Table 2 SN8000 CM Board Pin-out

3 Murata i.MX Interconnect Board Configuration

The Murata i.MX Interconnect board is a comprehensive adapter board for i.MX6.

- Connects standard SDIO lines: DAT[0..3], CLK, CMD.
- Connects additional WL_REG_ON and WL_HOST_WAKE control signals.
- Provides 32 KHz slow clock on adapter board.
- Power SN8000 EVB from either VBAT_SDIO (from Freescale EVK) or from external lab bench power supply.

Samtec QSH-030-01-L-D-A 60-pin connector is used on board to connect to the SN8000/SN8000UFL CM.

3.1 Default Configuration

Table 3 shows the pin-out from the Murata i.MX Interconnect board ^[1,2,3].

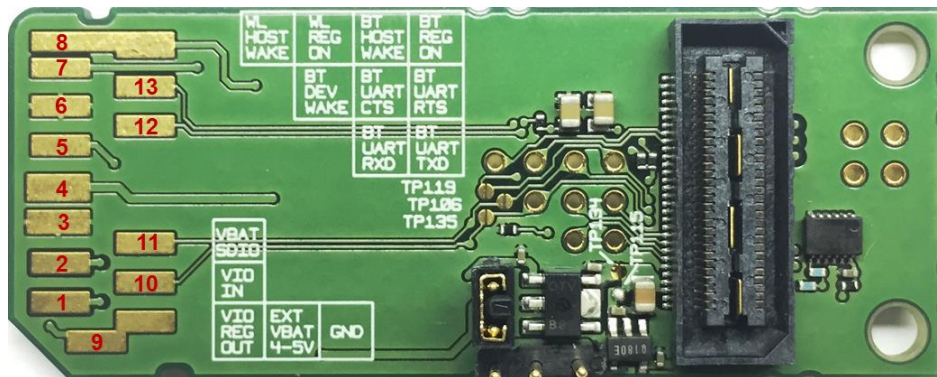


Figure 3 Murata i.MX Interconnect Board

MMC Pin #	Freescale i.MX EVK SD /MMC Pin	CM Pin #	SN8000 CM Signal	SN8000 Pin #	Short-Pad /Jumper Closed	Notes
1	DAT3	18	SDIO_DATA_3	38	N/A	WLAN 4-bit SDIO connection is default. Cannot be modified.
2	CMD	24	SDIO_CMD	37	N/A	WLAN 4-bit SDIO connection is default. Cannot be modified.
3	VSS		NC		N/A	Note used
N/A		56	VDD_IO	33	TP115; (TP122+TP123)	Default configuration VDD_IO is set to VBAT_SDIO 3.3V. For 1.8V VIO Option: switch jumper (TP122+TP123) to (TP123+TP124)
4	VDD	53,55	VDD_BAT	12	TP133	VBAT_SDIO from Freescale EVK typically 3.3V. Alternative option is connecting external power supply (4-5V Range) so VBAT_IN=3.6V.
5	CLK	20	SDIO_CLK	35	N/A	WLAN 4-bit SDIO connection is default. Cannot be modified.
6	VSS		NC		N/A	Note used
7	DAT0	22	SDIO_DATA_0	36	N/A	WLAN 4-bit SDIO connection is default. Cannot be modified.
8	DAT1	16	SDIO_DATA_1	24	N/A	WLAN 4-bit SDIO connection is default. Cannot be modified.
9	DAT2	14	SDIO_DATA_2	2	N/A	WLAN 4-bit SDIO connection is default. Cannot be modified.
10	DAT4					
11	DAT5	45	NC	N/A	TP109	This pin is NOT connected to SN8000 by default. It can be optionally used to connect to

MMC Pin #	Freescale i.MX EVK SD /MMC Pin	CM Pin #	SN8000 CM Signal	SN8000 Pin #	Short-Pad /Jumper Closed	Notes
						SN8000 module pin 5 (GPIO1). Please see section 3.2.
12	DAT6	41	NC	N/A	TP130	This pin is NOT connected to SN8000 by default. It can be optionally used to connect to SN8000 module pin 10 (RST_N). Please see section 3.2.
13	DAT7					

Table 3 Murata i.MX Interconnect Board Pin-out

Figure 4 and Figure 5 below shows the top and bottom view of the board.

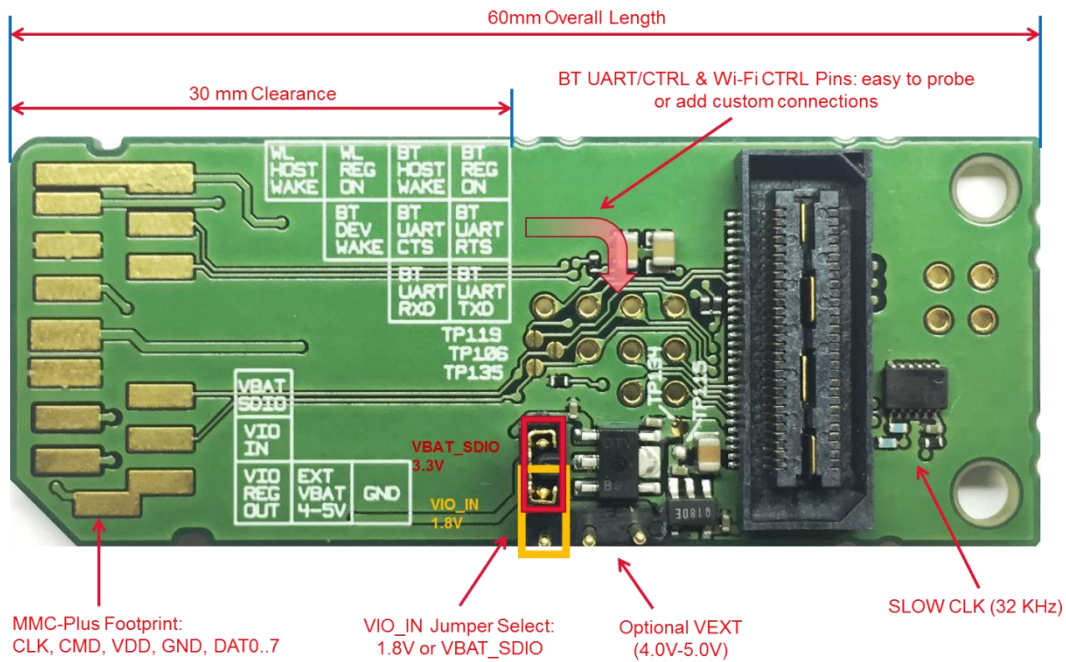


Figure 4 Murata i.MX Interconnect Board Top View

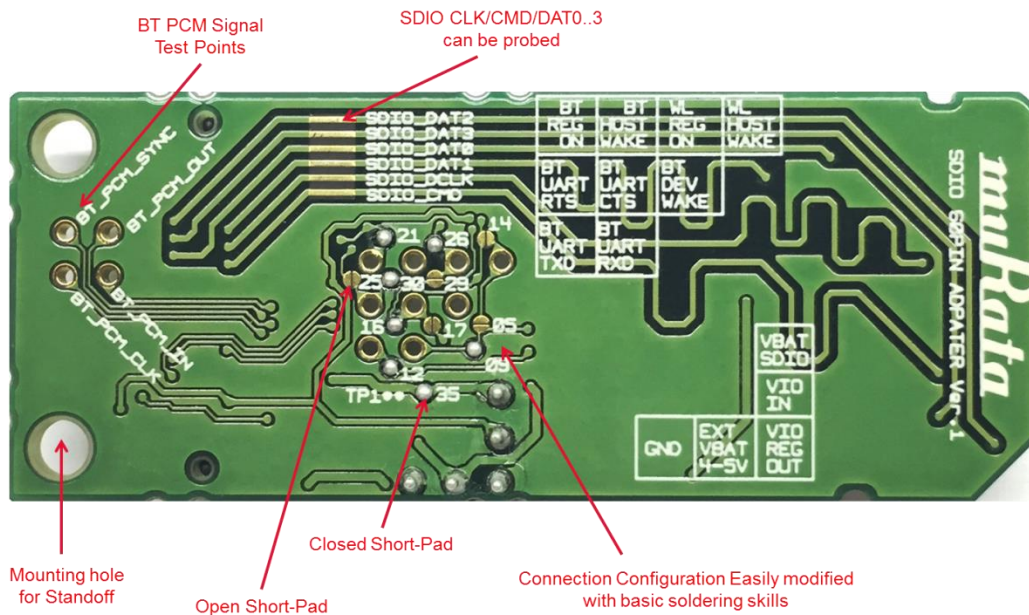


Figure 5 Murata i.MX Interconnect Board Bottom View

3.2 Optional Connection

DAT5 and DAT6 can be used optionally to connect to SN8000 GPIO1 and RST_N pins.

3.2.1 DAT5

DAT5 pin can be alternatively used to connect to SN8000 CM/SN8000UFL CM pin 15, which is connected to SN8000/SN8000UFL module pin 5, GPIO1.

	MMC Pin #	Freescale i.MX EVK SD /MMC Pin	SN8000 CM/ Murata i.MX Interconnect Pin #	Murata i.MX Interconnect pin	SN8000 CM Signal	SN8000 Pin #	SN8000 Signal	Short-Pad Config
Default	11	DAT5	45	BT_UART_RXD	NC	N/A	N/A	Close TP109 Open TP105
Option	11	DAT5	15	WL_HOST_WA KE	WL_IRQ	5	GPIO1	Open TP109 Close TP105

Table 4 DAT5 Pin Alternative Connection

To achieve this, disconnect TP109 and connect TP105.

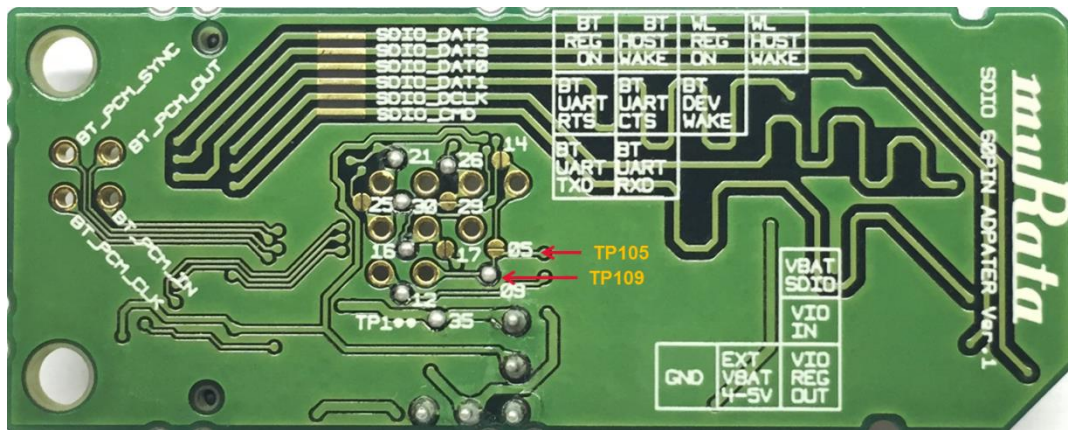


Figure 6 DAT5 Pin Alternative Connection

3.2.2 DAT6

DAT6 pin can be alternatively used to connect to SN8000 CM/SN8000UFL CM pin 17, which is connected to SN8000/SN8000UFL module pin 10, RST_N.

	MMC Pin #	Freescale i.MX EVK SD /MMC Pin	SN8000 CM/ Murata i.MX Interconnect Pin #	Murata i.MX Interconnect pin	SN8000 CM Signal	SN8000 Pin #	SN8000 Signal	Short-Pad Config
Default	12	DAT6	41	BT_UART_RTS	N/A	N/A	N/A	Close TP130 Open TP129
Option	12	DAT6	17	WL_REG_ON	WL_RST_N	10	RST_N	Open TP130 Close TP129

Table 5 DAT6 Pin Alternative Connection

To achieve this, disconnect TP130 and connect TP129.

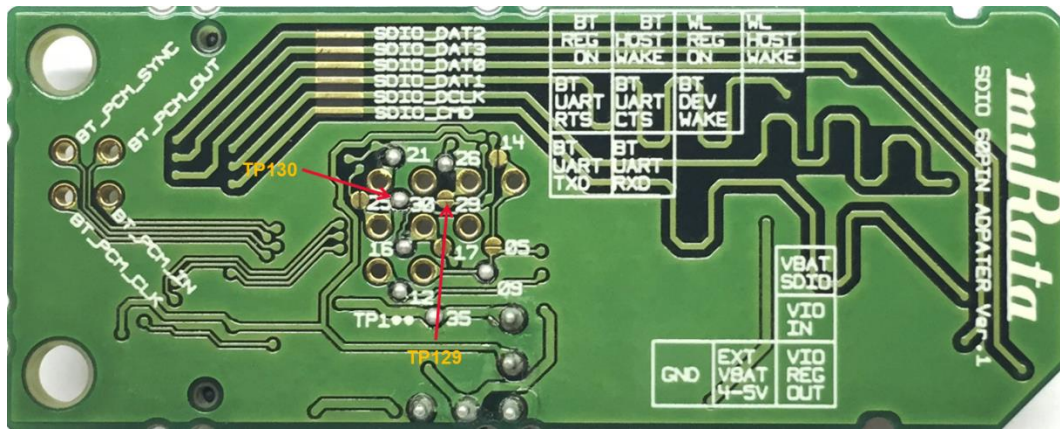


Figure 7 DAT6 Pin Alternative Connection

4 Connect to Freescale i.MX6

Before connect the SN8000CMK to i.MX6 development board, check and confirm the interface voltage that you are going to use and make sure the jumper is in the correct position as you want, see **Figure 8**. Connect VBAT_SDIO (TP122) and VIO_IN (TP123), the board is configured to take VBAT_SDIO 3.3V. Connect VIO_IN (TP123) and VIO_REG_OUT (TP124), VDD_IO is set to 1.8V.

NOTE: There is no place to print the label for TP122, TP123 and TP124. Please compare this section with the Murata i.MX Interconnect board schematic.

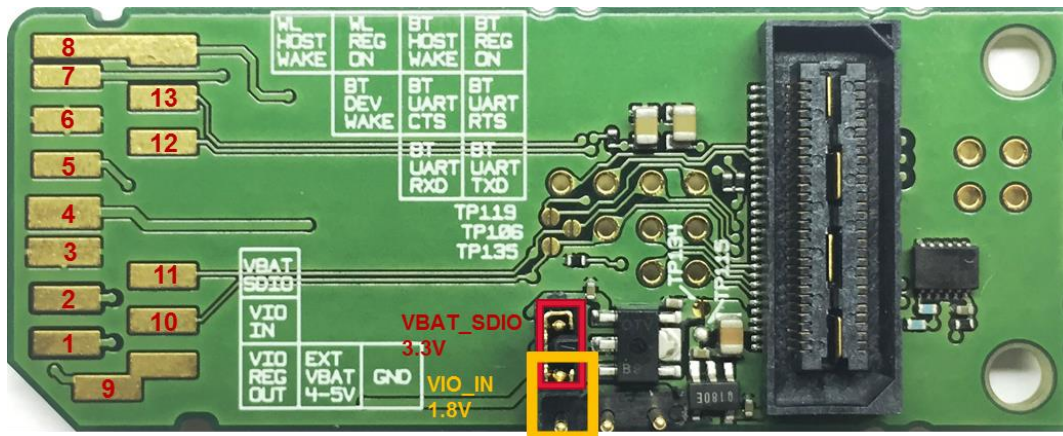


Figure 8 VIO_IN Jumper Selection

2.4 GHz Chip Antenna
& RF Switch Connector



SN8000 (BCM433362)

Murata Custom Interconnect
SDIO to 60PIN Adapter

i.MX6Q/DL Sabre Smart

Figure 9 Connect to i.MX6D/DL Sabre Smart

5 Errata

The TP133 is misprinted as TP135 on the bottom side of the Murata i.MX Interconnect board, see **Figure 10**.

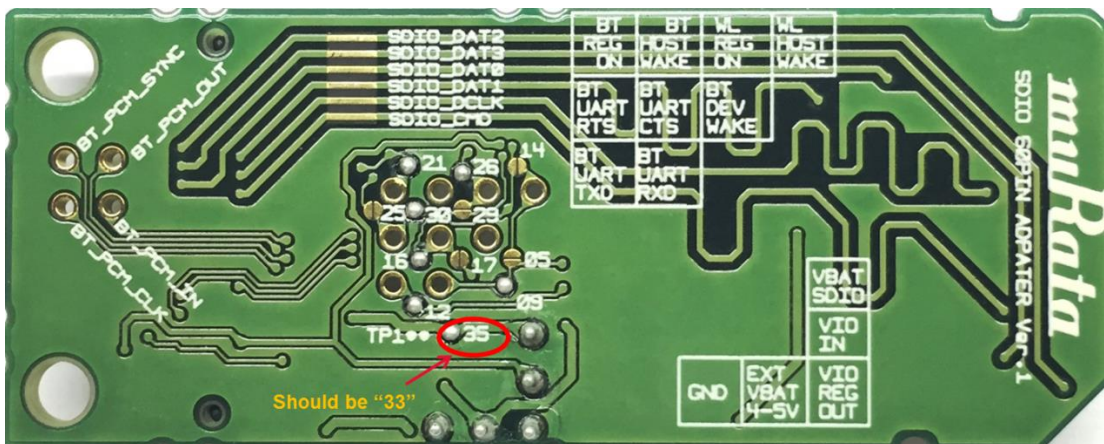


Figure 10 TP Label Misprint

6 Software

Driver of SN8000 is integrated in the i.MX6 the BSP. Please refer to Murata wireless website, <http://wireless.murata.com/wireless/iMX>, for details.

7 Technical Support Contact

Contact Wireless module application support at imxfag@murata.com

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