



# DIFFERENTIAL-TO-HSTL ZERO DELAY CLOCK GENERATOR

**ICS8725-21**

## General Description



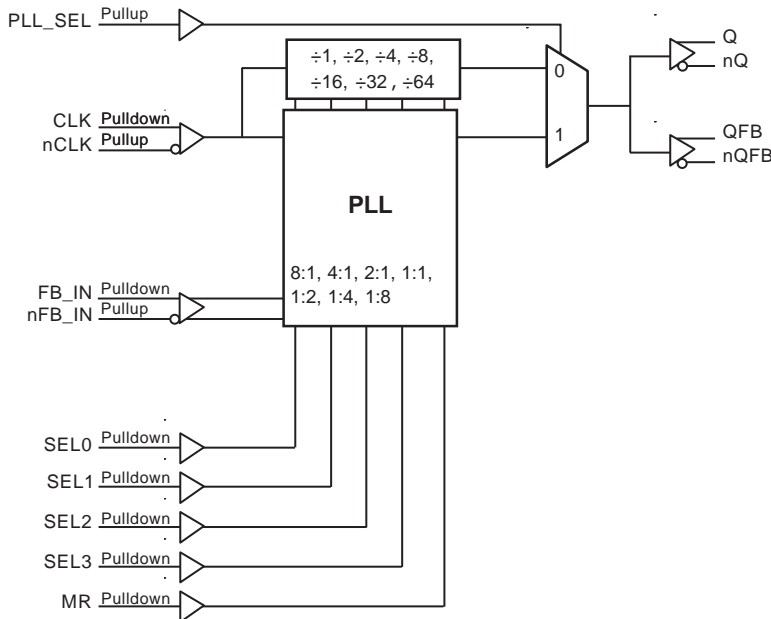
The ICS8725-21 is a highly versatile 1:1 Differential-to-HSTL Clock Generator and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. The CLK, nCLK pair can accept most standard differential input levels. The

ICS8725-21 has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider, and has an output frequency range of 31.25MHz to 630MHz. The reference divider, feedback divider and output divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve “zero delay” between the input clock and the output clocks. The PLL\_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

## Features

- One differential HSTL output pair  
One differential feedback output pair
- Differential CLK/nCLK input pair
- CLK/nCLK pair can accept the following differential input levels: LVPECL, LVDS, HSTL, HCSSL, SSTL
- Output frequency range: 31.25MHz to 630MHz
- Input frequency range: 31.25MHz to 630MHz
- VCO range: 250MHz to 630MHz
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- Cycle-to-cycle jitter: 35ps (maximum)
- Output skew: 50ps (maximum)
- Static phase offset: 30ps ± 125ps
- 3.3V core, 1.8V output operating supply
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages
- Industrial temperature information available upon request

## Block Diagram



## Pin Assignment

CLK	1	20	nc
nCLK	2	19	SEL1
MR	3	18	SEL0
VDD	4	17	VDD
nFB_IN	5	16	PLL_SEL
FB_IN	6	15	VDDA
SEL2	7	14	SEL3
GND	8	13	VDDO
nQFB	9	12	Q
QFB	10	11	nQ

**ICS8725-21**

**20-Lead SOIC**

**7.5mm x 12.8mm x 2.3mm package body**

**M Package**

**Top View**

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1	CLK	Input	Pulldown	Non-inverting differential clock input.
2	nCLK	Input	Pullup	Inverting differential clock input.
3	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Q and QFB to go low and the inverted outputs nQ and nQFB to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTTL interface levels.
4, 17	V <sub>DD</sub>	Power		Core supply pins.
5	nFB_IN	Input	Pullup	Inverting differential feedback input to phase detector for regenerating clocks with "Zero Delay." Connect to pin 9.
6	FB_IN	Input	Pulldown	Non-inverted differential feedback input to phase detector for regenerating clocks with "Zero Delay." Connect to pin 10.
7, 14, 18, 19	SEL2, SEL3, SEL0 SEL1	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTTL interface levels.
8	GND	Power		Power supply ground.
9, 10	nQFB, QFB	Output		Differential feedback output pair. HSTL interface levels.
11, 12	nQ/Q	Output		Differential output pair. HSTL interface levels.
13	V <sub>DDO</sub>	Power		Output supply pin.
15	V <sub>DDA</sub>	Power		Analog supply pin.
16	PLL_SEL	Input	Pullup	PLL select. Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. When HIGH, selects PLL. LVCMOS/LVTTTL interface levels.
20	nc	Unused		No connect.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

## Function Tables

Table 3A. Control Input Function Table

Inputs					Outputs PLL_SEL = 1 PLL Enable Mode
SEL3	SEL2	SEL1	SEL0	Reference Frequency Range (MHz)*	Q/nQ
0	0	0	0	250 - 630	÷1
0	0	0	1	125 - 315	÷1
0	0	1	0	62.5 - 157.5	÷1
0	0	1	1	31.25 - 78.75	÷1
0	1	0	0	250 - 630	÷2
0	1	0	1	125 - 315	÷2
0	1	1	0	62.5 - 157.5	÷2
0	1	1	1	31.25 - 78.75	÷4
1	0	0	0	125 - 315	÷4
1	0	0	1	250 - 630	÷8
1	0	1	0	125 - 315	x2
1	0	1	1	62.5 - 157.5	x2
1	1	0	0	31.25 - 78.75	x2
1	1	0	1	62.5 - 157.5	x4
1	1	1	0	31.25 - 78.75	x4
1	1	1	1	31.25 - 78.75	x8

\*NOTE: VCO frequency range for all configurations above is 250MHz to 630MHz.

Table 3B. PLL Bypass Function Table

Inputs				Outputs PLL_SEL = 0 PLL Bypass Mode
SEL3	SEL2	SEL1	SEL0	Q/nQ, QFB/nQFB
0z	0	0	0	÷4
0	0	0	1	÷4
0	0	1	0	÷4
0	0	1	1	÷8
0	1	0	0	÷8
0	1	0	1	÷8
0	1	1	0	÷16
0	1	1	1	÷16
1	0	0	0	÷32
1	0	0	1	÷64
1	0	1	0	÷2
1	0	1	1	÷2
1	1	0	0	÷4
1	1	0	1	÷1
1	1	1	0	÷2
1	1	1	1	÷1

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$	-0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	46.2°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{DDO}$	Output Supply Voltage		1.6	1.8	2.0	V
$I_{DD}$	Power Supply Current				137	mA
$I_{DDA}$	Analog Supply Current				17	mA
$I_{DDO}$	Output Supply Current			0		mA

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	SEL[0:3], MR	$V_{DD} = V_{IN} = 3.465V$		150	$\mu\text{A}$
		PLL_SEL	$V_{DD} = V_{IN} = 3.465V$		5	$\mu\text{A}$
$I_{IL}$	Input Low Current	SEL[0:3], MR	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		$\mu\text{A}$
		PLL_SEL	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		$\mu\text{A}$

**Table 4C. Differential DC Characteristics,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK, FB_IN	$V_{DD} = V_{IN} = 3.465V$		150	$\mu\text{A}$
		nCLK, nFB_IN	$V_{DD} = V_{IN} = 3.465V$		5	$\mu\text{A}$
$I_{IL}$	Input Low Current	CLK, FB_IN	$V_{DD} = 3.465V$ , $V_{IN} = 0V$	-5		$\mu\text{A}$
		nCLK, nFB_IN	$V_{DD} = 3.465V$ , $V_{IN} = 0V$	-150		$\mu\text{A}$
$V_{PP}$	Peak-to-Peak Voltage; NOTE 1		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		GND + 0.5		$V_{DD} - 0.85$	V

NOTE 1:  $V_{IL}$  should not be less than -0.3V.NOTE 2: Common mode input voltage is defined as  $V_{IH}$ .**Table 4D. HSTL DC Characteristics,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		1.0		1.4	V
$V_{OL}$	Output Low Voltage; NOTE 1		0		0.4	V
$V_{OX}$	Output Crossover Voltage; NOTE 2		40		60	%
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.1	V

NOTE 1: Outputs termination with  $50\Omega$  to ground.

NOTE 2: Defined with respect to output voltage swing at a given condition.

**Table 5. Input Frequency Characteristics,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units	
$F_{IN}$	Input Frequency	CLK, nCLK	PLL_SEL = 1	31.25		630	MHz
			PLL_SEL = 0			630	MHz

## AC Electrical Characteristics

**Table 6. AC Characteristics,  $V_{DD} = V_{DDA} = 3.3V \pm 5\%$ ,  $V_{DDO} = 1.8V \pm 0.2V$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$**

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				630	MHz
$t_{PD}$	Propagation Delay; NOTE 1	PLL_SEL = 0V, $f \leq 700\text{MHz}$	3.2		4.5	ns
$t_{sk}(\emptyset)$	Static Phase Offset; NOTE 2, 5	PLL_SEL = 3.3V	-95	30	155	ps
$t_{sk}(o)$	Output Skew; NOTE 3, 5	PLL_SEL = 0V			50	ps
$f_{jit}(cc)$	Cycle-to-Cycle Jitter; NOTE 5, 6				35	ps
$f_{jit}(\theta)$	Phase Jitter; NOTE 4, 5, 6				$\pm 50$	ps
$t_L$	PLL Lock Time				1	ms
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	300		700	ps
$t_{PW}$	Output Pulse Width		$t_{PERIOD}/2 - 85$	$t_{PERIOD}/2$	$t_{PERIOD}/2 + 85$	ps

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.

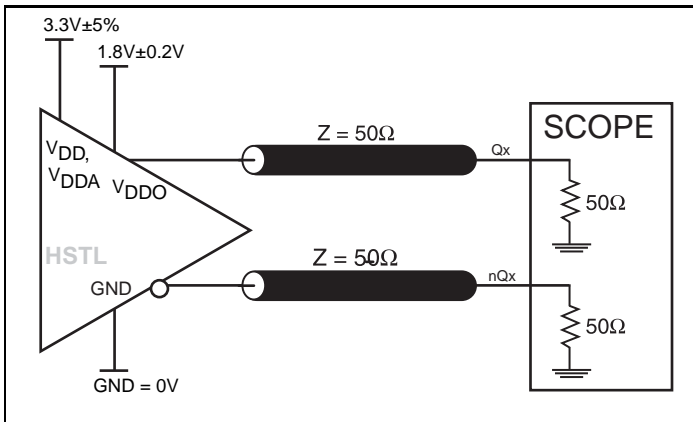
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 4: Phase jitter is dependent on the input source used.

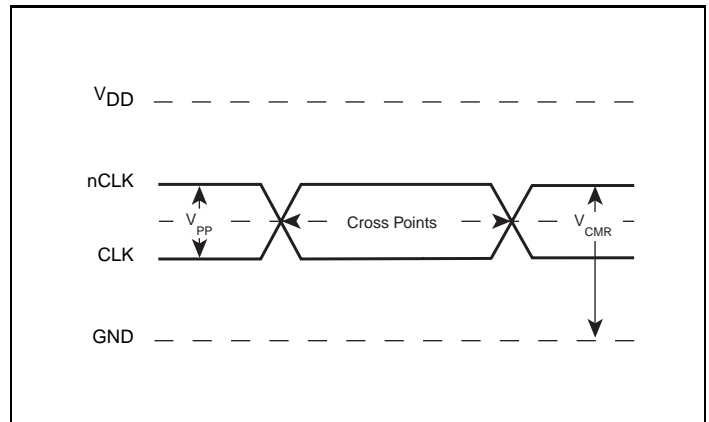
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6: Characterized at VCO frequency of 622MHz.

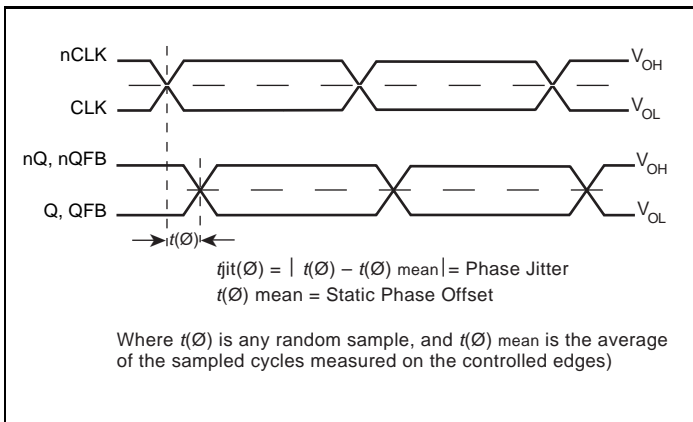
### Parameter Measurement Information



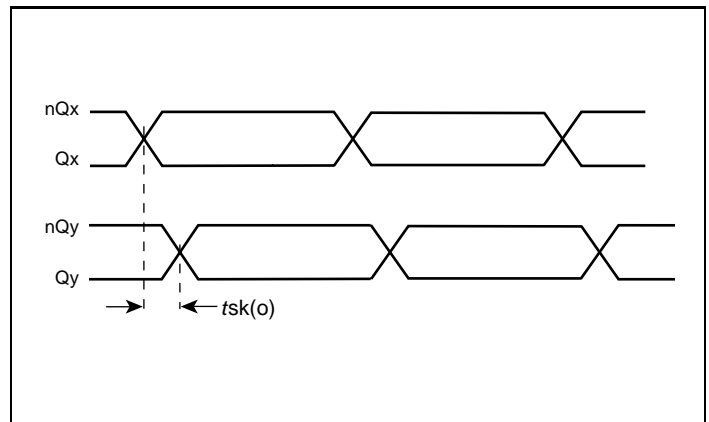
3.3V Core/1.8V Output Load AC Test Circuit



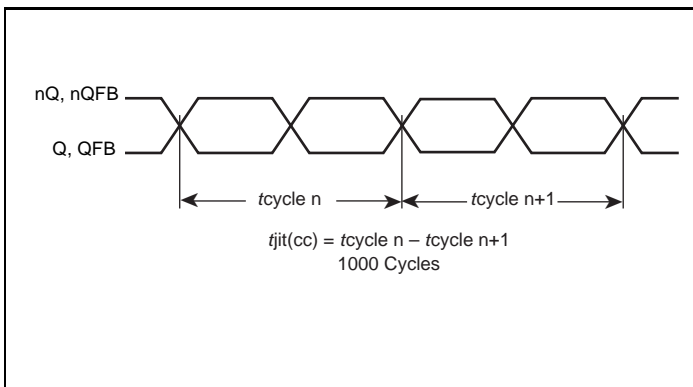
Differential Input Level



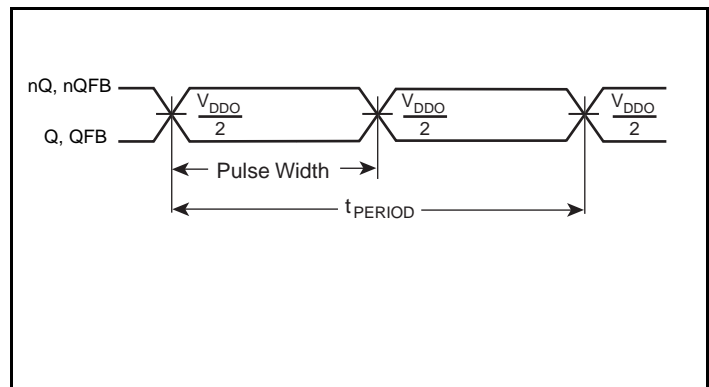
Phase Jitter and Static Phase Offset



Output Skew



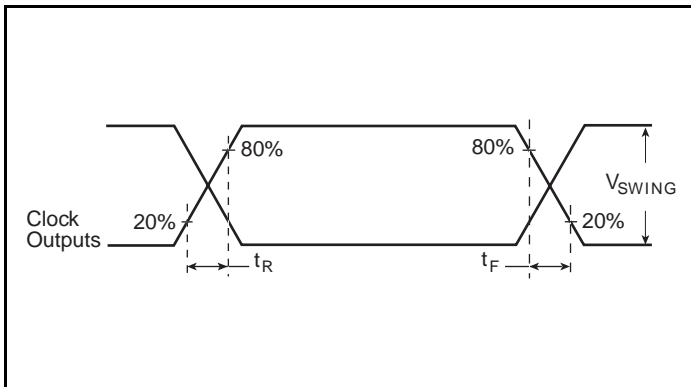
Cycle-to-Cycle Jitter



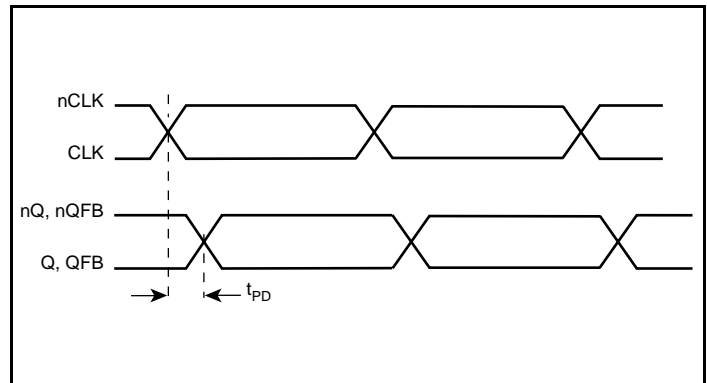
Output Pulse Width



## Parameter Measurement Information, continued



Output Rise/Fall Time



Propagation Delay

## Application Information

### Power Supply Filtering Technique

To achieve optimum jitter performance, power supply isolation is required. The ICS8725-21 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{DD}$ ,  $V_{DDA}$  and  $V_{DDO}$  should be individually connected to the power supply plane through vias, and  $0.01\mu\text{F}$  bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic  $V_{DD}$  pin and also shows that  $V_{DDA}$  requires that an additional  $10\Omega$  resistor along with a  $10\mu\text{F}$  bypass capacitor be connected to the  $V_{DDA}$  pin. The  $10\Omega$  resistor can also be replaced by a ferrite bead.

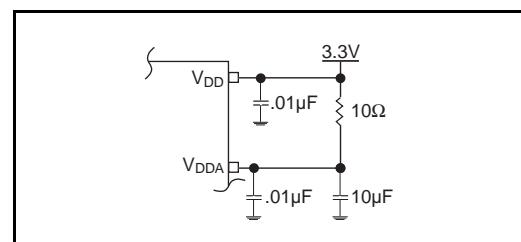


Figure 1. Power Supply Filtering

## Recommendations for Unused Input Pins

### Inputs:

#### LVC MOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

## Wiring the Differential Input to Accept Single Ended Levels

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} = V_{DD}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{DD} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

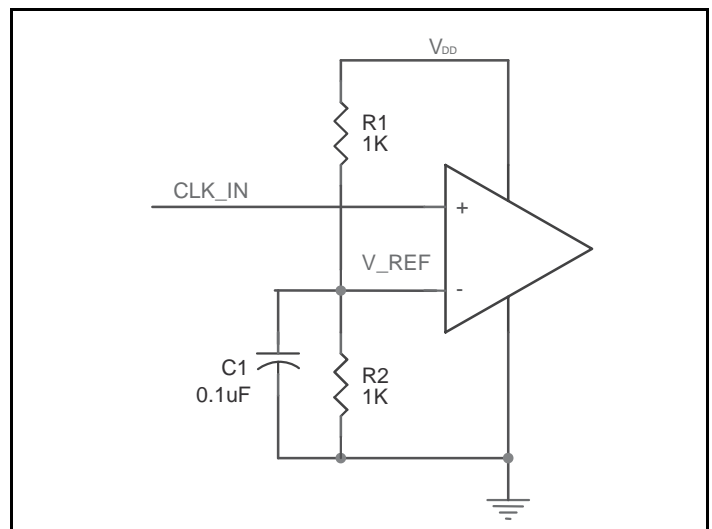
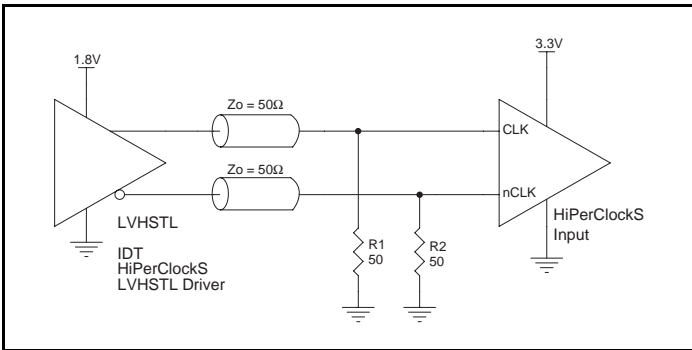


Figure 2. Single-Ended Signal Driving Differential Input

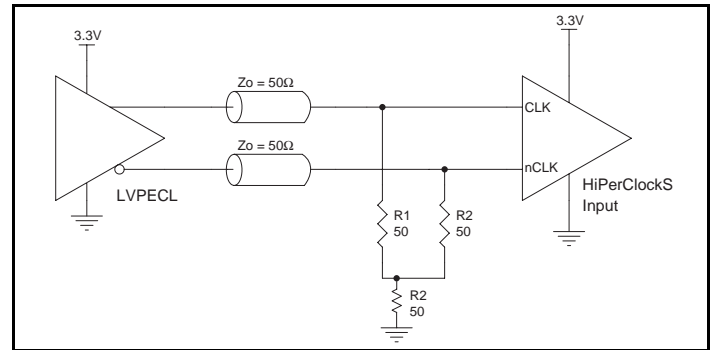
### Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3F show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver

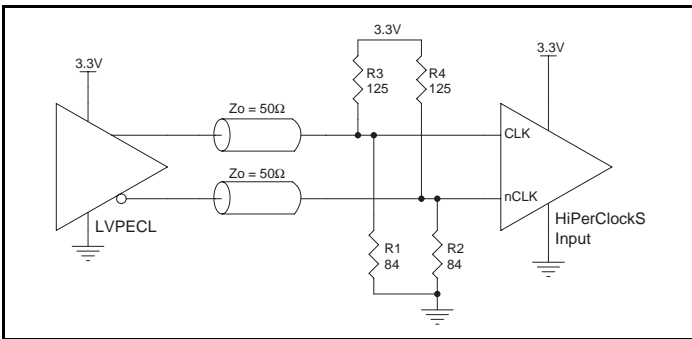
component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



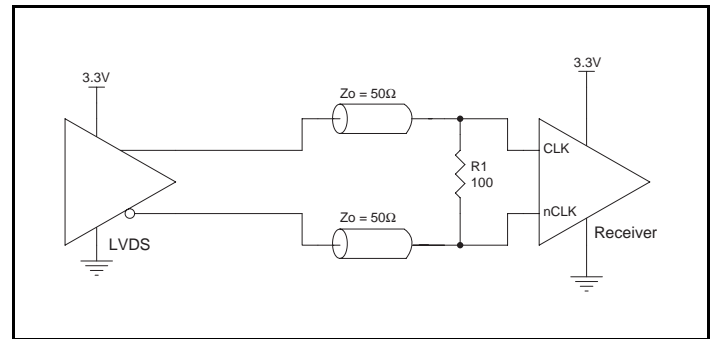
**Figure 3A. HiPerClockS CLK/nCLK Input Driven by an IDT Open Emitter HiPerClockS LVHSTL Driver**



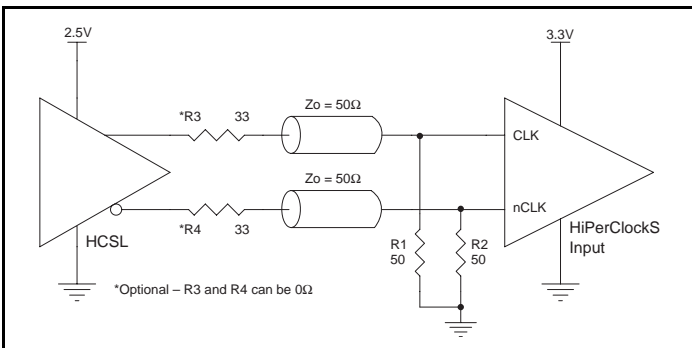
**Figure 3B. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



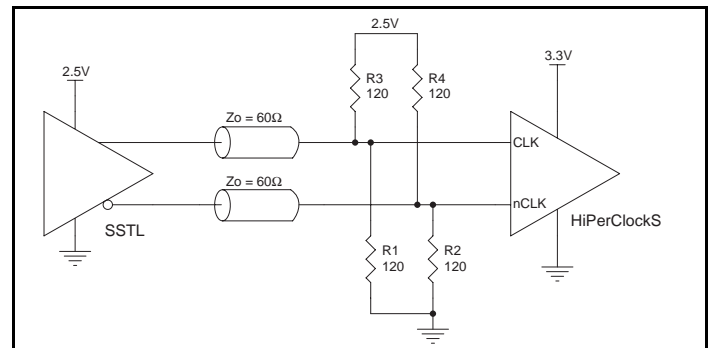
**Figure 3C. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVPECL Driver**



**Figure 3D. HiPerClockS CLK/nCLK Input Driven by a 3.3V LVDS Driver**



**Figure 3E. HiPerClockS CLK/nCLK Input Driven by a 3.3V HCSL Driver**



**Figure 3F. HiPerClockS CLK/nCLK Input Driven by a 2.5V SSTL Driver**

### Schematic Example

Figure 4 shows a schematic example of the ICS8725-21. In this example, the input is driven by an HCSL driver. The zero delay buffer is configured to operate at 155.52MHz input and 77.75MHz output. The logic control pins are configured as follows:

SEL[3:0] = 0101

PLL\_SEL = 1

For ICS8725-21, the decoupling capacitors should be physically located near the power pin.

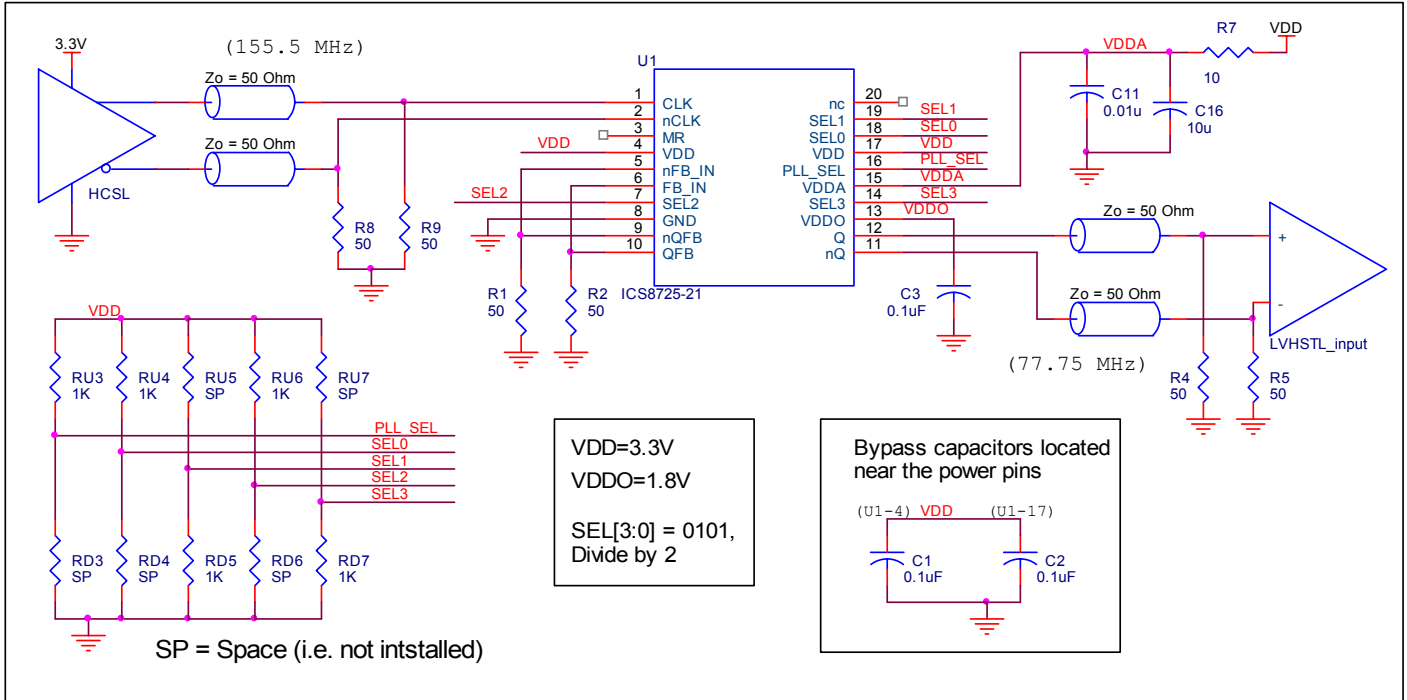


Figure 4. ICS8725-21 HSTL Buffer Schematic Example

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8725-21. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8725-21 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX}) = 3.465V * (137mA + 17mA) = 533.6mW$
- Power (outputs)<sub>MAX</sub> = **32.8mW/Loaded Output pair**

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) =  $533.6mW + 32.8mW = 566.4mW$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 39.7°C/W per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.566\text{W} * 39.7^\circ\text{C/W} = 111^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

**Table 7. Thermal Resistance  $\theta_{JA}$  for 20 Lead SOIC, Forced Convection**

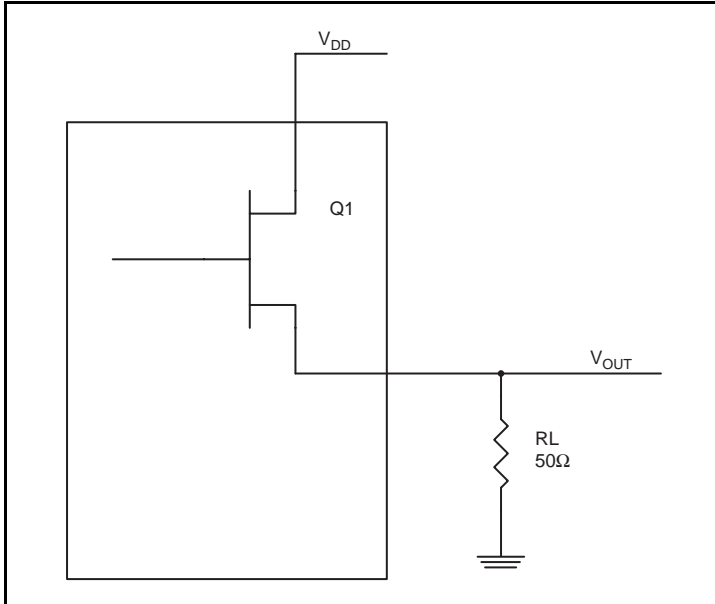
$\theta_{JA}$ vs. Air Flow			
Linear Feet per Minute	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 5*.



**Figure 5. HSTL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a  $50\Omega$  load.

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = (V_{OH\_MAX} / R_L) * (V_{DDO\_MAX} - V_{OH\_MAX})$$

$$Pd\_L = (V_{OL\_MAX} / R_L) * (V_{DDO\_MAX} - V_{OL\_MAX})$$

$$Pd\_H = (1.0V / 50\Omega) * (2V - 1.0V) = \mathbf{20mW}$$

$$Pd\_L = (0.4V / 50\Omega) * (2V - 0.4V) = \mathbf{12.8mW}$$

$$\text{Total Power Dissipation per output pair} = Pd\_H + Pd\_L = \mathbf{32.8mW}$$

### Reliability Information

Table 8.  $\theta_{JA}$  vs. Air Flow Table for a 20 Lead TSSOP

$\theta_{JA}$ vs. Air Flow			
Linear Feet per Minute	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### Transistor Count

The transistor count for ICS8725-21 is: 2969

### Package Outline and Package Dimensions

Package Outline - M Suffix for 20 Lead SOIC

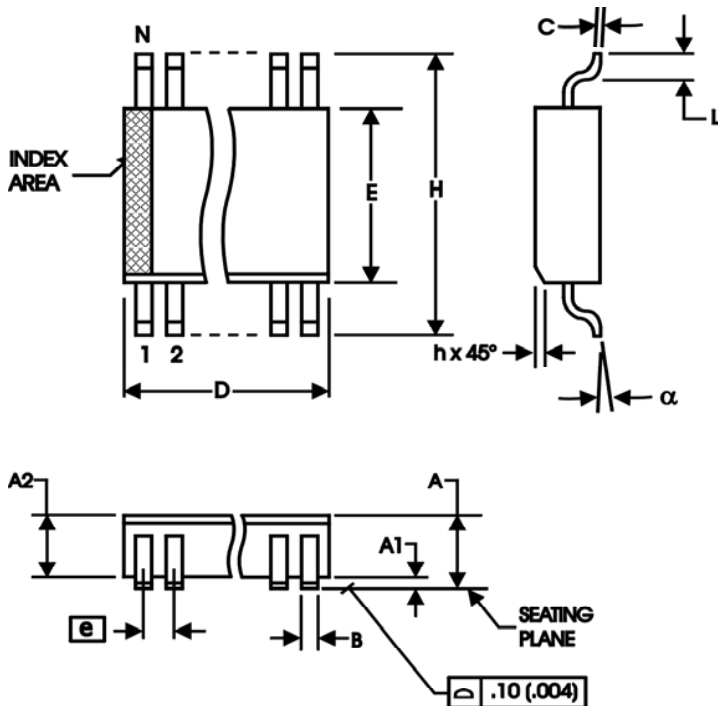


Table 9. Package Dimensions for 20 Lead SOIC

300 Millimeters All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	20	
A		2.65
A1	0.10	
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	12.60	13.00
E	7.40	7.60
e	1.27 Basic	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
$\alpha$	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MS-119

## Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8725AM-21	ICS8725AM-21	20 Lead SOIC	Tube	0°C to 70°C
ICS8725AM-21T	ICS8725AM-21	20 Lead SOIC	1000 Tape & Reel	0°C to 70°C
ICS8725AM-21LF	ICS8725AM-21LF	"Lead-Free" 20 Lead SOIC	Tube	0°C to 70°C
ICS8725AM-21LFT	ICS8725AM-21LF	"Lead-Free" 20 Lead SOIC	1000 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T10	14	Ordering Information Table - added Lead-Free marking and note.	6/9/05
A	T1	2 8	Pin Descriptions Table - corrected MR description. Added Recommendations for Unused Input and Output Pins.	5/22/06
A		11 12	Updated <i>Differential Clock Input Interface</i> section. Updated <i>Schematic Example</i> section.	2/27/08

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