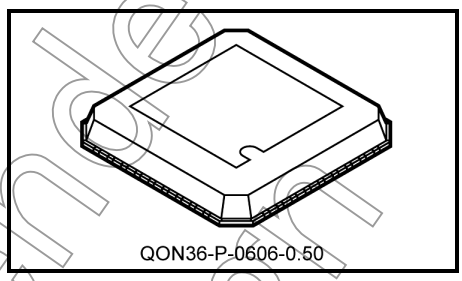
TOSHIBA BiCD Integrated Circuit Silicon Monolithic

TB6596FLG

DC and Stepping Motor Driver IC



Weight: 0.08 g (typ.)

The TB6596FLG is a DC motor driver IC using LDMOS output transistors with low ON-resistance.

The TB6596FLG incorporates one PWM-constant-current H-bridge driver, four direct-PWM-controlled H-bridge drivers, and also one linear constant-current H-bridge driver. The TB6596FLG is best suited to control various lens actuators in digital still cameras.

The three-wire serial interface provides control over the drivers, thus reducing the number of lines required for interfacing with the control IC.

Features

- Motor power supply voltage: $V_M \leq 6$ V (max)
- Control power supply voltage: V_{CC} = 3 to 6 V
- Output current: $I_{OUT} \leq 0.8$ A (max)
- Complementary P- and N-channel LDMOS output transistors
- Output ON-resistance: Ron (upper and lower sum) = 1.5 Ω (typ.)

Channel E: DC Motor Driver
- High-speed PWM control at several hundred kHz
- Motor control method can be selected from the following two with the serial data inputs:
  1. Controls motor speed by using both a frequency-locked-loop (FLL) speed discriminator that compares the FG and CLK signals, and an integrator.
     (Typical speed = Between 250 Hz and 1750 Hz in 16 steps.)
  2. Controls H-bridge by using a direct PWM input.
- Two power switching transistors for optical encoder

Channel A and B or Channel C and D: Stepping Motor Driver
- Four H-bridge drivers (channel A and B, channel C and D) for direct PWM control.
  (Capable of controlling up to two 2-phase bipolar stepping motors or four DC motors.)

Channel F: Shutter Driver
- Linear constant-current drivers
- Current ramp-up rate control for improving the dependency of a current ramp-up slope on supply voltage change at startup and also for improving its reproducibility.
  (Increases current in up to 32 steps by using the internal CLK, which is derived by dividing CLK by 1 to 16.)

Other Features
- Two 6-bit DACs provide reference values for each constant-current limiters
- Dedicated standby (power-save) pin
- Thermal shutdown (TSD): Disables the output bias generator when the internal junction temperature exceeds 170°C.
- Undervoltage lockout (UVLO): Resets and disables the internal circuitry when V_{CC} falls below 2.2 V (typ.)
- Small QON-36 package (0.5-mm lead pitch)
- Compatible with Pb-free reflow soldering

Note: This product has a MOS structure and is sensitive to electrostatic discharge. When handling this product, ensure that the environment is protected against electrostatic discharge by using an earth strap, a conductive mat and an ionizer. Ensure also that the ambient temperature and relative humidity are maintained at reasonable levels.

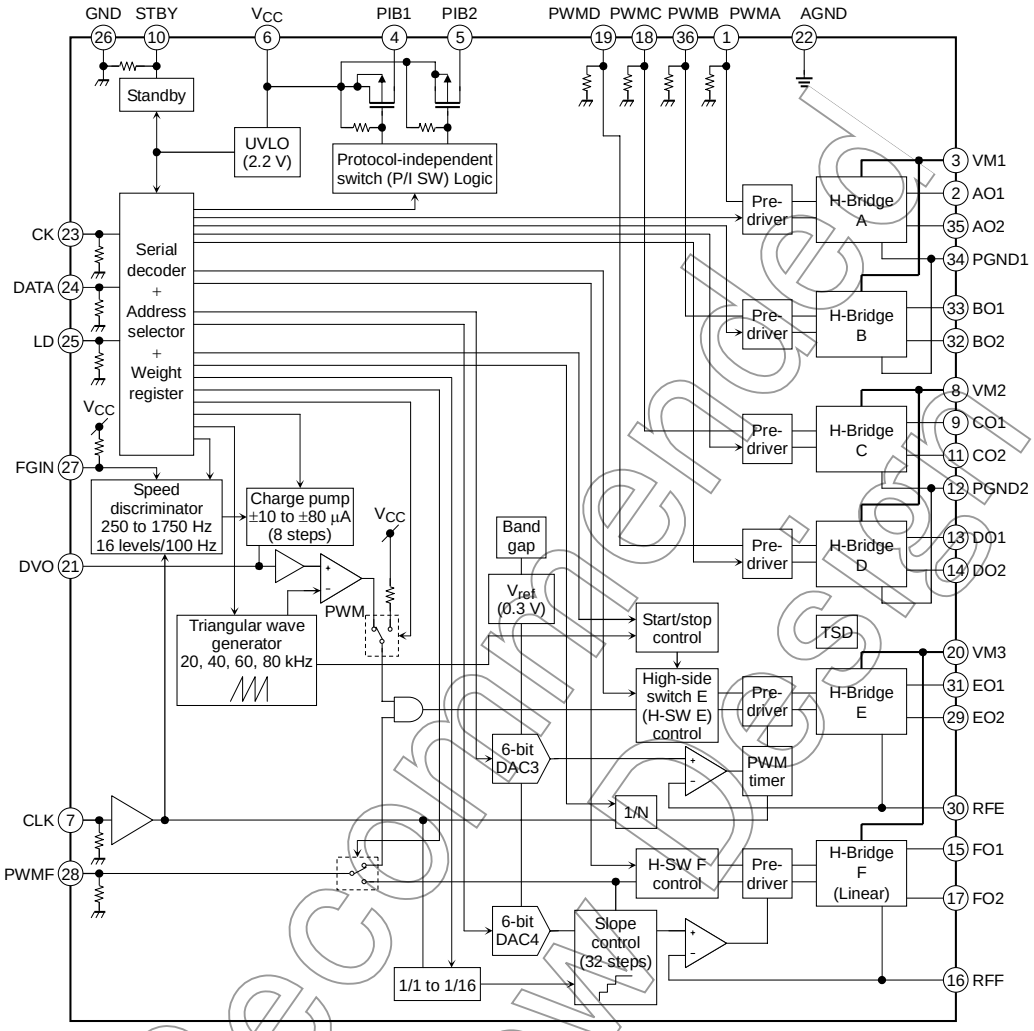
About solderability, following conditions were confirmed

- Solderability

  (1) Use of Sn-37Pb solder Bath
  - solder bath temperature = 230°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

  (2) Use of Sn-3.0Ag-0.5Cu solder Bath
  - solder bath temperature = 245°C
  - dipping time = 5 seconds
  - the number of times = once
  - use of R-type flux

Block Diagram



Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	Remarks
Supply voltage		V_{CC}	6	V	V_{CC}
Motor supply voltage		V_M	6	V	V_M
Output voltage		V_{OUT}	6	V	
Output current	H-SW	I_{OUT}	0.8	A	
	PI SW Tr.	I_D	0.1		PIB1, PIB2
Input voltage		V_{IN}	−0.2 to 6	V	Control input pins
Power dissipation		P_D	0.6	W	IC only
			1.04		(Note)
Operating temperature		T_{opr}	−20 to 85	°C	
Storage temperature		T_{stg}	−55 to 150	°C	

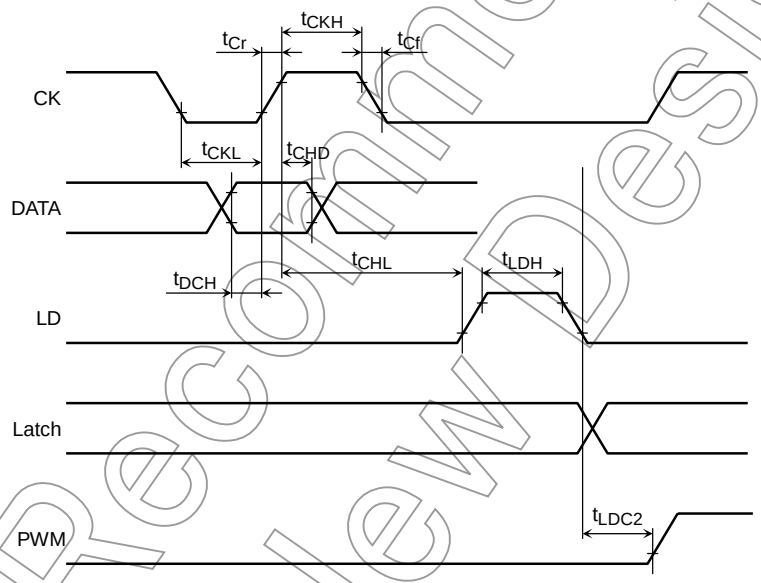
Note: When mounted on a glass epoxy single-sided PCB (size: 50 mm × 50 mm × 1.6 mm) with a 40% dissipating copper surface.

Operating Ranges (Ta = –20 to 85°C)

Characteristics		Symbol	Rating			Unit	Remarks
			Min	Typ.	Max		
Supply voltage for small-signal circuitry		V_{CC}	3	3.3	5.5	V	
Motor supply voltage		V_M	2.2	3.3	5.5	V	
Output current	H-SW	I_{OUT}	—	—	600	mA	V_M = 3 to 5.5 V
			—	—	350		2.2 V ≤ V_M < 3 V
	PI SW Transistors	I_D	—	—	30		
PWM frequency (Channels A to E)		f_{PWM}	—	—	100	kHz	
CLK driver frequency		f_{CLK}	—	1	5	MHz	

Operating Ranges: Serial Data Controller (Ta = –20 to 85°C)

Characteristics	Symbol	Rating		Unit
		Min	Max	
Clock pulse width Low	t_{CKL}	200	—	ns
Clock pulse width High	t_{CKH}	200	—	ns
Clock rise time	t_{Cr}	—	50	ns
Clock fall time	t_{Cf}	—	50	ns
Data setup time	t_{DCH}	30	—	ns
Data hold time	t_{CHD}	60	—	ns
CK to LD rising edge	t_{CHL}	200	—	ns
LD to PWM delay	t_{LDC2}	100	—	ns
Load pulse width High	t_{LDH}	2	—	μs
CK (clock pulse) frequency	f_{CLK}	—	2.5	MHz



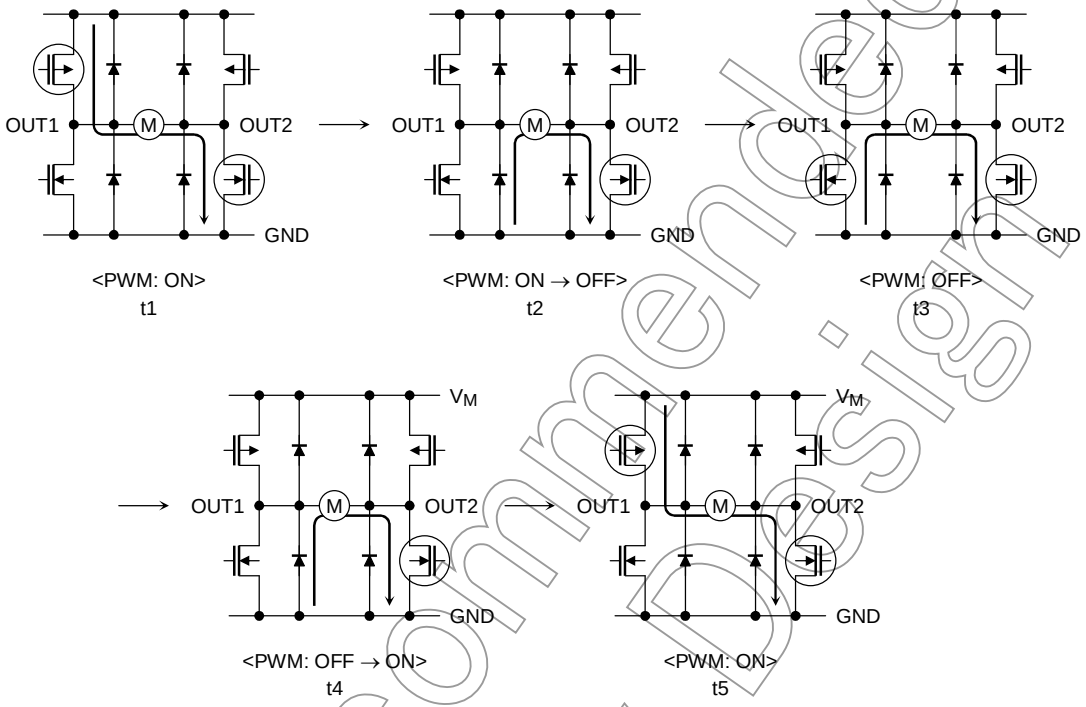
Principle of Operation

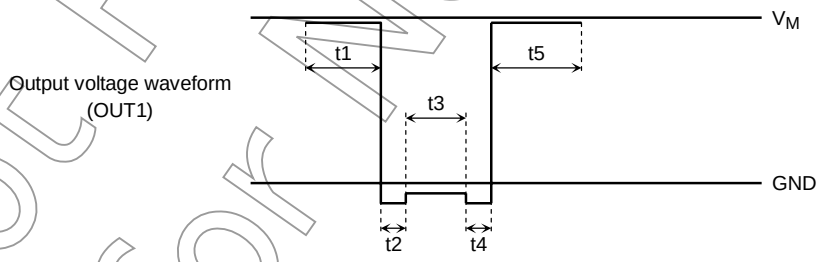
Bridge Outputs: Basic operation of channels A through E

PWM Control

In PWM constant-current mode, the PWM chopper circuit alternates between on (t1, t5) and short brake (t3).

(To eliminate shoot-through current, a dead time (t2, t4) is inserted when the PWM is turned on and off.)





Constant-Current Bridge Driver (Channel E): PWM constant-current choppers

The TB6596FLG has PWM choppers with a constant turn-off period.

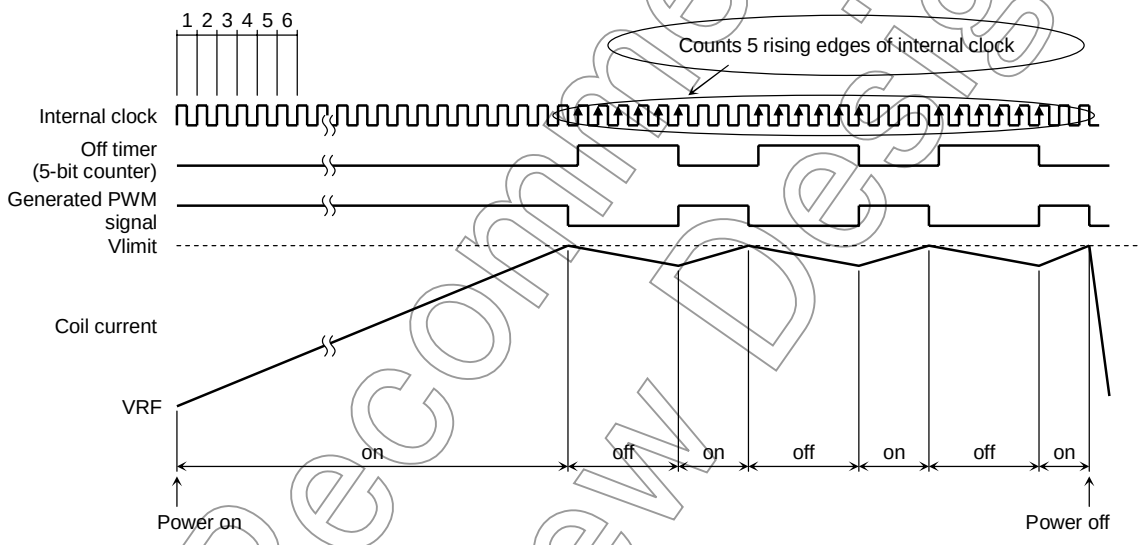
The turn-off period is measured by counting the number of rising edges of an internal clock signal, which is generated by dividing the external CLK signal. The turn-off period can be adjusted by changing either the CLK frequency or the number of its rising edges counted (three or five counts; the default is five counts).

Turning on the power supply causes a current to flow into the motor coils. The peak current through the winding is sensed via an external current-sensing resistor. As the current increases, a voltage (VRF) develops across the resistor, which is fed back to the internal comparator. At the predetermined reference voltage (Vlimit: current limiting voltage), the comparator turns off (chops) the power supply.

When high-side output transistors are turned off, the TB6596FLG, by default, counts five rising edges of the internal clock signal as a turn-off period. (The counter resets at the sixth rising edge of the clock.)

Based on this turn-off period, the TB6596FLG generates a PWM signal that turns on and off the output transistors.

Timing Diagram of the PWM Constant-Current Chopper Circuit with the Default Turn-Off Period



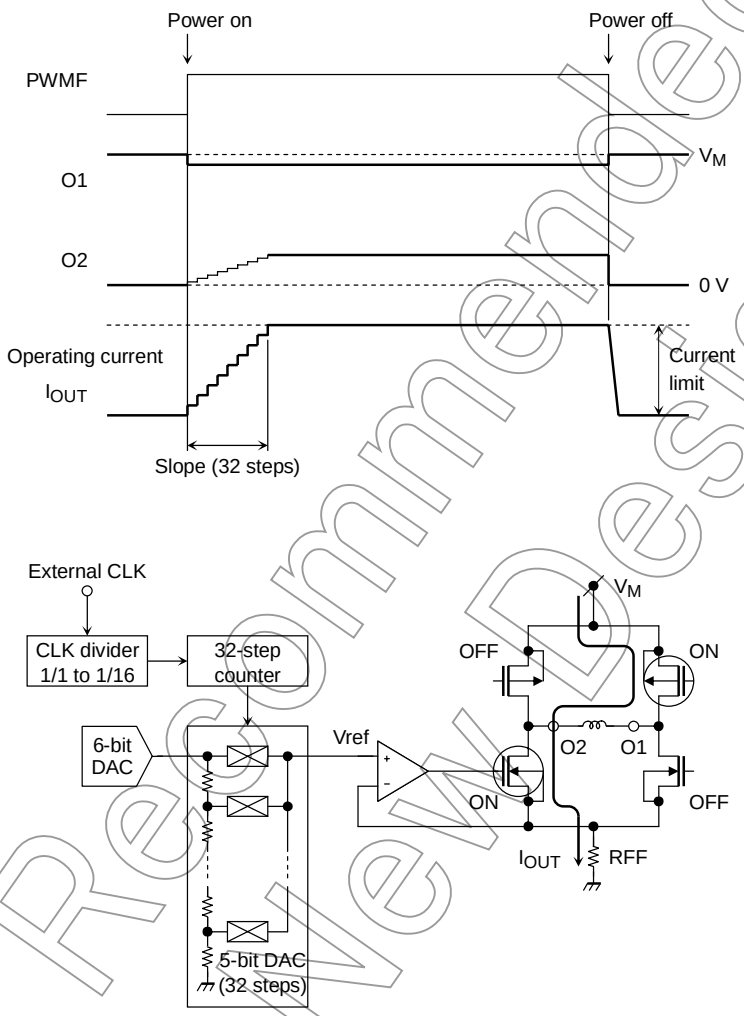
(The upper limit of the coil current (IO peak) can be calculated as: IO = Vlimit/RNF.)

Linear Constant-Current Bridge: Channel F

This bridge driver circuit is tuned on and off by setting the PEMF pin High and Low, respectively.

The driver output current is converted to a voltage through the external resistor RFF and fed back to a sense amplifier, thus creating a negative feedback loop. This enables the constant-current drive using the low-side driver.

The constant-current value is adjusted by changing the Vref input to the sense amplifier, which is specified by an internal 6-bit DAC (max = 0.3 V).

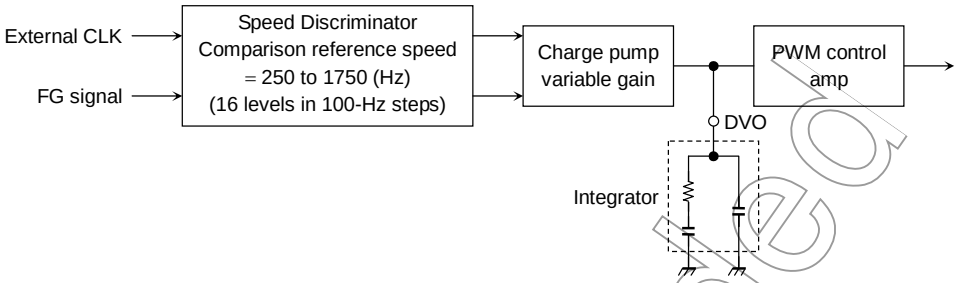


*Current ramp-up rate controller:

To improve the dependency of a current ramp-up slope on supply voltage change at startup and its reproducibility according to the time constant of the coil, the reference voltage for the comparator is increased using a 5-bit DAC (in 32 steps) up to the current limit. This can stabilize the reproducibility of a current ramp-up slope.

The current ramp-up rate is specified by dividing an external CLK. The frequency divider ratio can be selected from 16 options (1/1 to 1/16) by using 4-bit serial data inputs.

Speed Control

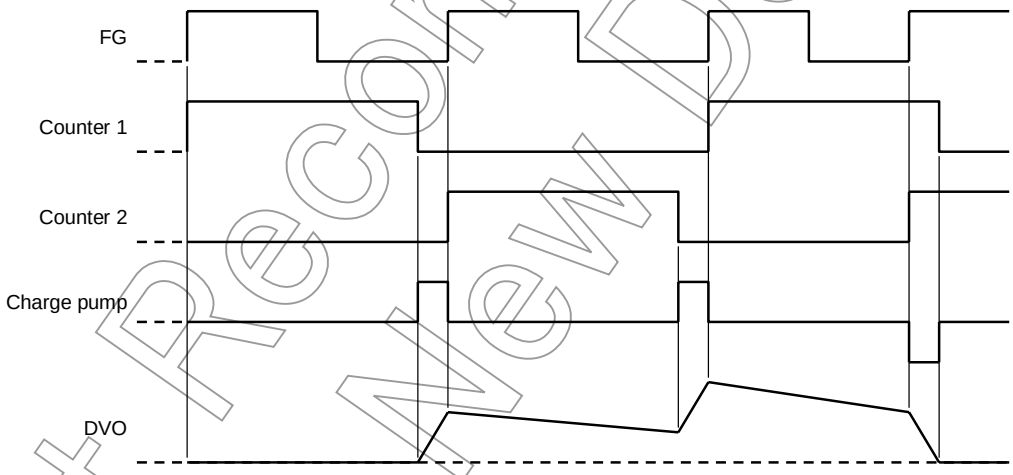


- The FLL speed discriminator compares the FG signal against the reference speed which is derived from an external CLK.
- The speed discriminator has two counters that alternately count one cycle of the FG signal. It then generates error pulses (charge and discharge) according to the frequency difference. Based on these pulses, the integrator (set by an external RC) and the PWM control amplifier generates a motor drive output signal to control the motor rotational speed.
- The reference speed of the speed discriminator is selectable from 16 levels between 250 and 1750 Hz in 100-Hz steps. (It is selected by serial data inputs.)
- The motor rotation speed (N) is calculated by the following equation:

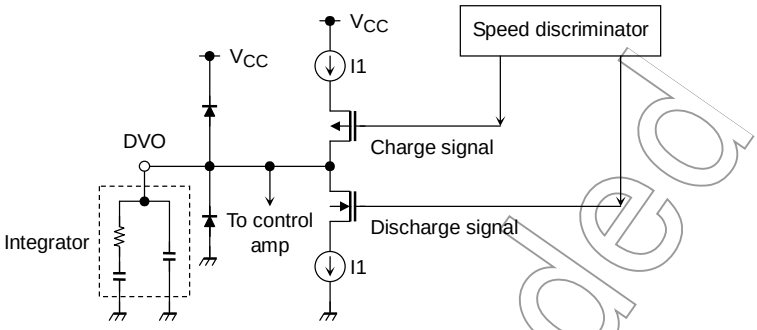
  $N\ (rpm) = f_{CLK}\ (Hz)/CT \times 60/Z$

  Z: Number of FG pulses per rotor rotation

  CT: Speed discriminator count



Charge Pump Circuit

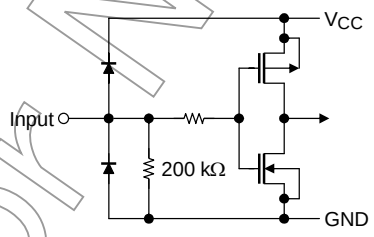


- Consisting of CMOS transistors, this charge pump achieves a high resolution of the speed control signal.
- The gain of the speed discriminator can be internally selected from eight combinations of charging and discharging current values (±10 to 80 μA). And the total control gain is determined by adjusting the charge pump current and the time constant of the external integrator.
- When the motor is not rotating, this circuit remains in discharge mode (–50 μA). Thus, the amount of charge stored in a capacitor of the external integrator becomes zero resetting the analog control value.
- Since the FG signal is not generated immediately after the PWME drive signal assertion due to the stationary motor, the speed control loop is not enabled at this time. Therefore, the forced commutation signal (Duty cycle = 100%) is applied as a motor driving signal for a short period of time from the rising edge of the PWME signal.
  - * The motor startup time can be selected from 64 options (0 to 63) in 2.048-ms steps by a 6-bit serial command.
- For powering off, the motor operation of a certain period of time after the falling edge of the PWM signal can be selected from the brake and the reverse-plus-brake modes.
  - * The reverse rotation time can be selected from 64 options (0 to 63) in 2.048-ms steps by a 6-bit serial command.

Input Pins:

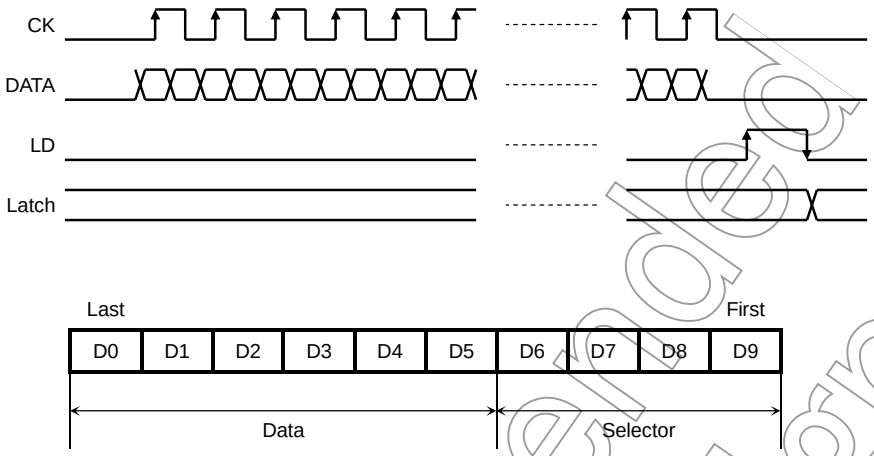
All input pins (CK, DATA, LD, PWME, PWMF, STBY, CLK) have a pull-down resistor of about 200 kΩ. The FGIN pin is pulled up to V_{CC} via a pull-up resistor of about 200 kΩ.

CK, DATA, LD, PWMA, B, C, D, PWMF, STBY, CLK



Serial Data Format

10-Bit Serial Data



Each Resister Mode

D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Address
0	0	0	0	p2a	p2b	p1a	p1b	—	—	0
0	0	0	1	mod2	mod1	pm2	pm1	—	—	1
0	0	1	0	p4a	p4b	p3a	p3b	—	—	2
0	0	1	1	mod4	mod3	pm4	pm3	—	—	3
0	1	0	0	Reverse brake time(0 to 127 ms)						4
0	1	0	1	p5a	p5b	vc	pms	sw2	sw1	5
0	1	1	0	mod5	pm5	If5	Charge pump gain (3 bits)			6
0	1	1	1	Target speed value (4 bits)				Carrier frequency		7
1	0	0	0	Forced commutation time for startup (0 to 127 ms)						8
1	0	0	1	DA5 (6 bits): Sets the current level for channel E						9
1	0	1	0	p6a	p6b	Constant-current ramp-up rate (4 bits)				10
1	0	1	1	mod6	pm6	If6	—	—	—	11
1	1	0	0	DA6 (6 bits): Sets the current level for channel F						12
1	1	0	1	—	—	—	—	—	—	13
1	1	1	0	—	—	—	—	—	—	14
1	1	1	1	—	—	—	off	—	—	15

Ifx: Current control for channels E and F (0 = Enable; 1 = Disable)
Pms: Channel switching of the PMW input (0 = channel E; 1 = channel F)
Off: Chop-off count (0 = 5 internal clock cycles, 1 = 3 internal clock cycles)
Swx: Turns on/off SW1 and SW2 (0 = off; 1 = on)
Vc: Channel E control mode (0 = External PWM control; 1 = Internal FLL speed control)
Reverse brake: Sets the reverse brake time to be 2.048 ms × specified value
Forced commutation time for startup: Full drive for a period of 2.048 ms × specified value after startup
Charge pump gain: These 3 bits specify the gain of the charge pump to one of the 8 levels between ±10 μA to ±80 μA in 10-μA steps.
Career frequency: These 2 bits specify the triangular wave frequency to one of the frequencies: 20 kHz, 40 kHz, 60 kHz and 80 kHz.
Speed target: These 4 bits specify the speed target value to any of the 16 speed between 250 Hz to 1750 Hz in 100-Hz steps.
Constant-current ramp-up rate: Controls the current ramp-up slope for channel F by changing the number of

internal clock cycle count. (0 to 15 cycles: Steps up the DAC output voltage at every specified count.)

(*) Address 15 setting

(1) All register data are cleared (set to "0") if user set all "0" at address 15. Avoid the setting all"0" at the address ,or set at other address after setting at address 15.
(Chop-off count should be 5 clock cycles in default state means even without setting at this.)

(2) D1 and D0 in address 15 are forbidden area. Avoid setting "1" at D1 and D0.

Driver Operating Modes

modx = 0, pmx = 0

pxa	pxb	PMx	OUTxA	OUTxB	Driving Mode
0	0	X	Z	Z	Stop
0	1	L	L	L	Short brake
0	1	H	L	H	Reverse
1	0	L	L	L	Short brake
1	0	H	H	L	Forward
1	1	X	L	L	Short brake

modx = 0, pmx = 1

pxa	pxb	PMx	OUTxA	OUTxB	Driving Mode
0	0	X	Z	Z	Stop
0	1	L	L	H	Reverse
0	1	H	L	L	Short brake
1	0	L	H	L	Forward
1	0	H	L	L	Short brake
1	1	X	L	L	Short brake

modx = 1, pmx = X

pxa	pxb	PMx	OUTxA	OUTxB	Driving Mode
0	X	X	Z	Z	STOP
1	0	L	H	L	Forward
1	0	H	L	H	Reverse
1	1	X	L	L	Short brake

Note: Only valid for channel E. (Reverse brake function)

- When short brake mode is selected, the motor operation is controlled in the following sequence.

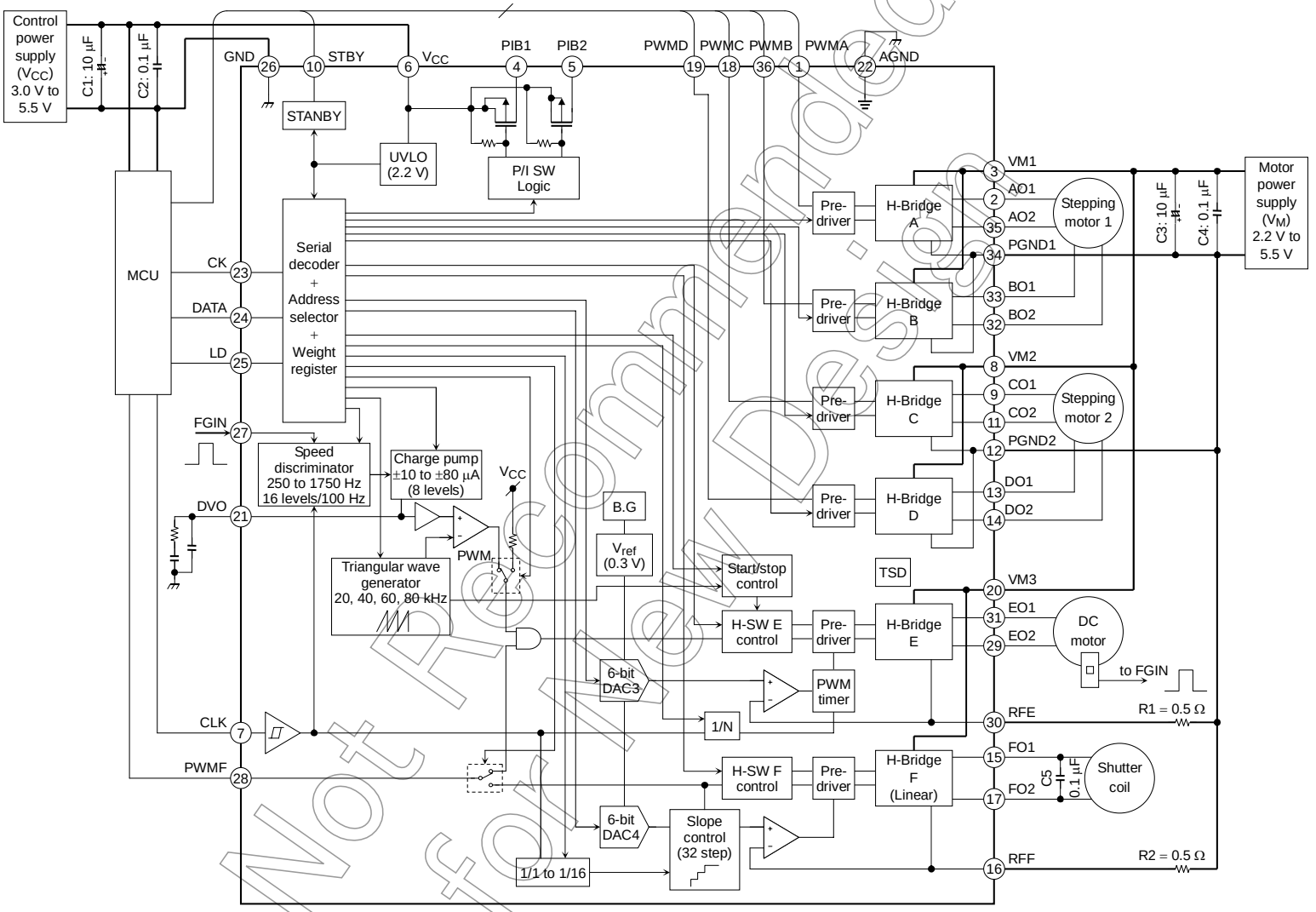
  Reverse brake → Short brake

- The reverse brake time is specified by serial data. (When Reverse brake time = 0, the TB6596FLG does not enter Reverse brake mode.)
- During the reverse brake operation, the operating mode cannot be changed.
- When the PMx input changes during the short brake operation at modx = 0, the operating mode changes according to the spxa and pxb inputs as shown in the above table. (Direct PWM control)

Electrical Characteristics (unless otherwise specified, V_{CC} = 3.3 V, V_M = 5 V, Ta = 25°C)

Characteristics			Symbol	Test Condition	Min	Typ.	Max	Unit
Supply current			I_{CC}	All 6 channels in Forward mode	—	1	2.5	mA
			$I_{CC\ (STB)}$	Standby mode (STBY = 0 V)	—	0.1	10	μA
			$I_{M\ (STB)}$		—	0	1	
Serial, STBY, PWM and CLK inputs	Input voltage		V_{INH}		V_{CC} − 0.8	—	V_{CC} + 0.2	V
			V_{INL}		−0.2	—	0.4	
	Input current		I_{INH}	V_{IH} = 3 V	10	15	20	μA
			I_{INL}	V_{IL} = 0 V	—	—	1	
FG input	Input voltage		V_{INHFG}		V_{CC} − 0.8	—	V_{CC} + 0.2	V
			V_{INLFG}		−0.2	—	0.4	
	Input current		I_{INSH}	V_{IH} = 3 V	—	—	1	μA
			I_{INSL}	V_{IL} = 0 V	−20	−15	−10	
Output saturation voltage (Channels A to F)			$V_{sat\ (U+L)}$	I_O = 0.2 A	—	0.3	0.4	V
				I_O = 0.6 A	—	0.9	1.2	
Output leakage current (Channels A to F)			$I_{L\ (U)}$	V_M = 6 V	—	—	1	μA
			$I_{L\ (L)}$		—	—	1	
Output diode forward voltage			$V_{F\ (U)}$	I_F = 0.6 A (Design value)	—	1	—	V
			$V_{F\ (L)}$		—	1	—	
Offset voltage for constant-current detection comparator			Comp ofs	RRF = 1 Ω, V_{ref} = 0.1 V (including DAC)	−10	—	10	mV
Charge pump	Charge current	Min	ICHG Min	VDO = 1 V (Design target only)	—	10	—	μA
		Max	ICHG Max		—	80	—	
		Step	ICHG step		—	10	—	
	Discharge current	Min	IDIS Min	VDO = 2 V (Design target only)	—	−10	—	
		Max	IDIS Max		—	−80	—	
		Step	IDIS step		—	−10	—	
6-bit DAC	Nonlinearity		LB	Channels E and F	−3	—	3	LSB
	Differential linearity error		DLB		−2	—	2	
P/I SW Transistors	Output saturation voltage		Vsat	ID = 20 mA	—	—	0.1	V
	Output leakage current		IDSS	VDS = 6 V	—	—	1	μA
Speed control	Minimum speed		FLL Min	(Design target only)	—	250	—	Hz
	Maximum speed		FLL Max		—	1750	—	
	Speed step		FLL step		—	100	—	
Triangular wave carrier	Minimum speed		Ftrig Min	(Design target only)	—	17	—	kHz
	Maximum speed		Ftrig Max		—	68	—	
	Speed step		Ftrig step		—	17	—	
Start/Reverse	Minimum control time		Tmin	(Design target only)	—	0	—	ms
	Maximum control time		Tmax		—	129	—	
	Control time step		T step		—	2.048	—	
Thermal shutdown threshold			TSD	(Design target only)	—	170	—	°C
Thermal shutdown hysteresis			ΔTSD		—	20	—	

Application Circuit



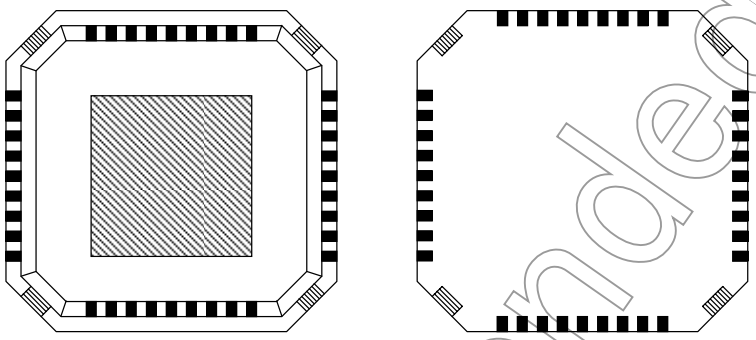
- Bypass capacitors (C1, C2, C3, C4) should be connected as close to the IC as possible.
- The Cdp capacitor of 0.01 to 0.1 µF should be connected to channel-F outputs as necessary to prevent the oscillation.

Notes: Excessive power might be introduced into the IC in case of a short-circuit between power supply and ground, an output short-circuit to power supply, an output short-circuit to ground or a short-circuit across the load. If any of these events occur, the device may be degraded or permanently damaged.

QON Package Considerations

Package Appearances

(Top view) (Bottom view)



Please follow the following guidelines for the QON package.

Guidelines:

(1) The solder plated pads at the four corners of the package (shaded areas in the bottom view) should not be soldered for the purpose of improving the mechanical strength of solder joints.

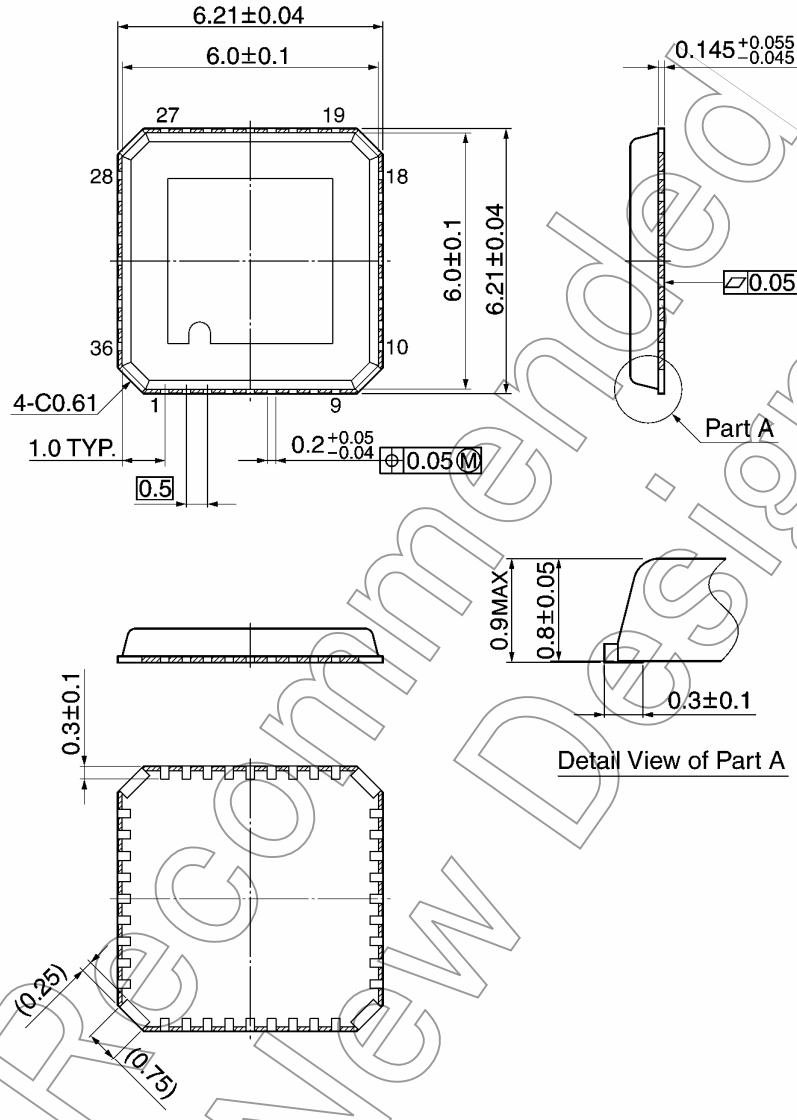
(2) When using the TB6596FLG, it should be ensured that the thermal pad and solder plated pads (shaded areas in the top and bottom views) are electrically insulated (Note).

Note: Care should be taken in the board design to prevent solder for through-hole joints from flowing to the solder plated pads on the bottom of the package (shaded areas in the bottom view).

- When mounting or soldering this package, care must be taken to avoid electrostatic discharge or electrical overstress to the IC. (This is to avoid electrical leakage and a buildup of electrostatic charge in the end product.)
- It should be ensured that no voltage is directly applied to the solder plated pads when designing the PC board.

Package Dimensions

QON36-P-0606-0.50 Unit: mm



Note 1: The solder-plated parts at the four corners of the package should not be used as external pins.

Note 2: The four corners of the package should not be soldered.

Note 3: Shaded areas: Resin surfaces

Weight: 0.08 g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Toshiba does not grant any license to any industrial property rights by providing these examples of application circuits.

5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on Handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to Remember on Handling of ICs

(1) Thermal Shutdown Circuit
Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(2) Heat Radiation Design
In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (Tj) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(3) Back-EMF
When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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