FUJITSU SEMICONDUCTOR
DATA SHEET

DS501-00045-1v0-E

*Memory ReRAM*

# 4M (512 K × 8) Bit SPI

# MB85AS4MT

## ■ DESCRIPTION

MB85AS4MT is a ReRAM (Resistive Random Access Memory) chip in a configuration of 524,288 words × 8 bits, using the resistance-variable memory process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.
MB85AS4MT adopts the Serial Peripheral Interface (SPI).
MB85AS4MT is able to retain data without using a back-up battery, as is needed for SRAM.
The memory cells used in the MB85AS4MT can be used for 1.2 × $10^6$ rewrite operations.

## ■ FEATURES

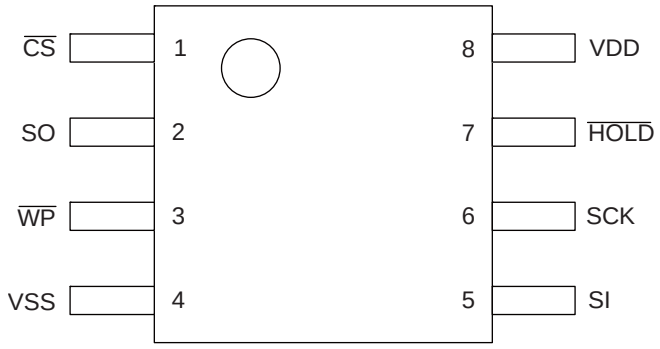
- Bit configuration : 4 Mbits (524,288 words × 8 bits)
- Serial Peripheral Interface : SPI (Serial Peripheral Interface)
  Correspondent to SPI mode 0 (0, 0) and mode 3 (1, 1)
- Write buffer size : 256 bytes
- Operating frequency : 5 MHz (Max)
- Data endurance : 1.2 × $10^6$ times / byte
- Data retention : 10 years (+85 °C)
- Operating power supply voltage : 1.65 V to 3.6 V
- Operating power supply current : Rewrite current 1.3 mA (Typ)
  Read-out current 0.2 mA (Typ@5 MHz)
  Standby current 10 μA (Typ)
  Sleep current 2 μA (Typ)
- Operation ambient temperature range : -40 °C to +85 °C
- Package : 8-pin plastic SOP (FPT-8P-M11)
  RoHS compliant


2016.12

FUJITSU

## ■ PIN ASSIGNMENT

(TOP VIEW)

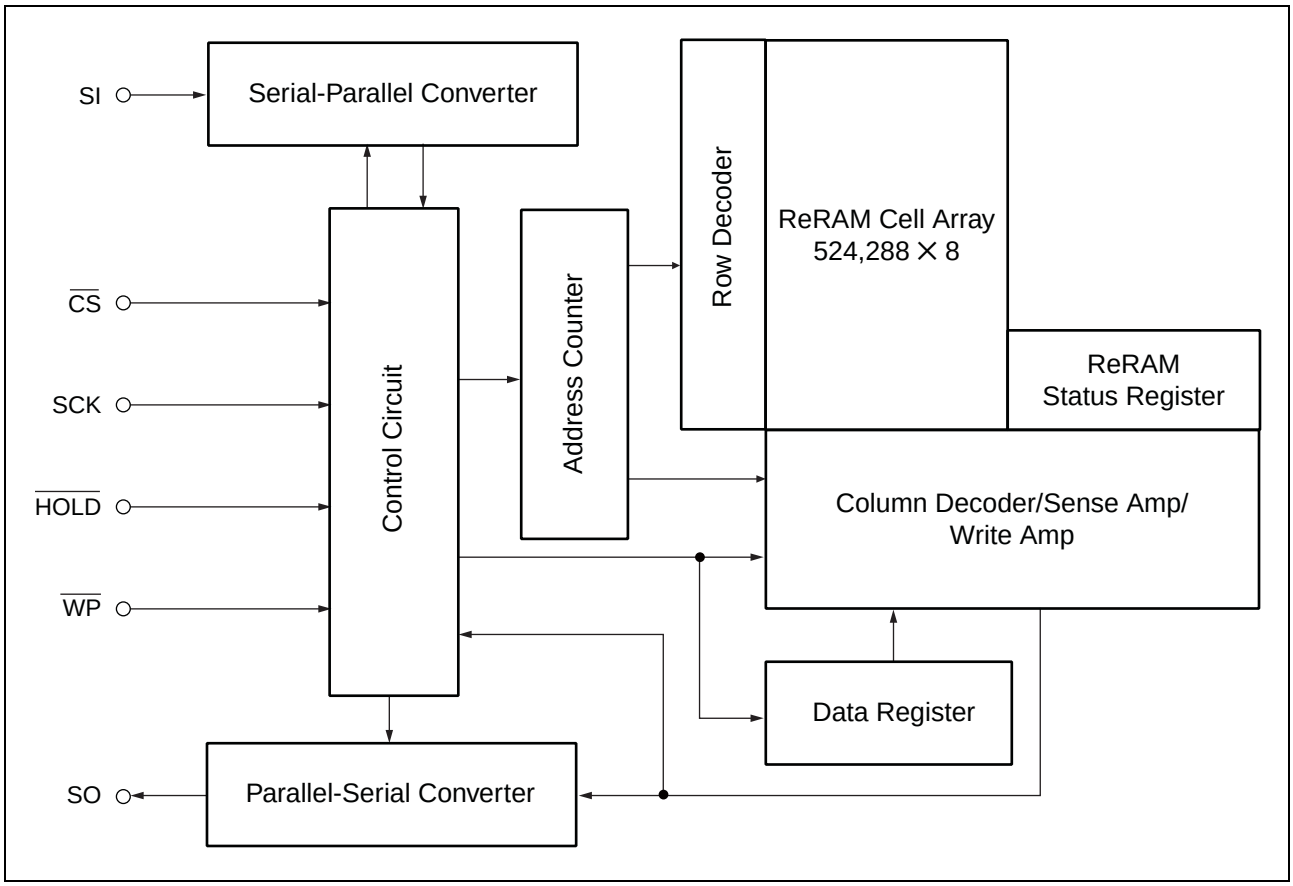



(FPT-8P-M11)

## ■ PIN FUNCTIONAL DESCRIPTIONS

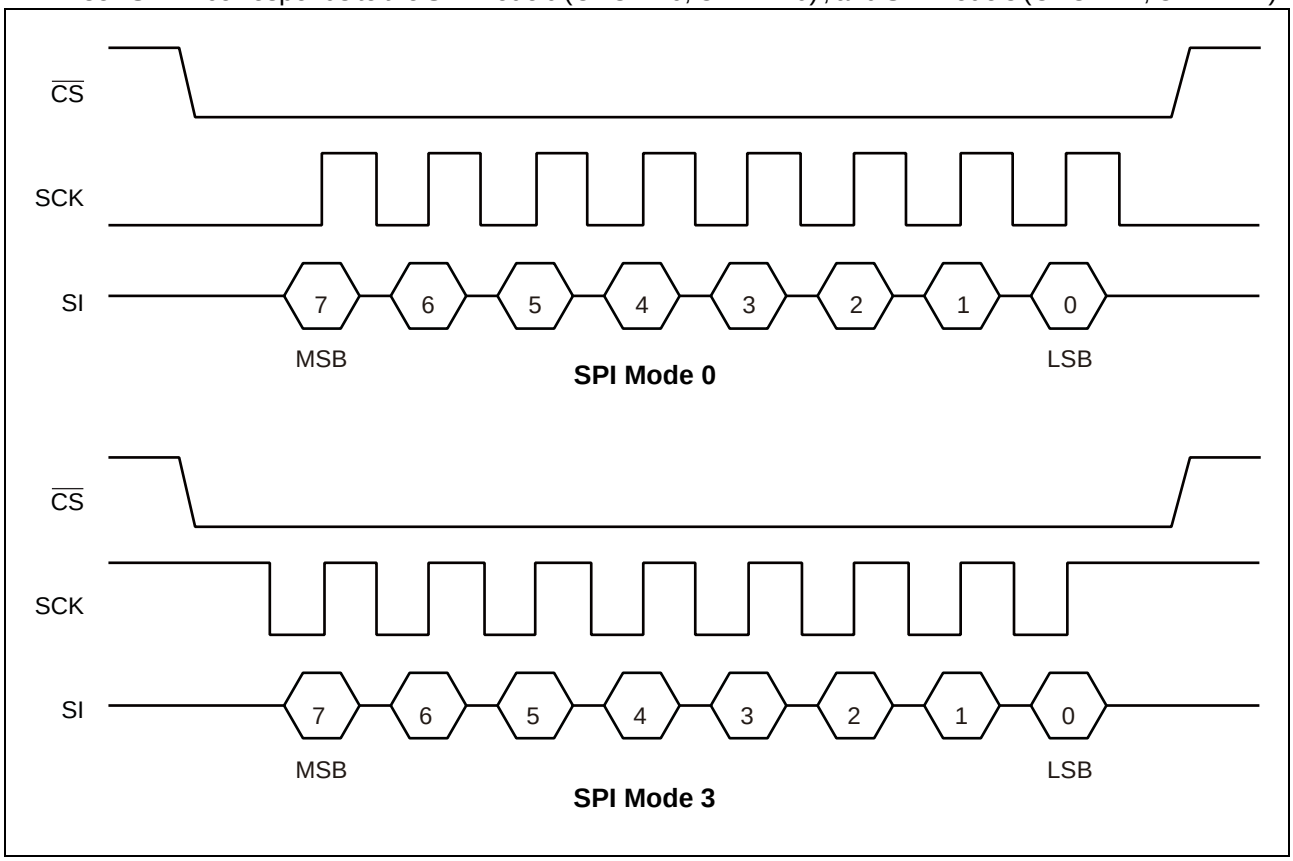
| Pin No. | Pin Name | Functional description |
|---|---|---|
| 1 | $\overline{CS}$ | Chip Select pin<br>This is an input pin to make chips select. When $\overline{CS}$ is “H” level, device is in deselect (standby) status and SO becomes High-Z. Inputs from other pins are ignored for this time. When $\overline{CS}$ is “L” level, device is in select (active) status. $\overline{CS}$ has to be “L” level before inputting op-code. |
| 3 | $\overline{WP}$ | Write Protect pin<br>This is a pin to control writing to a status register. The writing of status register (see “■ STATUS REGISTER”) is protected in related with $\overline{WP}$ and WPEN. See “■ WRITING PROTECT” for detail. |
| 7 | $\overline{HOLD}$ | Hold pin<br>This pin is used to interrupt serial input/output without making chips deselect. When $\overline{HOLD}$ is “L” level, hold operation is activated, SO becomes High-Z, SCK and SI become do not care. While the hold operation, $\overline{CS}$ has to be retained “L” level. |
| 6 | SCK | Serial Clock pin<br>This is a clock input pin to input/output serial data. SI is loaded synchronously to a rising edge, SO is output synchronously to a falling edge. |
| 5 | SI | Serial Data Input pin<br>This is an input pin of serial data. This inputs op-code, address, and writing data. |
| 2 | SO | Serial Data Output pin<br>This is an output pin of serial data. Reading data of ReRAM memory cell array and status register data are output. This is High-Z during standby. |
| 8 | VDD | Supply Voltage pin |
| 4 | VSS | Ground pin |

## ■ BLOCK DIAGRAM



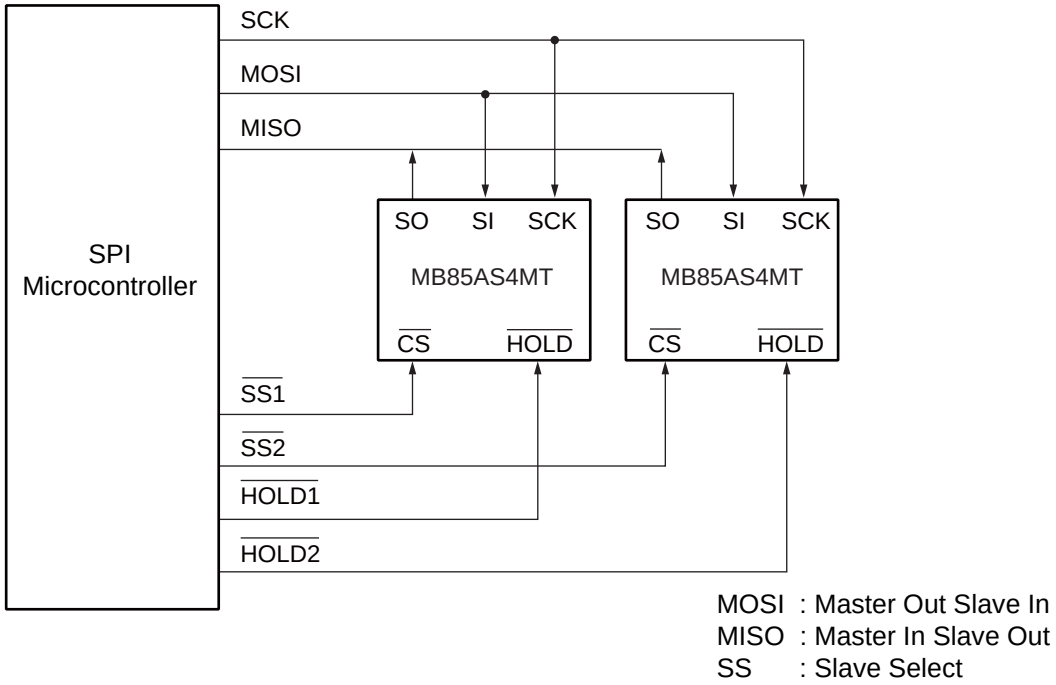
## ■ SPI MODE

MB85AS4MT corresponds to the SPI mode 0 (CPOL = 0, CPHA = 0) , and SPI mode 3 (CPOL = 1, CPHA = 1) .

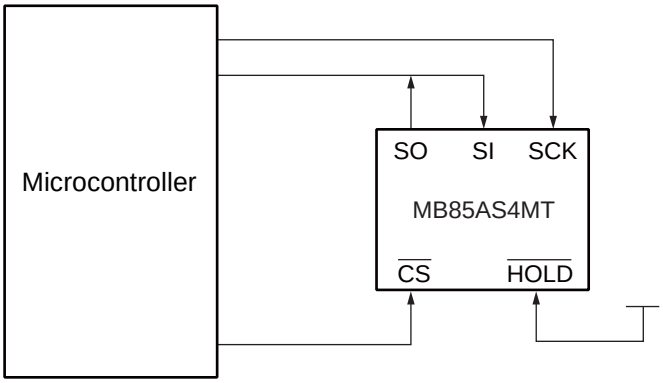


## ■ SERIAL PERIPHERAL INTERFACE (SPI)

MB85AS4MT works as a slave of SPI. More than 2 devices can be connected by using microcontroller equipped with SPI port. By using a microcontroller not equipped with SPI port, SI and SO can be bus connected to use.




**System Configuration with SPI Port**




**System Configuration without SPI Port**

## ■ STATUS REGISTER

| Bit No. | Bit Name | Function |
|---|---|---|
| 7 | WPEN | Status Register Write Protect<br>This is a bit composed of nonvolatile memories (ReRAM). WPEN protects writing to a status register (refer to "■ WRITING PROTECT") relating with $\overline{WP}$ input. Writing with the WRSR command and reading with the RDSR command are possible. |
| 6 to 4 | — | Not Used Bits<br>These are bits composed of volatile memories, writing with the WRSR command is possible. These bits are not used but they are read with the RDSR command. |
| 3 | BP1 | Block Protect<br>This is a bit composed of nonvolatile memory. This defines size of write protect block for the WRITE command (refer to "■ BLOCK PROTECT"). Writing with the WRSR command and reading with the RDSR command are possible. |
| 2 | BP0 | |
| 1 | WEL | Write Enable Latch<br>This indicates ReRAM Array and status register are writable. The WREN command is for setting, and the WRDI command is for resetting. With the RDSR command, reading is possible but writing is not possible with the WRSR command. WEL is reset after the following operations.<br>After power ON.<br>The rising edge of $\overline{CS}$ after WRDI command recognition.<br>The end of writing process after WRSR command recognition.<br>The end of writing process after WRITE command recognition. |
| 0 | WIP | Write In Progress<br>This indicates ReRAM Array and status register are in writing process. During this writing process, any commands except RDSR will not be executed (refer to "2. WIP polling"). With the RDSR command, reading is possible but writing is not possible with the WRSR command. |

## ■ OP-CODE

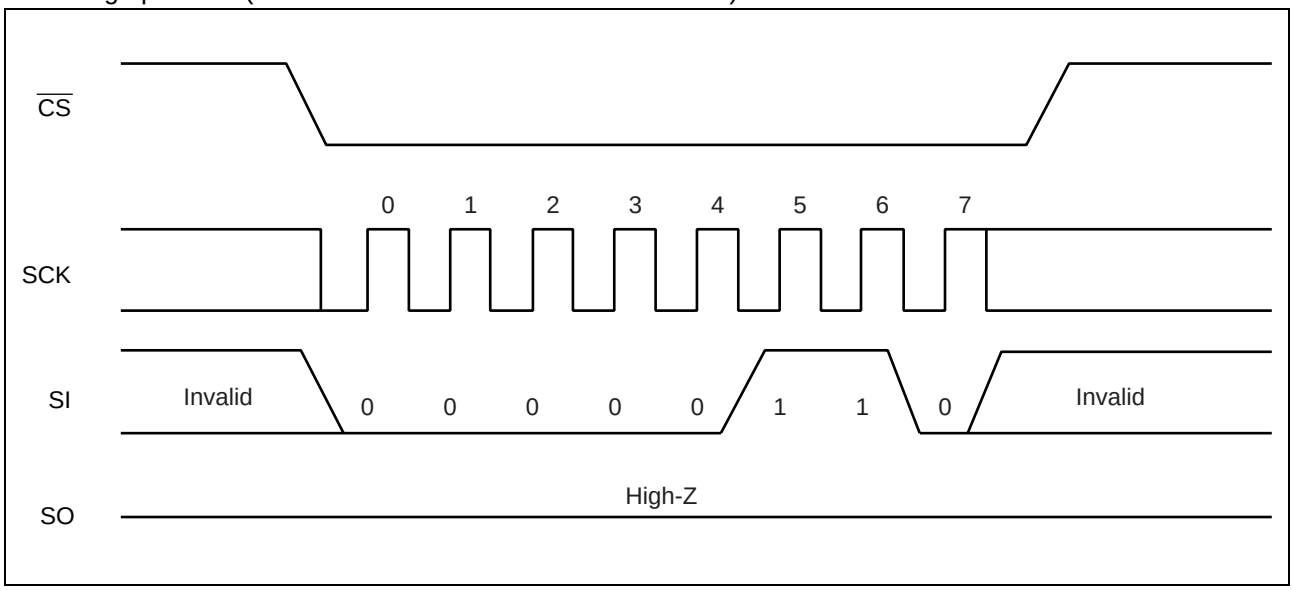
MB85AS4MT accepts 8 kinds of command specified in op-code. Op-code is a code composed of 8 bits shown in the table below. Do not input invalid codes other than those codes. If $\overline{CS}$ is risen while inputting op-code, the command are not performed.

| Name | Description | Op-code |
|---|---|---|
| WREN | Set Write Enable Latch | $0000\ 0110_B$ |
| WRDI | Reset Write Enable Latch | $0000\ 0100_B$ |
| RDSR | Read Status Register | $0000\ 0101_B$ |
| WRSR | Write Status Register | $0000\ 0001_B$ |
| READ | Read Memory Code | $0000\ 0011_B$ |
| WRITE | Write Memory Code | $0000\ 0010_B$ |
| RDID | Read Device ID | $1001\ 1111_B$ |
| SLEEP | Sleep Mode | $1011\ 1001_B$ |

## ■ COMMAND

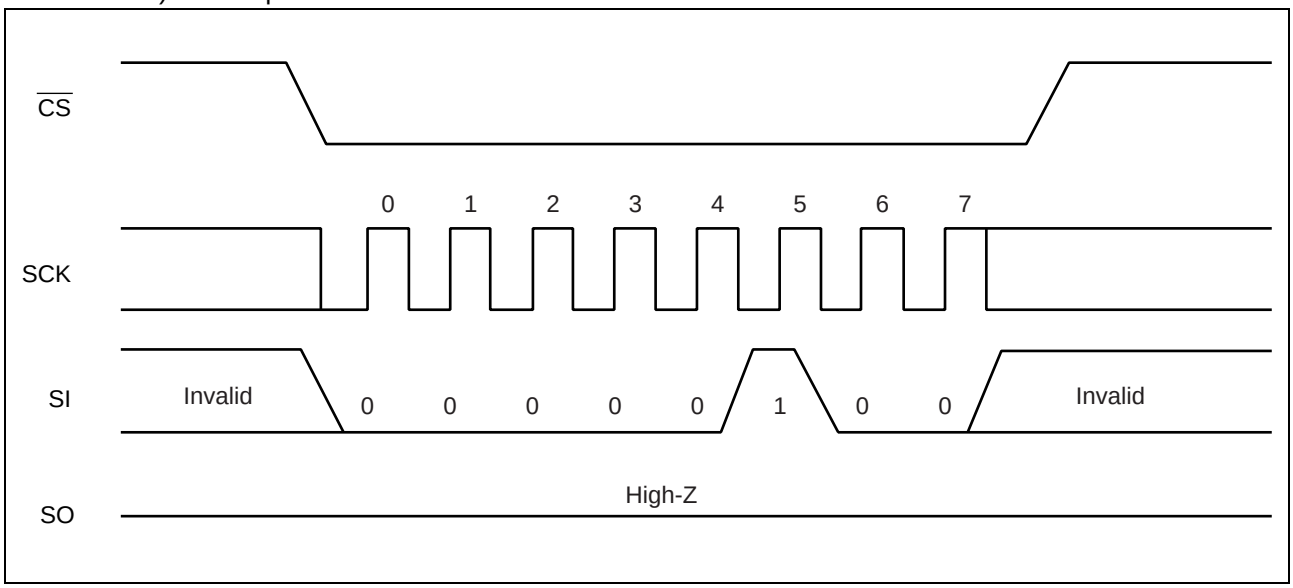
**• WREN**

The WREN command sets WEL (Write Enable Latch) . WEL has to be set with the WREN command before writing operation (WRSR command and WRITE command) .



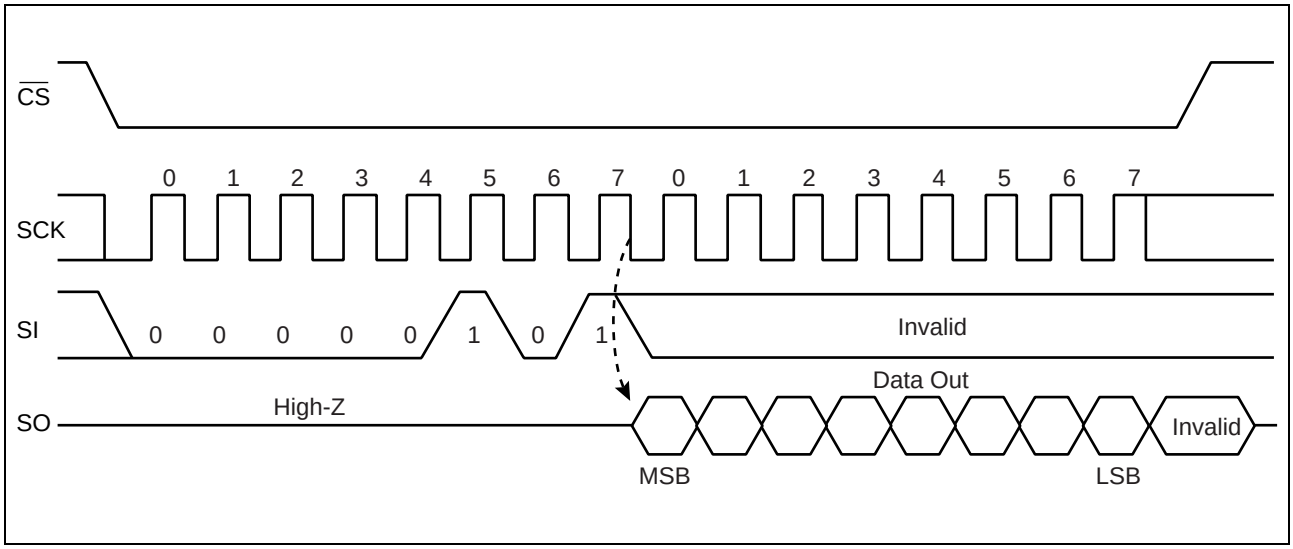

**• WRDI**

The WRDI command resets WEL (Write Enable Latch) . Writing operation (WRSR command and WRITE command) are not performed when WEL is reset.



• **RDSR**

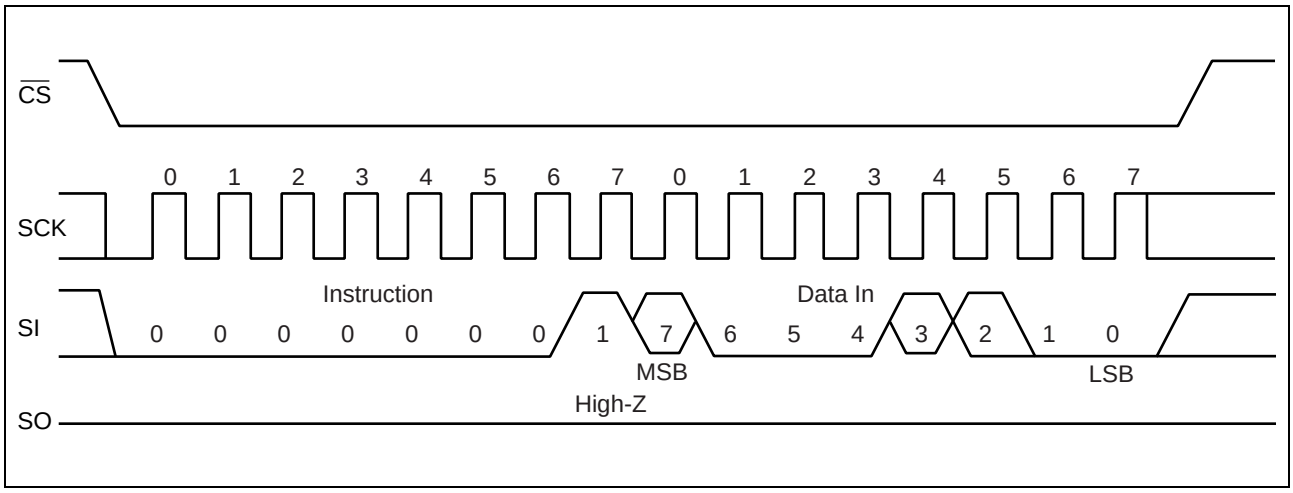
The RDSR command reads status register data. After op-code of RDSR is input to SI, 8-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. In the RDSR command, repeated reading of status register is enabled by sending SCK continuously before rising of $\overline{CS}$.




• **WRSR**

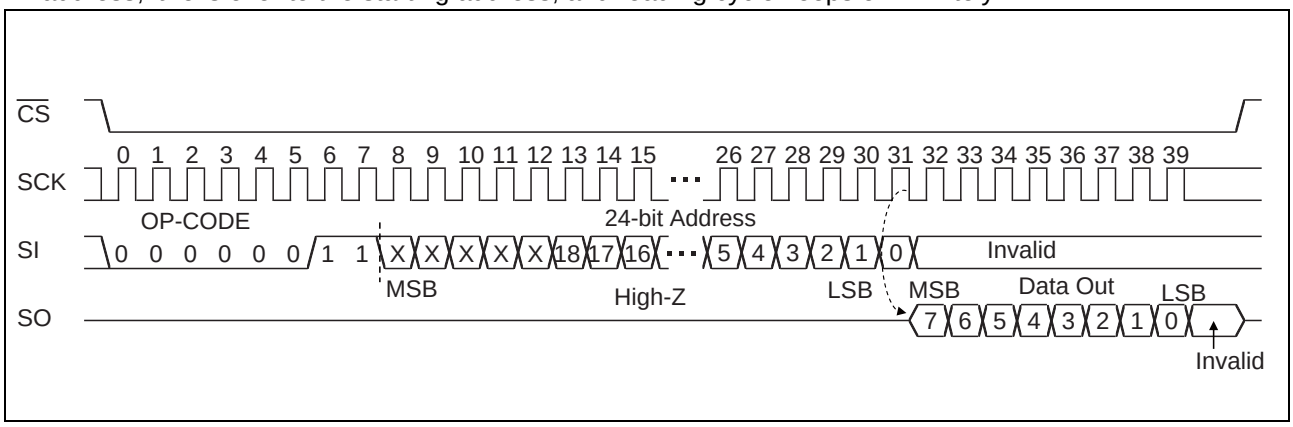
The WRSR command writes data to the nonvolatile memory bit of status register. After performing WRSR op-code to a SI pin, 8 bits writing data is input. WEL (Write Enable Latch) is not able to be written with WRSR command. A SI value correspondent to bit 1 is ignored. Bit 0 of the status register cannot be written. The SI value corresponding to bit 0 is ignored. $\overline{WP}$ signal level shall be fixed before performing WRSR command, and do not change the $\overline{WP}$ signal level until the end of command sequence.

After rising edge of $\overline{CS}$, MB85AS4MT starts writing operation to nonvolatile register and set WIP bit in status register to “1”. After this writing operation has finished, reset this WIP bit from “1” to “0”. Although the RDSR command is executable for WIP polling during this writing process, any other commands will not be performed.



- **READ**

The READ command reads ReRAM memory cell array data. Arbitrary 24 bits address and op-code of READ are input to SI. The 5-bit upper address bit is invalid. Then, 8-cycle clock is input to SCK. SO is output synchronously to the falling edge of SCK. While reading, the SI value is invalid. When $\overline{CS}$ is risen, the READ command is completed, but keeps on reading with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles before $\overline{CS}$ rising. When it reaches the most significant address, it rolls over to the starting address, and reading cycle keeps on infinitely.

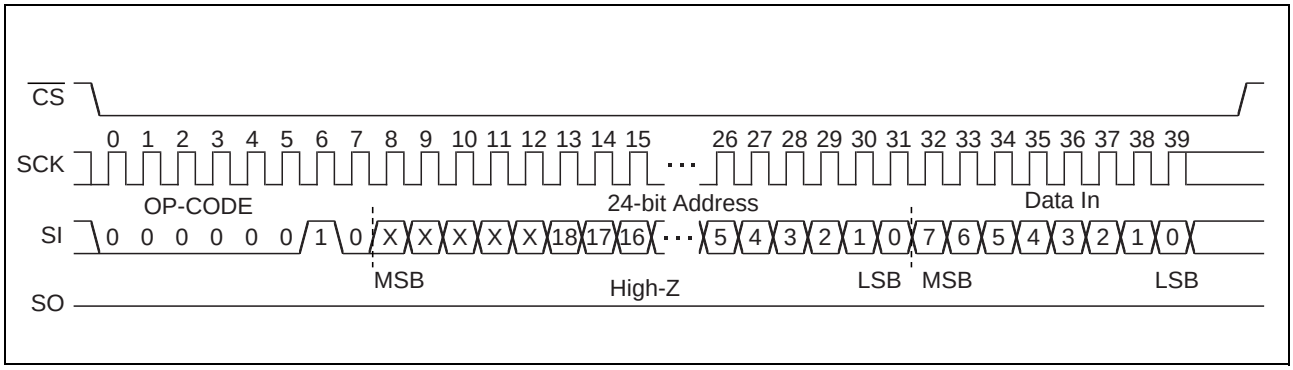



- **WRITE**

The WRITE command writes data to ReRAM memory cell array. WRITE op-code, arbitrary 24 bits of address and 8 bits of writing data are input to SI. The 5-bit upper address bit is invalid.

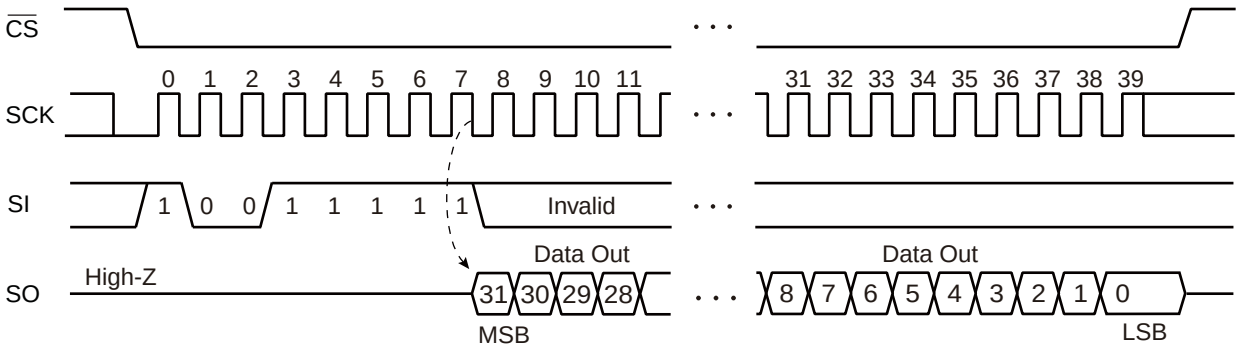
During the $\overline{CS}$ is low, input writing data are temporary saved in the data register. The maximum writing data size is 256 bytes during this $\overline{CS}$ = low period. If the input writing data are more than 8 bits, it is possible to continue writing with automatic address increment. When it reaches the most significant address, it rolls over to the starting address, and writing cycle can be continued up to 256 bytes (which is the size of data register). Data exceed 256 bytes can not be written.

After rising edge of $\overline{CS}$, MB85AS4MT starts writing operation to nonvolatile memory and set WIP bit in status register to “1”. After this writing operation has finished, reset this WIP bit from “1” to “0”. Although the RDSR command is executable for WIP polling during this writing process, any other commands will not be performed.



- **RDID**

The RDID command reads fixed Device ID. After performing RDID op-code to SI, 32-cycle clock is input to SCK. The SI value is invalid for this time. SO is output synchronously to a falling edge of SCK. The output is in order of Manufacturer ID (8bit)/Continuation code (8bit)/Product ID (1st Byte)/Product ID (2nd Byte). In the RDID command, SO holds the output state of the last bit in 32-bit Device ID until $\overline{CS}$ is risen. RDID command is applicable to “Up to 25 MHz operation”.




| | bit | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** | **Hex** | |
| Manufacturer ID | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | $04_H$ | Fujitsu |
| Continuation code | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | $7F_H$ | |

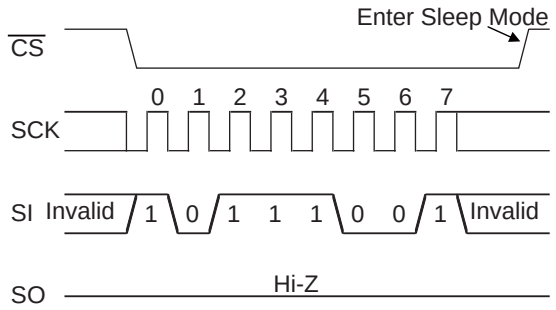
| | Proprietary use | | | Density | | | | | Hex | |
|---|---|---|---|---|---|---|---|---|---|---|
| Product ID (1st Byte) | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | $C9_H$ | Density: $01001_B$ = 4 Mbit |

| | Proprietary use | | | | | | | | Hex | |
|---|---|---|---|---|---|---|---|---|---|---|
| Product ID (2nd Byte) | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | $03_H$ | |

- **SLEEP**

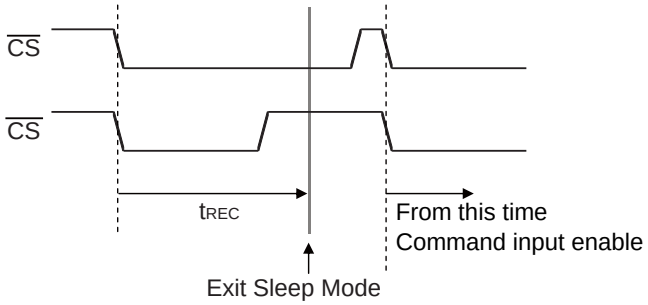
The SLEEP command shifts the LSI to a low power mode called “SLEEP mode”. The transition to the SLEEP mode is carried out at the rising edge of $\overline{CS}$ after operation code in the SLEEP command. However, when at least one SCK clock is inputted before the rising edge of $\overline{CS}$ after operation code in the SLEEP command, this SLEEP command is canceled.

After the SLEEP mode transition, SCK and SI inputs are ignored and SO changes to a Hi-Z state.




Sleep Mode Entry

Returning to an normal operation from the SLEEP mode is carried out after $t_{REC}$ (Max 400 µs) time from the falling edge of $\overline{CS}$ (see the figure below). It is possible to return $\overline{CS}$ to H level before $t_{REC}$ time. However, it is prohibited to bring down $\overline{CS}$ to L level again during $t_{REC}$ period.




Sleep Mode Exit

## ■ WRITING OPERATION OF NONVOLATILE MEMORY

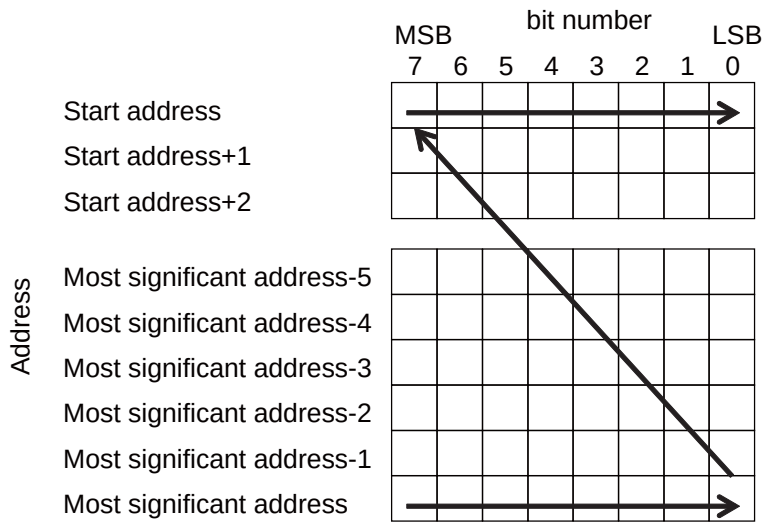
Each input data is not written to the nonvolatile memory by unit of byte right after its data input. Multiple bytes up to maximum 256 bytes are temporarily saved to the data register. After the command input is finished and rising edge of $\overline{CS}$, start writing operation from this data register to the nonvolatile memory.

### 1. Address counter control

In case of memory access by WRITE and READ commands, after the end of op-code and address input, it is possible to keep on accessing (= reading or writing) with automatic address increment which is enabled by continuously sending clocks to SCK in unit of 8 cycles while $\overline{CS}$ is low level. However, for the WRITE command, continuous writing is restricted by the limit of buffer size in the data register.

When it reaches the most significant address, it rolls over to the starting address, and this automatic address increment will be continued by the address counter control.

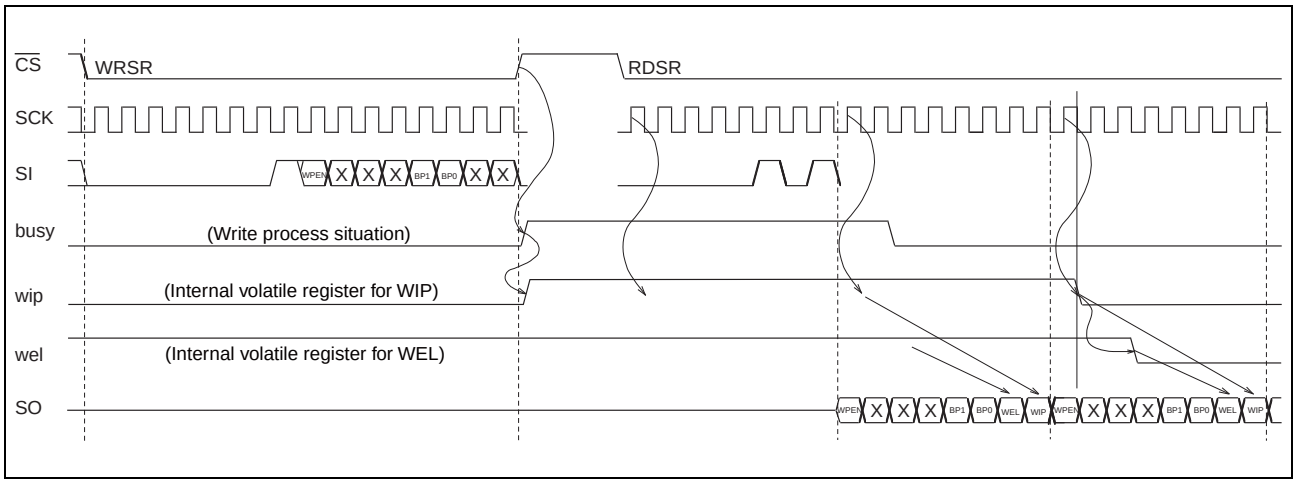
Over write protection to the nonvolatile memory is enabled by BP0 and BP1 bits in status register. When the memory address exceed it from write protected block to unprotected block by address counter control, write to the unprotected block only. Similarly, when memory address exceed it from unprotected block to protected block, does not write to the protected block.




### 2. WIP polling

After the last writing data was input, writing to the nonvolatile memory needs tWC waiting time from the rising edge of $\overline{CS}$. This tWC time becomes larger than a minimum clock cycle. Production variation and operating condition are considered, and this maximum tWC value is defined. In the usual operation, this tWC time is shorter than the maximum value. Therefore, MB85AS4MT supports WIP polling to improve memory access by optimizing the waiting time.

After starting the data writing to nonvolatile memory, MB85AS4MT sets “1” to a volatile register related to the WIP bit in status register. After finished the writing operation, reset this WIP bit from “1” to “0”. Although the usual commands are not executable during this writing process, only the RDSR command is acceptable. RDSR command outputs the value of status register to SO. It is possible to confirm if the internal writing operation to nonvolatile memory is finished or not, by checking the corresponding bit to WIP in output data from SO.




RDSR command also outputs the WPEN, BP1 and BP0 of status register to SO. In the polling after WRSR command, MB85AS4MT outputs the WPEN, BP1 and BP0 data which is set before the writing to nonvolatile memory is completed. On the other hand for WEL and WIP, MB85AS4MT outputs (WEL,WIP)=2'b11 when the writing to nonvolatile memory is not completed. When it is competed, outputs (WEL,WIP)=2'b00.

If continuously sending clocks to SCK during $\overline{CS}$ = low, it is also possible to keep on outputting WPEN to WIP bits in status register in unit of 8 cycles since 17th clock. In case the WIP polling is applied, WIP and WEL bits in status register output to SO by RDSR command are updated regularly.

Figure shows the example of RDSR command input with continuously sending clocks over 17 during $\overline{CS}$ = low, before the writing process of WRSR command is finished.

## ■ BLOCK PROTECT

Writing protect block for WRITE command is configured by the value of BP0 and BP1 in the status register.

| BP1 | BP0 | Protected Block |
|---|---|---|
| 0 | 0 | None |
| 0 | 1 | $60000_H$ to $7FFFF_H$ (upper 1/4) |
| 1 | 0 | $40000_H$ to $7FFFF_H$ (upper 1/2) |
| 1 | 1 | $00000_H$ to $7FFFF_H$ (all) |

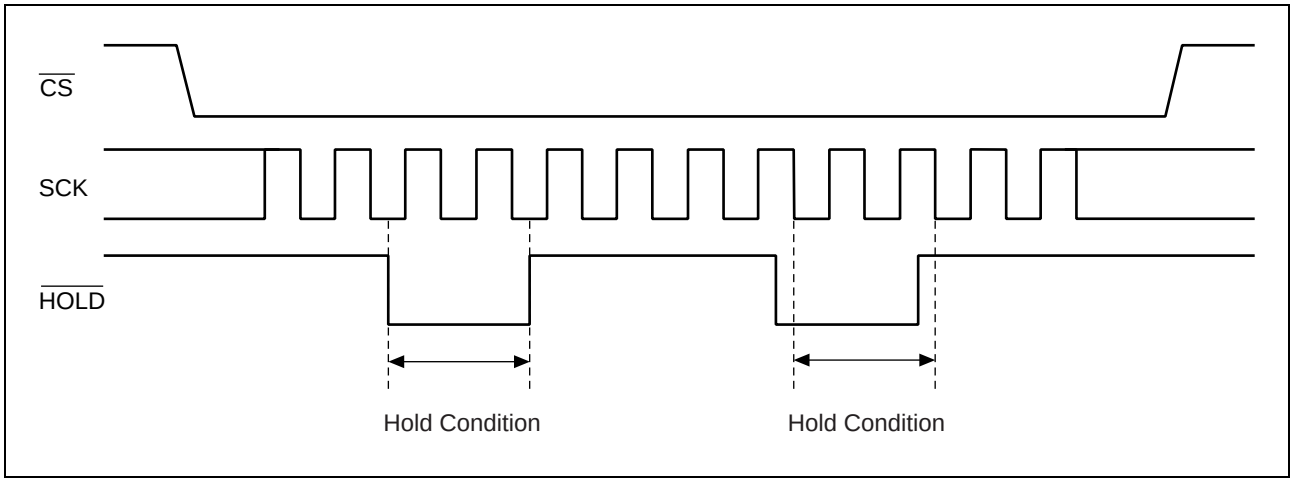
## ■ WRITING PROTECT

Writing operation of the WRITE command and the WRSR command are protected with the value of WEL, WPEN, $\overline{WP}$ as shown in the table.

| WEL | WPEN | $\overline{WP}$ | Protected Blocks | Unprotected Blocks | Status Register |
|---|---|---|---|---|---|
| 0 | X | X | Protected | Protected | Protected |
| 1 | 0 | X | Protected | Unprotected | Unprotected |
| 1 | 1 | 0 | Protected | Unprotected | Protected |
| 1 | 1 | 1 | Protected | Unprotected | Unprotected |

## ■ HOLD OPERATION

Hold status is retained without aborting a command if $\overline{HOLD}$ is “L” level while $\overline{CS}$ is “L” level. The timing for starting and ending hold status depends on the SCK to be “H” level or “L” level when a $\overline{HOLD}$ pin input is transited to the hold condition as shown in the diagram below. In case the $\overline{HOLD}$ pin transited to “L” level when SCK is “L” level, return the $\overline{HOLD}$ pin to “H” level at SCK being “L” level. In the same manner, in case the $\overline{HOLD}$ pin transited to “L” level when SCK is “H” level, return the $\overline{HOLD}$ pin to “H” level at SCK being “H” level. Arbitrary command operation is interrupted in hold status, SCK and SI inputs become do not care. And, SO becomes High-Z while reading command (RDSR, READ). $\overline{CS}$ shall be set to “L” level during hold status.



## ■ ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Rating | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Power supply voltage* | $V_{DD}$ | – 0.5 | + 4.0 | V |
| Input voltage* | $V_{IN}$ | – 0.5 | $V_{DD}$ + 0.5 | V |
| Output voltage* | $V_{OUT}$ | – 0.5 | $V_{DD}$ + 0.5 | V |
| Operation ambient temperature | $T_A$ | – 40 | + 85 | °C |
| Storage temperature | Tstg | – 55 | + 125 | °C |

*:These parameters are based on the condition that $V_{SS}$ is 0 V.

WARNING: Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings.
Do not exceed any of these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Power supply voltage*1 | $V_{DD}$ | 1.65 | 3.3 | 3.6 | V |
| Operation ambient temperature*2 | $T_A$ | – 40 | — | + 85 | °C |

*1: These parameters are based on the condition that $V_{SS}$ is 0 V.

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated under these conditions.

Any use of semiconductor devices will be under their recommended operating condition. Operation under any conditions other than these conditions may adversely affect reliability of device and could result in device failure.

No warranty is made with respect to any use, operating conditions or combinations not represented on this data sheet. If you are considering application under any conditions other than listed herein, please contact sales representatives beforehand.

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(within recommended operating conditions)

| Parameter | Symbol | Condition | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| Input leakage current | $\|I_{LI}\|$ | $\overline{CS}$, $\overline{WP}$, SCK, SI, $\overline{HOLD}$ = 0 V to $V_{DD}$ | — | — | 1 | µA |
| Output leakage current | $\|I_{LO}\|$ | SO = 0 V to $V_{DD}$ | — | — | 1 | µA |
| Operating power supply current | $I_{DD}$ | SCK = 5 MHz (read) | — | 0.2 | 0.5 | mA |
| | | SCK = 5 MHz (write) | — | 1.3 | 3.0 | mA |
| Standby current | $I_{SB}$ | SCK = SI = $\overline{CS}$ = $V_{DD}$ | — | 10 | 45 | µA |
| Sleep current | $I_{ZZ}$ | $\overline{CS}$ = $V_{DD}$<br>All inputs $V_{SS}$ or $V_{DD}$ | — | 2 | 5 | µA |
| Input high voltage | $V_{IH}$ | $V_{DD}$ = 1.65 V to 3.6 V | $V_{DD} \times 0.8$ | — | $V_{DD} + 0.5$ | V |
| Input low voltage | $V_{IL}$ | $V_{DD}$ = 1.65 V to 3.6 V | – 0.5 | — | $V_{DD} \times 0.2$ | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = – 1.5 mA @$V_{DD} \geq$ 1.8 V<br>$I_{OH}$ = – 1.2 mA @$V_{DD}$ < 1.8 V | $V_{DD}$ – 0.5 | — | — | V |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 1.5 mA @$V_{DD} \geq$ 1.8 V<br>$I_{OL}$ = 1.2 mA @$V_{DD}$ < 1.8 V | — | — | 0.4 | V |

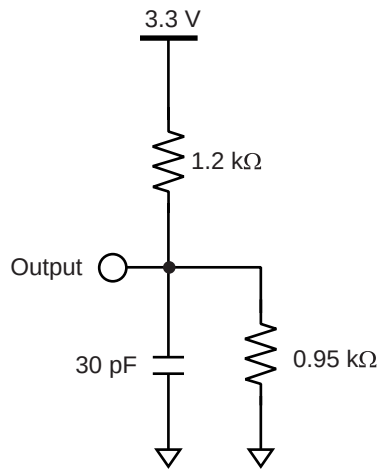
## 2. AC Characteristics

| Parameter | Symbol | Value | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| SCK clock frequency | $f_{CK}$ | 0 | — | 5 | MHz | |
| Clock high time | $t_{CH}$ | 60 | — | — | ns | |
| Clock low time | $t_{CL}$ | 60 | — | — | ns | |
| Chip select set up time | $t_{CSUH}$ | 60 | — | — | ns | $\overline{CS}$ rising to SCK rising |
| | $t_{CSUL}$ | 60 | — | — | | $\overline{CS}$ falling to SCK rising |
| Chip select hold time | $t_{CSHH}$ | 60 | — | — | ns | SCK rising to $\overline{CS}$ falling |
| | $t_{CSHL}$ | 60 | — | — | | SCK rising to $\overline{CS}$ rising |
| | $t_{CSH}$ | 50 | — | — | | SCK falling to $\overline{CS}$ rising |
| Output disable time | $t_{OD}$ | — | — | 60 | ns | |
| Output data valid time | $t_{ODV}$ | — | — | 60 | ns | |
| Output hold time | $t_{OH}$ | 0 | — | — | ns | |
| Deselect time | $t_D$ | 160 | — | — | ns | |
| Data rising time | $t_R$ | — | — | 50 | ns | |
| Data falling time | $t_F$ | — | — | 50 | ns | |
| Data set up time | $t_{SU}$ | 20 | — | — | ns | |
| Data hold time | $t_H$ | 20 | — | — | ns | |
| $\overline{HOLD}$ set uptime | $t_{HS}$ | 20 | — | — | ns | |
| $\overline{HOLD}$ hold time | $t_{HH}$ | 20 | — | — | ns | |
| $\overline{HOLD}$ output floating time | $t_{HZ}$ | — | — | 60 | ns | |
| $\overline{HOLD}$ output active time | $t_{LZ}$ | — | — | 60 | ns | |
| Write cycle time | $t_{WC}$ | — | 8500 | 17000 | µs | @50% data turn over (0xAAAA => 0xCCCC) |
| | | — | 16000 | 25000 | µs | @100% data turn over |
| SLEEP recovery time | $t_{REC}$ | — | — | 400 | µs | |

### AC Test Condition

Power supply voltage : 1.65 V to 3.6 V
Operation ambient temperature : – 40 °C to + 85 °C
Input voltage magnitude : $V_{DD} \times 0.8 \leq V_{IH} \leq V_{DD}$
$0 \leq V_{IL} \leq V_{DD} \times 0.2$
Input rising time : 5 ns
Input falling time : 5 ns
Input judge level : $V_{DD}/2$
Output judge level : $V_{DD}/2$

**AC Load Equivalent Circuit**

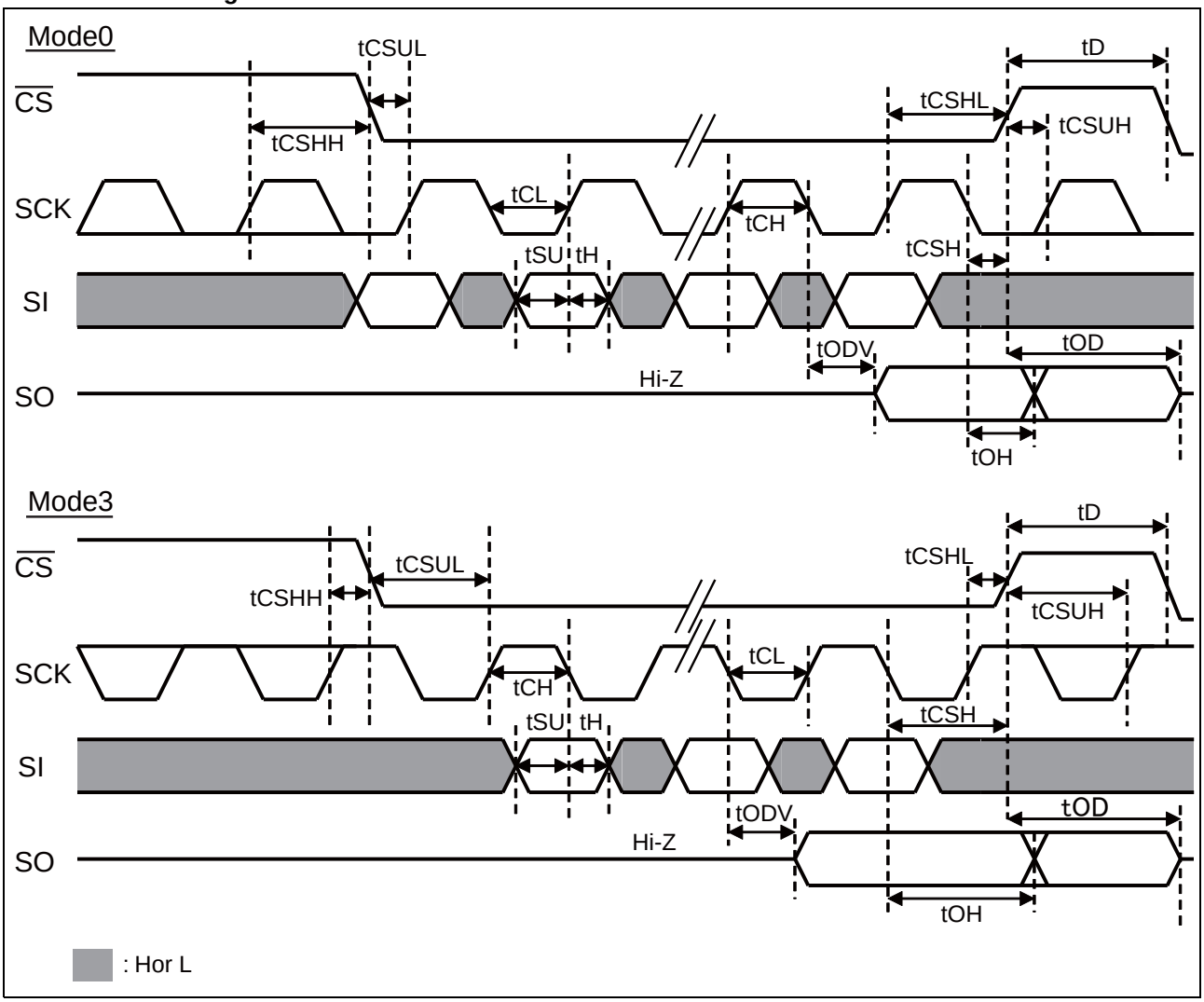



## 3. Pin Capacitance

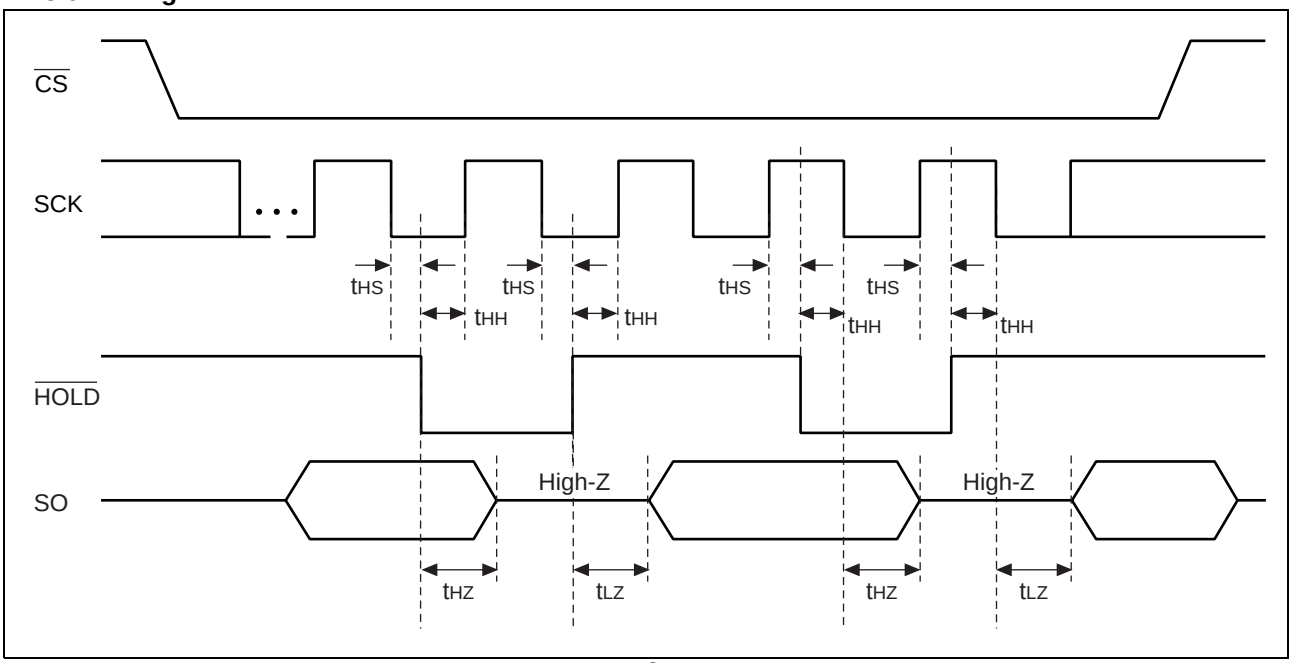
| Parameter | Symbol | Condition | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| Output capacitance | $C_O$ | $V_{DD} = V_{IN} = V_{OUT} = 0$ V, f = 1 MHz, $T_A$ = +25 °C | — | 8 | pF |
| Input capacitance | $C_I$ | | — | 6 | pF |

## ■ TIMING DIAGRAM

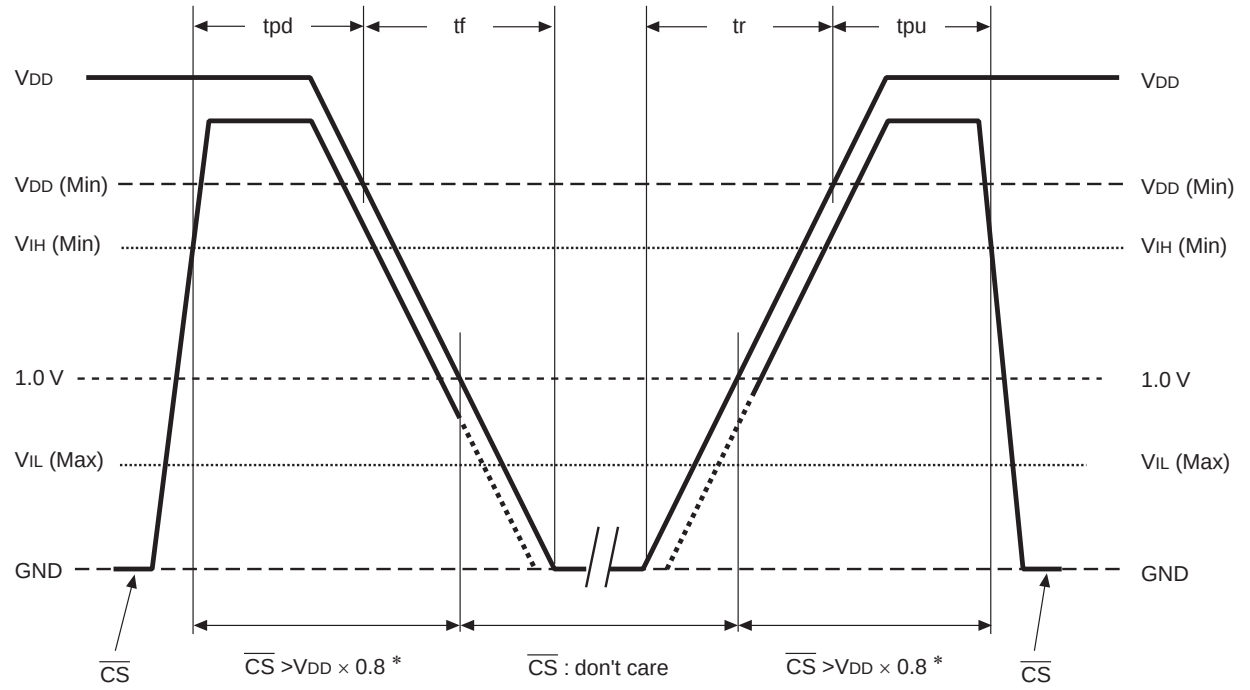
• **Serial Data Timing**




• **Hold Timing**



## ■ POWER ON/OFF SEQUENCE




* : $\overline{CS}$ (Max) < $V_{DD}$ + 0.5 V

| Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $\overline{CS}$ level hold time at power OFF | tpd | 25 | — | ms |
| $\overline{CS}$ level hold time at power ON | tpu | 400 | — | µs |
| Power supply rising time | tr | 0.05 | — | ms/V |
| Power supply falling time | tf | 0.1 | — | ms/V |

If the device does not operate within the specified conditions of read cycle, write cycle or power on/off sequence, memory data can not be guaranteed.

## ■ ReRAM CHARACTERISTICS

| Parameter | Value | | Unit | Remarks |
|---|---|---|---|---|
| | Min | Max | | |
| Write Endurance | $1.2 \times 10^6$ | — | Times/byte | Operation Ambient Temperature $T_A$ = + 85 °C |
| Data Retention | 10 | — | Years | Operation Ambient Temperature $T_A$ = + 85 °C<br>Retention time of the first reading/writing data right after shipment. |
| Data register size | — | 256 | byte | |

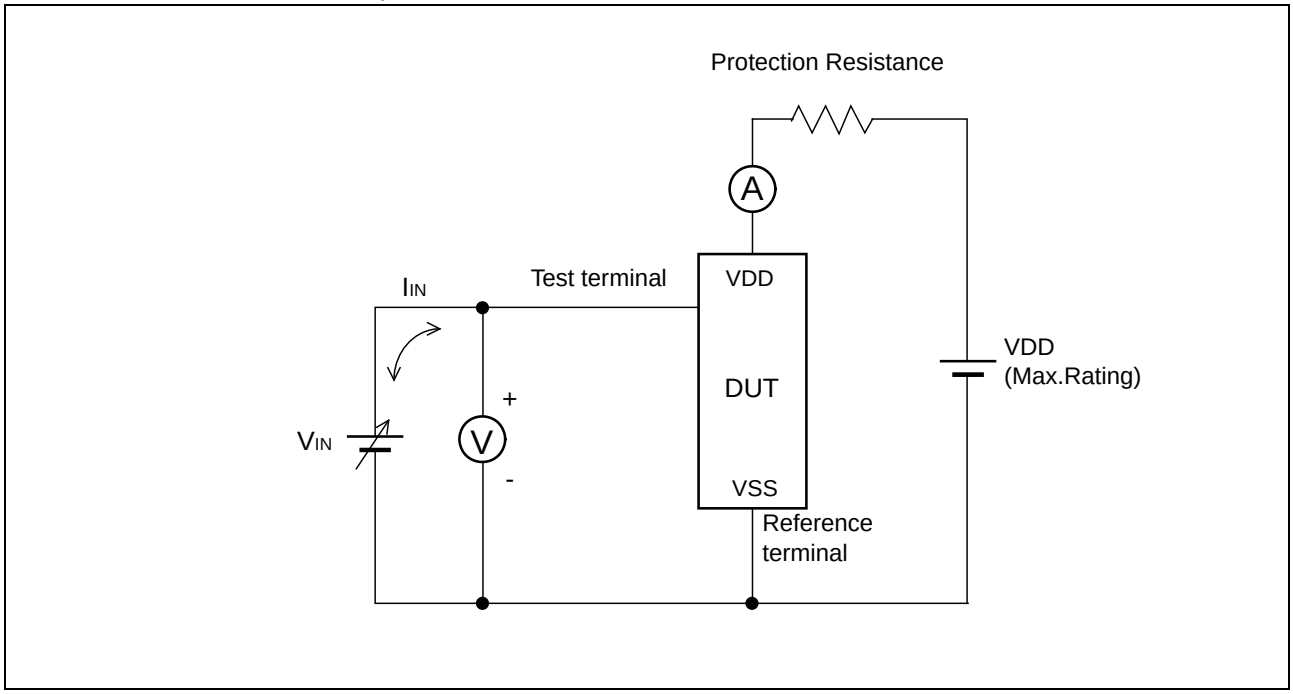
## ■ NOTE ON USE

We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

## ■ ESD AND LATCH-UP

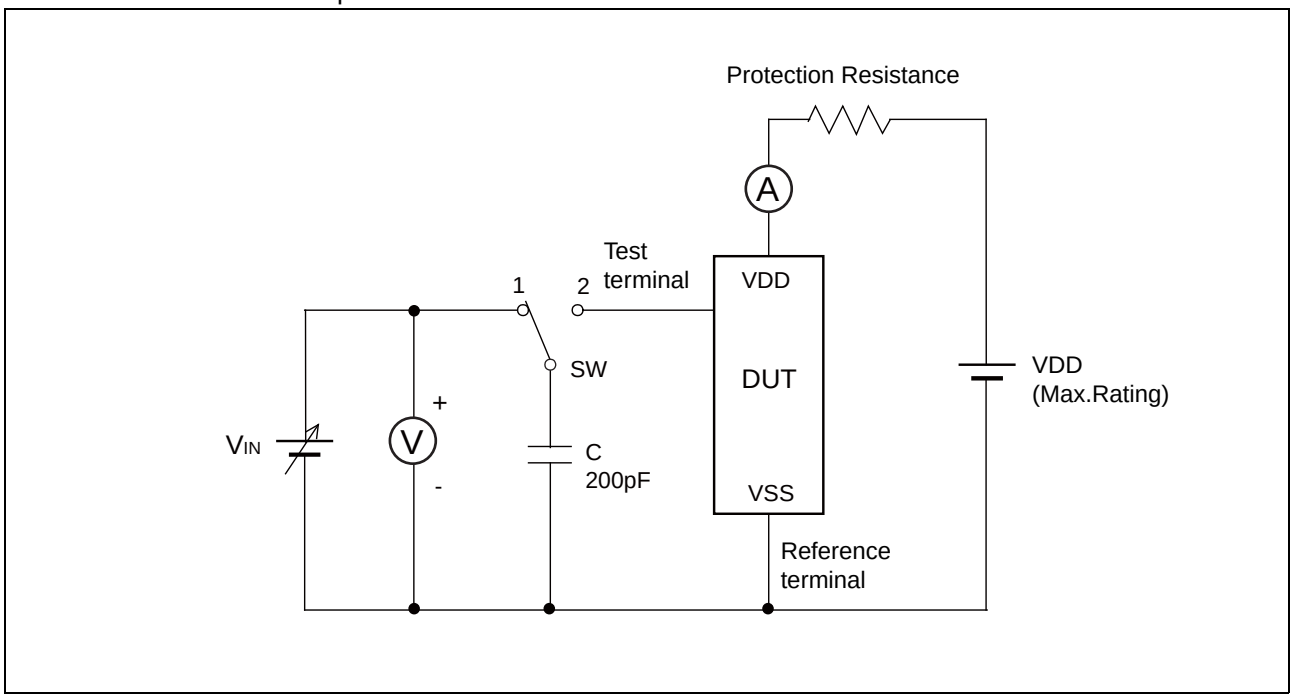
| Test | DUT | Value |
|---|---|---|
| ESD HBM (Human Body Model)<br>JESD22-A114 compliant | MB85AS4MTPF-G-BCERE1 | ≥ \|2000 V\| |
| ESD MM (Machine Model)<br>JESD22-A115 compliant | | ≥ \|200 V\| |
| ESD CDM (Charged Device Model)<br>JESD22-C101 compliant | | ≥ \|1000 V\| |
| Latch-Up (I-test)<br>JESD78 compliant | | — |
| Latch-Up ($V_{supply}$ overvoltage test)<br>JESD78 compliant | | — |
| Latch-Up (Current Method)<br>Proprietary method | | — |
| Latch-Up (C-V Method)<br>Proprietary method | | ≥ \|200 V\| |

- Current method of Latch-Up Resistance Test




Note : The voltage $V_{IN}$ is increased gradually and the current $I_{IN}$ of 300 mA at maximum shall flow.
Confirm the latch up does not occur under $I_{IN}$ = ±300 mA.
In case the specific requirement is specified for I/O and $I_{IN}$ cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

- C-V method of Latch-Up Resistance Test




Note : Charge voltage alternately switching 1 and 2 approximately 2 sec interval. This switching process is considered as one cycle. Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

## ■ MB85AS4MTPF (8-pin plastic SOP) REFLOW CONDITIONS AND FLOOR LIFE

[ JEDEC MSL ] : Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020D)

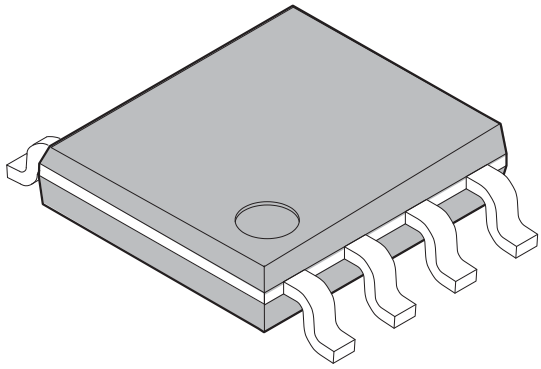
## ■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

## ■ ORDERING INFORMATION

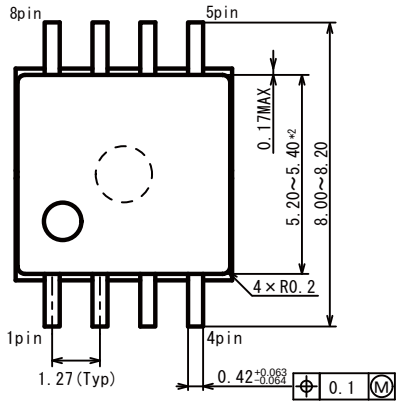
| Part number | Package | Shipping form | Minimum shipping quantity |
|---|---|---|---|
| MB85AS4MTPF-G-BCERE1 | 8-pin plastic SOP (FPT-8P-M11) | Embossed Carrier tape | 500 |

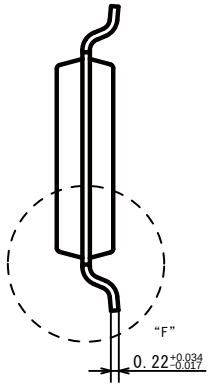
## ■ PACKAGE DIMENSION

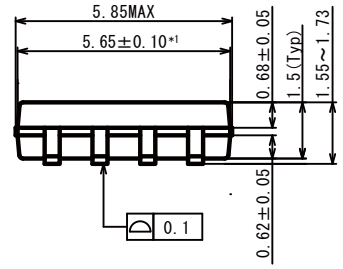
| 8-pin plastic SOP | | |
|---|---|---|
|  | Lead pitch | 1.27 mm |
| | Package width × package length | 5.3 mm × 5.65 mm |
| | Lead shape | Gullwing |
| | Sealing method | Plastic mold |
| | Mounting heigth | 1.73 mm MAX |
| | Weight | TBD g |
| (FPT-8P-M11) | | |

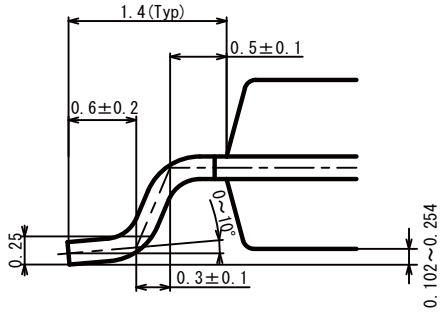
8-pin plastic SOP
（FPT-8P-M11）

Note 1) *1: These dimensions do not include resin protrution.
Note 2) *2: These dimensions do not include resin protrution.



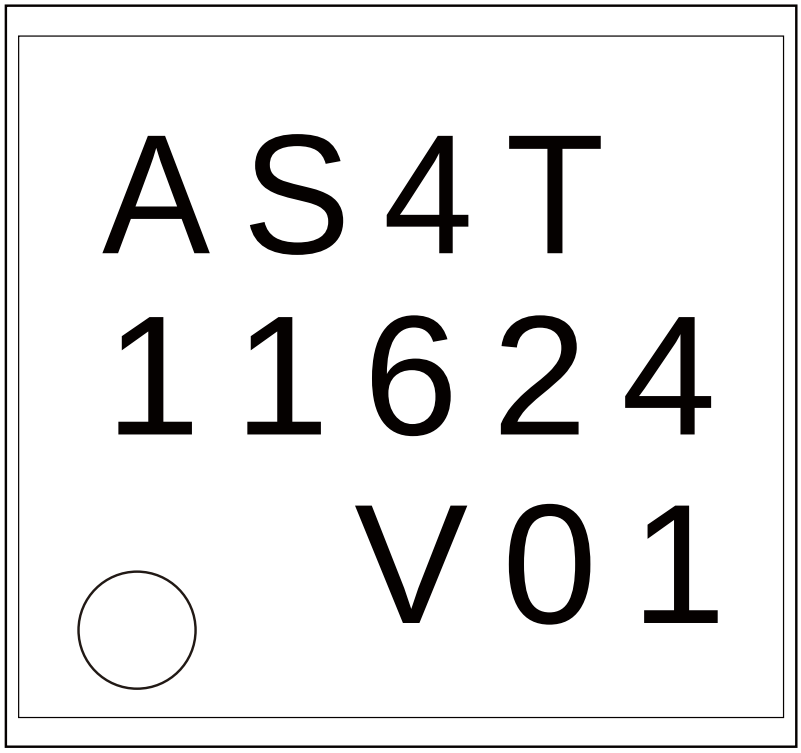

Details of "F" part



Dimenssions in mm

## ■ MARKING

[MB85AS4MTPF-G-BCERE1]




[FPT-08P-M11]

## ■ MAJOR CHANGES IN THIS EDITION

A change on a page is indicated by a vertical line drawn on the left side of that page.

| Page | Section | Change Results |
|---|---|---|
| 6 | ■ STATUS REGISTER | Bit 6 to 4: revised to volatile memory.<br>WEL: revised the reset condition. |
| 14 | ■ HOLD OPERATION | Revised $\overline{CS}$ operation during hold status. |

# MEMO

**FUJITSU SEMICONDUCTOR LIMITED**
Shin-Yokohama Chuo Building, 2-100-45 Shin-Yokohama,
Kohoku-ku, Yokohama, Kanagawa 222-0033, Japan
*http://jp.fujitsu.com/fsl/en/*



Edited: System Memory Business Division