



Package Style: Module, 10-Pin, 3mm x 3mm x 1.0mm

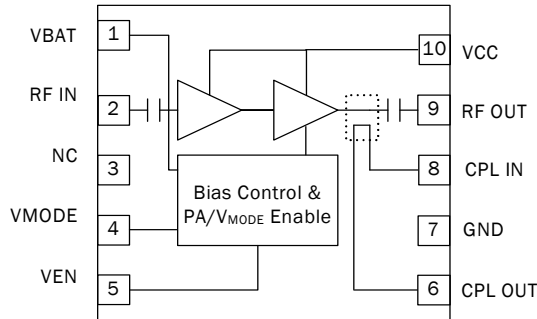


### Features

- HSDPA/HSUPA/HSPA+/LTE
- High Efficiency WCDMA Operation: 41% at  $P_{OUT}=+28dBm$
- Low Voltage Positive Bias Supply (3.0V to 4.2V)
- Internal Voltage Regulator - No External ( $V_{REF}$ ) Required
- Two Mode Power/Gain States with Digital Control Interface
- Integrated Power Coupler
- Integrated Blocking and Decoupling Capacitors

### Applications

- WCDMA/HSPA+/LTE Wireless Data Cards
- WCDMA/HSPA+/LTE Handsets



Functional Block Diagram

### Product Description

The RF7413 is a high-power, high-efficiency, linear power amplifier designed for use as the final RF amplifier in 3V, 50Ω WCDMA mobile cellular equipment and spread-spectrum systems. This PA is developed for UMTS Band 3 which operates in the 1710MHz to 1785MHz frequency band. The RF7413 has a digital control pin which enables a low power mode to reduce amplifier gain at lower power levels. The part also has an integrated directional coupler which eliminates the need for an external discrete coupler at the output. The RF7413 (Band 3) meets the spectral linearity requirements of High Speed Downlink Packet Access (HSDPA), High Speed Uplink Packet Access (HSUPA), and Long Term Evolution (LTE) data transmission. The RF7413 is assembled in a 10-pin, 3mm x 3mm module.

### Ordering Information

RF7413	3V WCDMA Band 3 Linear PA Module
RF7413PCBA-410	Fully Assembled Evaluation Board

### Optimum Technology Matching® Applied

- |   |                                      |                                     |                                    |
|---|--------------------------------------|-------------------------------------|------------------------------------|
| <input type="checkbox"/> GaAs HBT             | <input type="checkbox"/> SiGe BiCMOS | <input type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT  |
| <input type="checkbox"/> GaAs MESFET          | <input type="checkbox"/> Si BiCMOS   | <input type="checkbox"/> Si CMOS    | <input type="checkbox"/> BIFET HBT |
| <input checked="" type="checkbox"/> InGaP HBT | <input type="checkbox"/> SiGe HBT    | <input type="checkbox"/> Si BJT     | <input type="checkbox"/> LDMOS     |

## Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage in Standby Mode	6.0	V
Supply Voltage in Idle Mode	6.0	V
Supply Voltage in Operating Mode, 50Ω Load	6.0	V
Supply Voltage, V <sub>BAT</sub>	6.0	V
Control Voltage, V <sub>MODE</sub>	3.7	V
Control Voltage, V <sub>EN</sub>	3.7	V
RF - Input Power	+10	dBm
RF - Output Power	+30	dBm
Operating Ambient Temperature	-30 to +110	°C
Storage Temperature	-55 to +150	°C



**Caution!** ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

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RFMD Green: RoHS compliant per EU Directive 2002/95/EC, halogen free per IEC 61249-2-21, < 1000 ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Recommended Operating Conditions</b>					
Operating Frequency Range	1710		1785	MHz	
V <sub>BAT</sub>	+3.0	+3.2	+4.2	V	
V <sub>CC</sub>	+3.0 <sup>1</sup>	+3.2	+4.2	V	
V <sub>CC</sub> (used with DC-DC)	0.5		+4.2	V	PA used with DC-DC converter to reduce current drain at back-off and lower power levels
V <sub>EN</sub>	0		0.5	V	PA disabled.
	1.35	1.80	3.10	V	PA enabled.
V <sub>MODE</sub>	0		0.5	V	Logic "low".
	1.35	1.80	3.10	V	Logic "high".
P <sub>OUT</sub>					
Maximum Linear Output (HPM)	28.0 <sup>1,2</sup>			dBm	High Power Mode (HPM)
Maximum Linear Output (LPM)	16.0 <sup>1,2</sup>			dBm	Low Power Mode (LPM)
Ambient Temperature	-20	+25	+85	°C	

Notes:

<sup>1</sup>For operation at V<sub>CC</sub>=+3.0V, derate P<sub>OUT</sub> by 0.5dB.

<sup>2</sup>P<sub>OUT</sub> is specified for 3GPP (Voice) modulation. For HSDPA and HSPA+ operation, derate P<sub>OUT</sub> by 2dB:

HSDPA Configuration: β<sub>c</sub>=12, β<sub>d</sub>=15, β<sub>hs</sub>=24

HSPA+ Configuration: 3GPP Rel7 Subtest 1

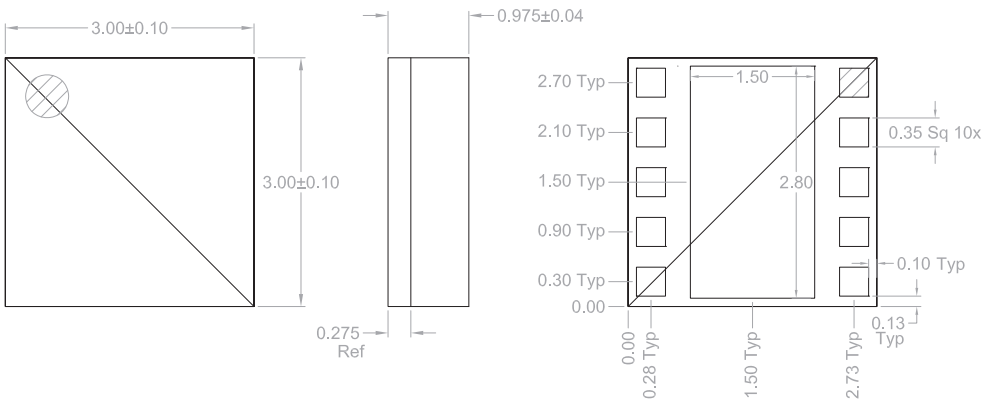
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
<b>Electrical Specifications</b>					T=+25°C, V <sub>CC</sub> =V <sub>BAT</sub> =+3.2V, V <sub>EN</sub> =+1.8V, 50Ω system, WCDMA Rel 99 Modulation unless otherwise specified.
Gain		31		dB	HPM, P <sub>OUT</sub> =28.0dBm
		17.5		dB	LPM, P <sub>OUT</sub> ≤ 16.0dBm
ACLR - 5MHz Offset		-41	-36	dBc	HPM, P <sub>OUT</sub> =28.0dBm
		-46	-38	dBc	LPM, P <sub>OUT</sub> ≤ 16.0dBm
ACLR - 10MHz Offset		-55	-48	dBc	HPM, P <sub>OUT</sub> =28.0dBm
		-68	-48	dBc	LPM, P <sub>OUT</sub> ≤ 16.0dBm
PAE	38	41		%	HPM, P <sub>OUT</sub> =28.0dBm
		10		%	LPM, P <sub>OUT</sub> ≤ 16.0dBm
Current Drain		452		mA	HPM, P <sub>OUT</sub> =28.0dBm
		125		mA	LPM, P <sub>OUT</sub> ≤ 16.0dBm
Quiescent Current		50		mA	HPM, DC only
Enable Current		0.03		mA	Source or sink current. V <sub>EN</sub> =1.8V.
Mode Current (I <sub>MODE</sub> )		0.01		mA	Source or sink current. V <sub>MODE</sub> =1.8V.
Leakage Current		2.0	10.0	μA	DC only. V <sub>CC</sub> =V <sub>BAT</sub> =4.2V, V <sub>EN</sub> =V <sub>MODE</sub> =0.5V.
Noise Power in Receive Band		-133		dBm/Hz	All power modes, measured at duplex offset frequency (F <sub>TX</sub> + 95MHz). Rx: 1805MHz to 1880MHz, P <sub>OUT</sub> ≤ 28.0dBm.
Input Impedance		1.6:1		VSWR	No ext. matching, P <sub>OUT</sub> ≤ 28dBm, all modes.
Harmonic, 2FO		-21	-7	dBm	P <sub>OUT</sub> ≤ 28.0dBm, all power modes.
Harmonic, 3FO		-24	-14	dBm	P <sub>OUT</sub> ≤ 28.0dBm, all power modes.
Spurious Output Level			-60	dBc	All spurious, P <sub>OUT</sub> ≤ 28dBm, all conditions, load VSWR ≤ 6:1, all phase angles.
Insertion Phase Shift	-30	5.6	+30	°	Phase shift at 16dBm when switching from HPM to LPM.
DC Enable Time			10	μS	DC only. Time from V <sub>EN</sub> =high to stable idle current (90% of steady state value).
RF Rise/Fall Time			6	μS	P <sub>OUT</sub> ≤ 28.0dBm, all modes. 90% of target, DC settled prior to RF.
Ruggedness			10:1	VSWR	HPM, P <sub>OUT</sub> =28.0dBm, all phases.
Coupling Factor		20		dB	P <sub>OUT</sub> ≤ 28.0dBm, all modes.
Daisy Chain Insertion Loss		0.25		dB	CPL_IN to CPL_OUT port, V <sub>EN</sub> =0.5V
Coupling Directivity		20		dB	

Pin	Function	Description
1	VBAT	Supply voltage for bias circuitry.
2	RF IN	RF input internally matched to 50Ω and DC blocked. The RF input matching circuit has a shunt inductor to ground which would short any DC voltage placed on this pin.
3	NC	No connection.
4	VMODE	Digital control input for power mode selection (see Operating Modes truth table).
5	VEN	Digital control input for PA enable and disable (see Operating Modes truth table).
6	CPL_OUT	Coupler output.
7	GND	This pin must be grounded.
8	CPL_IN	Coupler input used for cascading couplers in series. Terminate this pin with a 50Ω resistor if not connected to another coupler.
9	RF OUT	RF output internally matched to 50Ω and DC blocked.
10	VCC	Supply voltage for the first and second stage amplifiers, which can be connected to battery supply or output of DC-DC converter.
Pkg Base	GND	Ground connection. The package backside should be soldered to a topline ground pad connecting to the PCB ground plane with multiple ground vias. The pad should have a low thermal resistance and low electrical impedance to the ground plane.

### Operating Mode Truth Table

V <sub>EN</sub>	V <sub>MODE</sub>	V <sub>BAT</sub>	V <sub>CC</sub>	Conditions/Comments
Low	Low	3.0V to 4.2V	3.0V to 4.2V	Power down mode
Low	X	3.0V to 4.2V	3.0V to 4.2V	Standby Mode
High	Low	3.0V to 4.2V	3.0V to 4.2V	High power mode
High	High	3.0V to 4.2V	3.0V to 4.2V	Low power mode

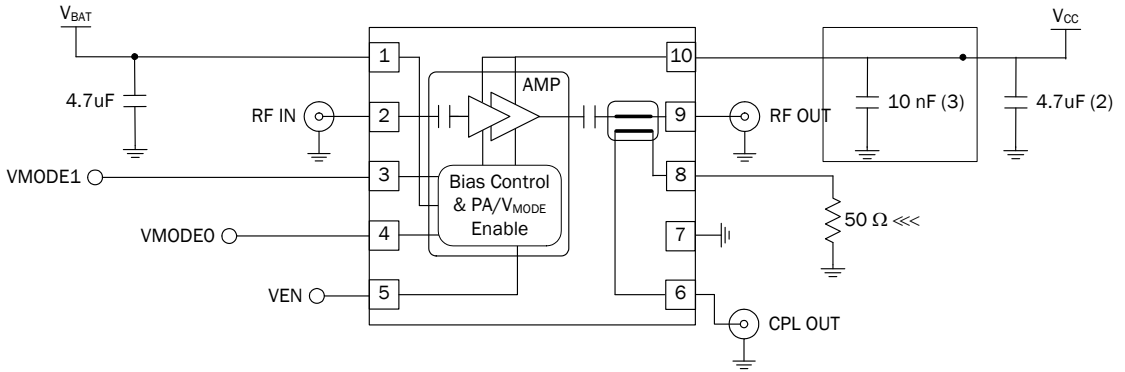
### Package Drawing



Notes:

1. Shaded area represents Pin 1 location
2. Defining I/O Pad Center:  
To define center of the I/O pad opening, draw a right triangle in one corner of the I/O pad. Then take the center of the hypotenuse to determine center of I/O pad

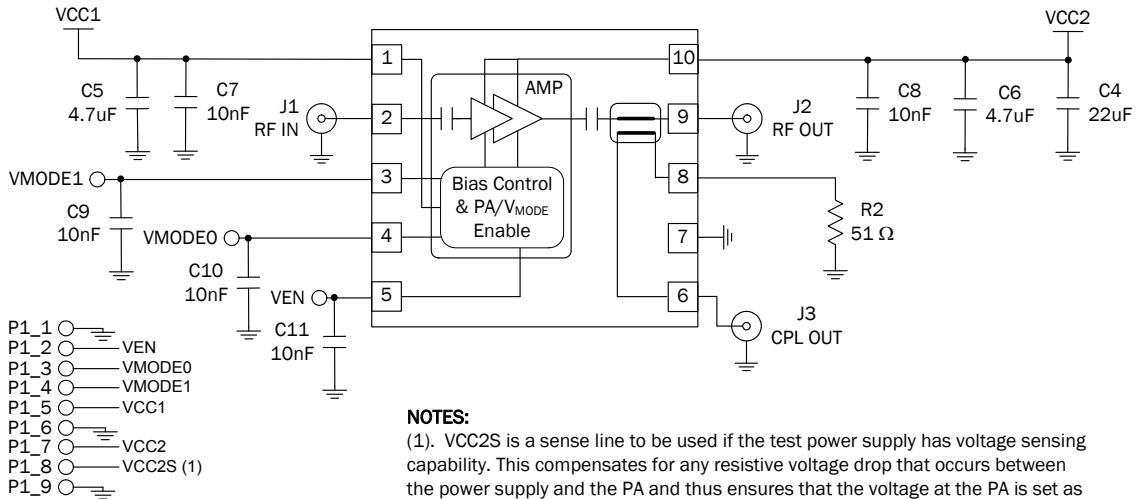
**Application Schematic**



**NOTES:**

- (1). The 50 Ω resistor should be removed if pin 8 is connected to another coupler for daisy chaining multiple couplers.
- (2). This capacitance value can be reduced for multi-PA with DC to DC converter applications where a total maximum capacitive load is required to be met. Keeping at least a 1uF capacitor close to the PA Vcc pin is recommended.
- (3). A capacitor of at least 10 nF should be placed close to the PA VCC pin (pin10) for optimum decoupling.

**Evaluation Board Schematic**



**NOTES:**

- (1). VCC2S is a sense line to be used if the test power supply has voltage sensing capability. This compensates for any resistive voltage drop that occurs between the power supply and the PA and thus ensures that the voltage at the PA is set as expected.

## PCB Design Requirements

### PCB Surface Finish

The PCB surface finish used for RFMD's qualification process is electroless nickel, immersion gold. Typical thickness is 3μinch to 8μinch gold over 180μinch nickel.

### PCB Land Pattern Recommendation

PCB land patterns for RFMD components are based on IPC-7351 standards and RFMD empirical data. The pad pattern shown has been developed and tested for optimized assembly at RFMD. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

### PCB Metal Land Pattern

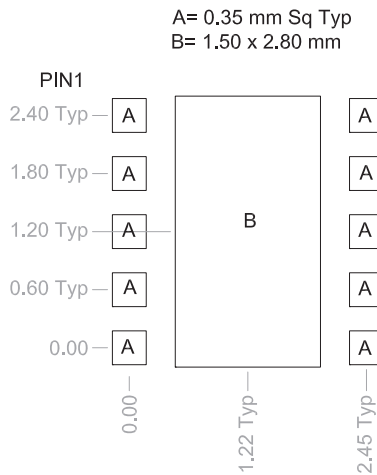
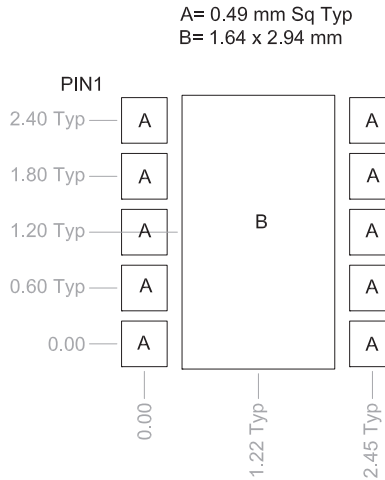


Figure 1. PCB Metal Land Pattern (Top View)

**PCB Solder Mask Pattern**

Liquid Photo-Imageable (LPI) solder mask is recommended. The solder mask footprint will match what is shown for the PCB metal land pattern with a 2mil to 3mil expansion to accommodate solder mask registration clearance around all pads. The center-grounding pad shall also have a solder mask clearance. Expansion of the pads to create solder mask clearance can be provided in the master data or requested from the PCB fabrication supplier.



**Figure 2. PCB Solder Mask Pattern (Top View)**

**Thermal Pad and Via Design**

The PCB land pattern has been designed with a thermal pad that matches the die paddle size on the bottom of the device.

Thermal vias are required in the PCB layout to effectively conduct heat away from the package. The via pattern has been designed to address thermal, power dissipation and electrical requirements of the device as well as accommodating routing strategies.

The via pattern used for the RFMD qualification is based on thru-hole vias with 0.203mm to 0.330mm finished hole size on a 0.5mm to 1.2mm grid pattern with 0.025mm plating on via walls. If micro vias are used in a design, it is suggested that the quantity of vias be increased by a 4:1 ratio to achieve similar results.