Data Sheet | March 2001 | File Number 3110.2

12-Bit, Low Cost, Monolithic D/A Converter

The HI-DAC80V is a monolithic direct replacement for the popular DAC80 and AD DAC80. Single chip construction along with several design innovations make the HI-DAC80V the optimum choice for low cost, high reliability applications. Intersil' unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching times and minimum glitch. On board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy.

Internally the HI-DAC80V eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-DAC80V is available as a voltage output device which is guaranteed over the 0^oC to 75^oC temperature range. It includes a buried zener reference featuring a low temperature coefficient as well as an on board operational amplifier. The HI-DAC80V requires only two power supplies and will operate in the range of ± (11.4V to 16.5V).

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HI3-DAC80V-5	0 to 75	24 Ld PDIP	E24.6

Features

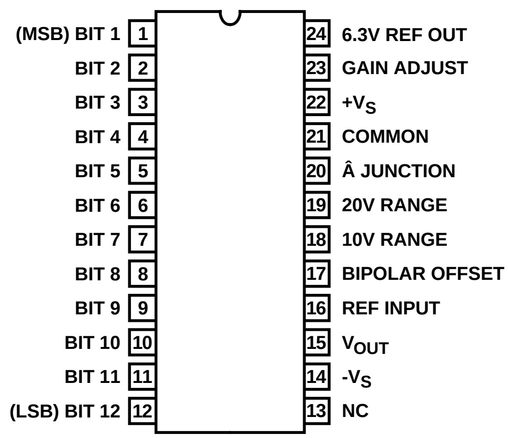
- DAC 80V Alternative Source
- Monolithic Construction
- Fast Settling Time (Typ) 1.5µs
- Guaranteed Monotonicity
- Wafer Laser Trimmed Linearity, Gain, Offset
- Span Resistors On-Chip
- On-Board Reference
- Supply Operation . . . . ±12V

Applications

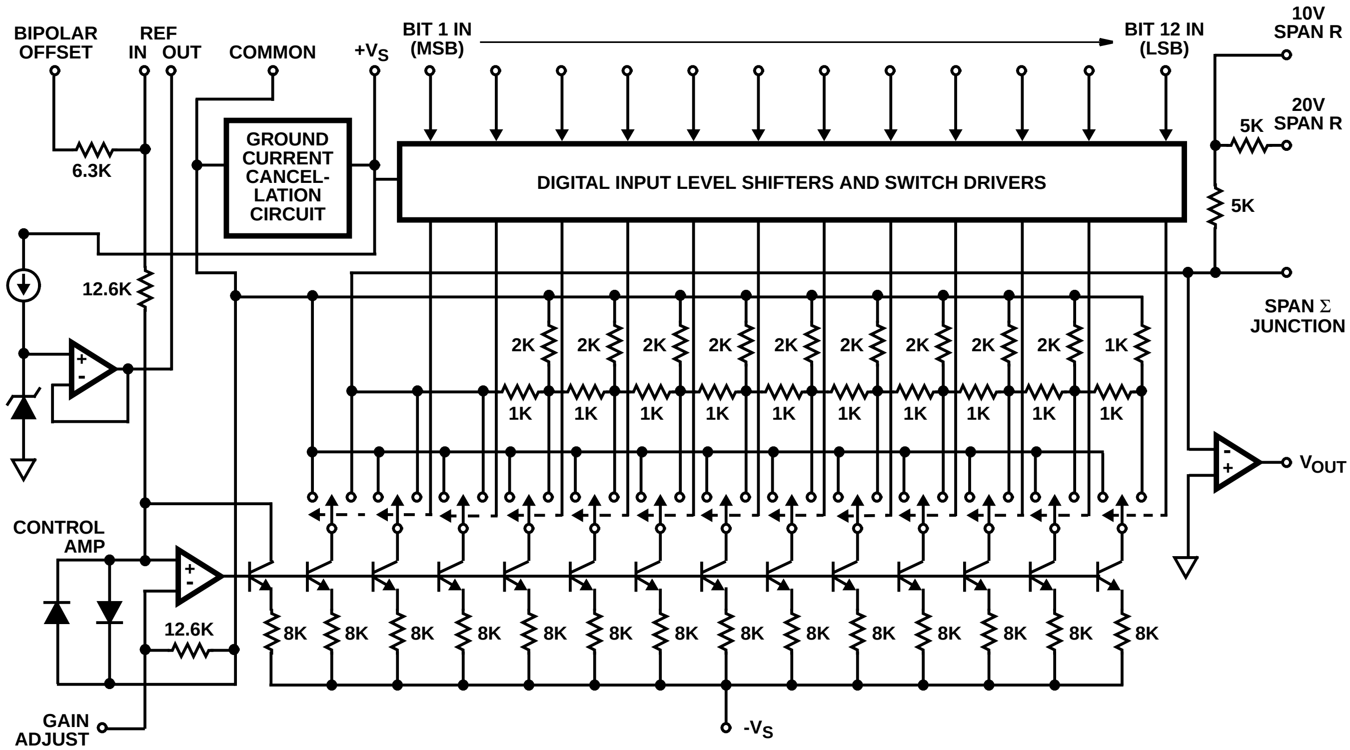
- High Speed A/D Converters
- Precision Instrumentation
- CRT Display Generation

Pinout

HI-DAC80V
(PDIP)
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings

Power Supply Inputs
- $+V_S$ . . . . . +20V
- $-V_S$ . . . . . -20V

Reference
- Input (Pin 16) . . . . . $+V_S$
- Output Drain 2.5mA

Digital Inputs (Bits 1 to 12) . . . . . -1V to $+V_S$

Operating Conditions

Temperature Range . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
PDIP Package	55

Maximum Power Dissipation
- PDIP Package 550mW

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

Die Characteristics

Process . . . . . Bipolar-DI
Transistor Count 214

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:
1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

$T_A = 25^oC$, V_S ±12V to ±15V (Note 5), Pin 16 Shorted to Pin 24, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Resolution		-	-	12	Bits
ACCURACY (Note 3)					
Linear Error	Full Temperature	-	$\pm^1/_4$	$\pm^1/_2$	LSB
Differential Linearity Error	Full Temperature	-	$\pm^1/_2$	$\pm^3/_4$	LSB
Monotonicity	Full Temperature		Guaranteed		
Gain Error	Full Temperature (Notes 2, 4)	-	±0.1	±0.3	% FSR
Offset Error	Full Temperature (Note 2)		±0.05	±0.15	% FSR
ANALOG OUTPUT					
Output Ranges (See Figure 2 and Table 2)		-	±2.5	-	V
		-	±5	-	V
		-	±10	-	V
		-	0 to 5	-	V
		-	0 to 10	-	V
Output Current		±5	-	-	mA
Output Resistance		-	0.05	-	Ω
Short Circuit Duration	To Common		Continuous		-
DRIFT (Note 3)					
Total Bipolar Drift (Includes Gain, Offset and Linearity Drifts)	Full Temperature	-	-	±20	ppm/^oC
Total Error					
Unipolar	Full Temperature (Note 6)	-	±0.08	±0.15	% FSR
Bipolar	Full Temperature (Note 6)	-	±0.06	±0.1	% FSR
Gain	With Internal Reference	-	±15	±30	ppm/^oC
	Without Internal Reference	-	±7	-	ppm/^oC

Electrical Specifications $T_A = 25^oC$, V_S ±12V to ±15V (Note 5), Pin 16 Shorted to Pin 24, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Unipolar Offset		-	±1	±3	ppm/^{o}C
Bipolar Offset		-	±5	±10	ppm/^{o}C
CONVERSION SPEED					
Settling Time					
With 10K Feedback	Full Scale Transition All Bits ON to OFF or OFF to ON to ±0.01% or FSR (Note 3)	-	3	-	µs
With 5K Feedback		-	1.5	-	µs
For 1 LSB Change		-	1.5	-	µs
Slew Rate		10	15	-	V/µs
INTERNAL REFERENCE					
Output Voltage		6.250	+6.3	6.350	V
Output Impedance		-	1.5	-	Ω
External Current		-	-	+2.5	mA
Tempco of Drift		-	5	-	ppm/^{o}C
DIGITAL INPUT (Note 2)					
Logic Levels					
Logic “1”	TTL Compatible At +1µA	+2	-	+5.5	V
Logic “0”	TTL Compatible At -100µA	0	-	+0.8	V
POWER SUPPLY SENSITIVITY (Notes 3, 5)					
+15V Supply		-	0.001	0.002	% FSR / %V_S
-15V Supply		-	0.001	0.002	% FSR / %V_S
POWER SUPPLY CHARACTERISTICS (Note 5)					
Voltage Range					
$+V_S$	Full Temperature	+11.4	+15	+16.5	V
$-V_S$	Full Temperature	-11.4	-15	-16.5	V
Current					
$+I_S$	Full Temperature, V_S = ±15V	-	+12	+15	mA
$-I_S$	Full Temperature, V_S = ±15V	-	-15	-20	mA

NOTES:

2. Adjustable to zero using external potentiometers.
3. See Definitions.
4. FSR is “Full Scale Range: and is 20V for ±10V range, 10V for ±5V range, etc.
5. The HI-DAC80V will operate with supply voltages as low as ±11.4V. It is recommended that output voltage range -10V to +10V not be used if the supply voltages are less than ±12.5V.
6. With Gain and Offset errors adjusted to zero at 25^{o}C.

Definitions of Specifications

Digital Inputs

The HI-DAC80V accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

Settling Time

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Intersil Corporation usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of $\pm^1/_2$ LSB about the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low. In a 12-bit system $\pm^1/_2$ LSB = ±0.012% of FSR.

TABLE 1.

DIGITAL INPUT	ANALOG OUTPUT		
	COMPLEMENTARY STRAIGHT BINARY	COMPLEMENTARY OFFSET BINARY	COMPLEMENTARY TWO'S COMPLEMENT†
MSB…LSB			
000…000	+ Full Scale	+ Full Scale	-LSB
100…000	Mid Scale-1 LSB	-1 LSB	+ Full Scale
111…111	Zero	- Full Scale	Zero
011…111	$+^1/_2$ Full Scale	Zero	- Full Scale

† Invert MSB with external inverter to obtain CTC Coding.

Thermal Drift

Thermal drift is based on measurements at 25°C, at high (T_H) and low (T_L) temperatures. Drift calculations are made for the high (T_H -25°C) and low (25°C-T_L) ranges, and the larger of the two values is given as a specification representing worst case drift.

Gain Drift, Offset Drift, Reference Drift and Total Bipolar Drift are calculated in parts per million per °C as follows:

$$\text{GainDrift} = \frac{\Delta FSR / \Delta °C}{FSR} \times 10^6$$

$$\text{OffsetDrift} = \frac{\Delta Offset / \Delta °C}{FSR} \times 10^6$$

$$\text{ReferenceDrift} = \frac{\Delta V_{REF} / (\Delta °C)}{V_{REF}} \times 10^6$$

$$\text{TotalBipolarDrift} = \frac{\Delta V_O / (\Delta °C)}{FSR} \times 10^6$$

NOTE: FSR = Full Scale Output Voltage - Zero Scale Output Voltage.

ΔFSR = FSR (T_H) - FSR (25°C),
or FSR (25°C) - FSR (T_L).
V_O = Steady State response to any input code.

Total Bipolar Drift (TBD) is the variation of output voltage with temperature, in the bipolar mode of operation. It represents the net effect of drift in Gain, Offset, Linearity and Reference Voltage. Total Bipolar Drift values are calculated, based on measurements as explained above. Gain and Offset need not be calibrated to zero at 25°C. The specified limits for TBD apply for any input code and for any power supply setting within the specified operating range.

Accuracy

Linearity Error (Short for "Integral Linearity Error." Also, sometimes called "Integral Nonlinearity" and "Nonlinearity".) The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to end-point linearity for D/A converter products from Intersil Corporation, i.e., the line is drawn between the end-points of the actual transfer characteristic (codes 00…0 and 11…1).

Differential Linearity Error The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

Monotonicity The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for Increasing code, or decrease for decreasing code.

Total Error The net output error resulting from all internal effects (primarily non-ideal Gain, Offset, Linearity and Reference Voltage). Supply voltages may be set to any values within the specified operating range. Gain and offset errors must be calibrated to zero at 25°C. Then the specified limits for Total Error apply for any input code and for any temperature within the specified operating range.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in $-V_S$, or $+V_S$ supplies. It is specified under DC conditions and expressed as full scale range percent of change divided by power supply percent change.

$$PSS = \frac{\dfrac{\Delta FullScaleRange \times 100}{FSR(Nominal)}}{\dfrac{\Delta V_S \times 100}{V_S(Nominal)}}$$

Glitch

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale, i.e., the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the Product of duration and amplitude.)

Decoupling and Grounding

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-DAC80V (preferably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

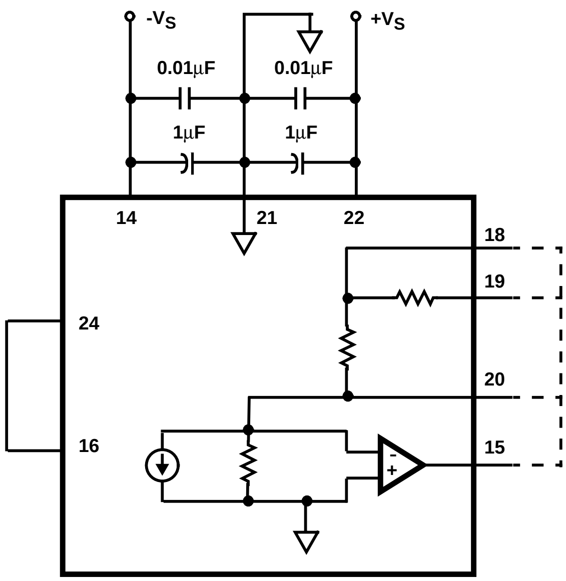


FIGURE 1.

Reference Supply

An internal 6.3V reference is provided on board the HI-DAC80V. The voltage (pin 24) is accurate to ±0.8% and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-DAC80V. All gain adjustments should be made under constant load conditions.

Output Voltage Ranges

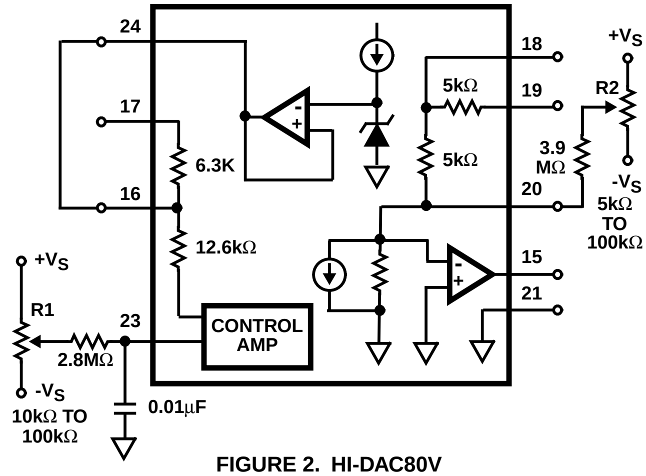


FIGURE 2. HI-DAC80V

TABLE 2. RANGE CONNECTIONS

		CONNECT		
	RANGE	**PIN 15**	**PIN 17**	**PIN 19**
Unipolar	0 to +5V	18	NC	20
	0 to +10V	18	NC	NC
Bipolar	±2.5V	18	20	20
	±5V	18	20	NC
	±10V	19	20	15

TABLE 3. GAIN AND OFFSET CALIBRATIONS

UNIPOLAR CALIBRATION	
Step 1:	Offset Turn all bits OFF (11 . . . 1) Adjust R2 for 0V out
Step 2:	Gain Turn all bits ON (00 . . . 0) Adjust R1 for FS - 1 LSB That is: 4.9988 for 0 to +5V range 9.9976 for 0 to +10V range
BIPOLAR CALIBRATION	
Step 1:	Offset Turn all bits OFF (11 . . . 1) Adjust R2 for Negative FS That is: -10V for ±10V range -5V for ±5V range -2.5V for ±2.5V range
Step 2:	Gain Turn all bits ON (00 . . . 0) Adjust R1 for Positive FS - 1 LSB That is: +9.9951V for ±10V Range +4.9976V for ±5V Range +2.4988V for ±2.5V Range
This Bipolar procedure adjusts the output range end points. The maximum error at zero (half scale) will not exceed the Linearity Error. See the “Accuracy” Specifications.	

Die Characteristics

DIE DIMENSIONS

108 mils x 163 mils

METALLIZATION

Type: Al
Thickness: 16kÅ ±2kÅ

TIE SUBSTRATE TO

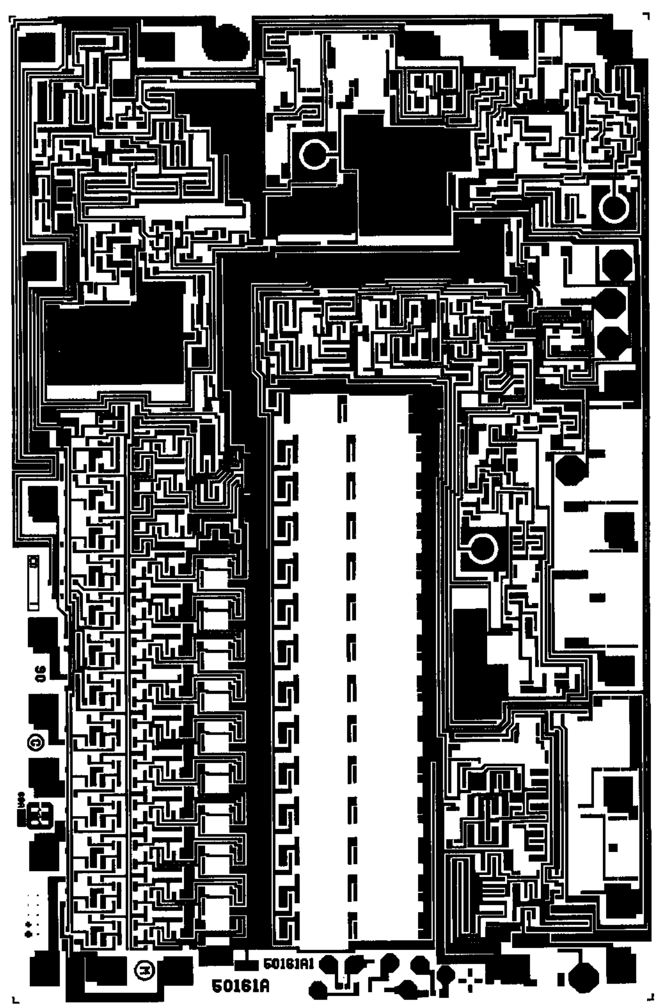
Ground

PASSIVATION

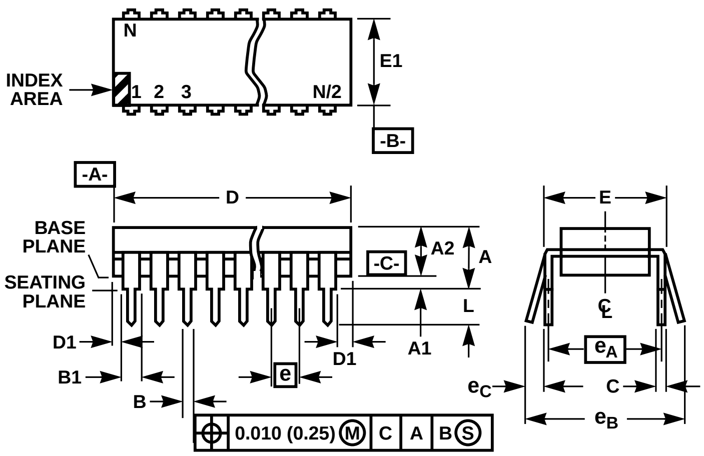
Type: Nitride over Silox
Nitride Thickness: 3.5kÅ ±0.5kÅ
Silox Thickness: 12kÅ ±1.5kÅ

Metallization Mask Layout

HI-DAC80V



Dual-In-Line Plastic Packages (PDIP)



E24.6 **(JEDEC MS-011-AA ISSUE B)**
24 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.150	1.290	29.3	32.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	24		24		9

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NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $\boxed{e_A}$ are measured with the leads constrained to be perpendicular to datum $\boxed{\text{-C-}}$.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

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