

## Universal Evaluation Board for Triple, High Speed Op Amps Offered in 14-Lead SOIC Packages

### FEATURES

- Enables quick breadboarding/prototyping**
- User-defined circuit configuration**
- Edge-mounted SMA connector provisions**
- Easy connection to test equipment and other circuits**

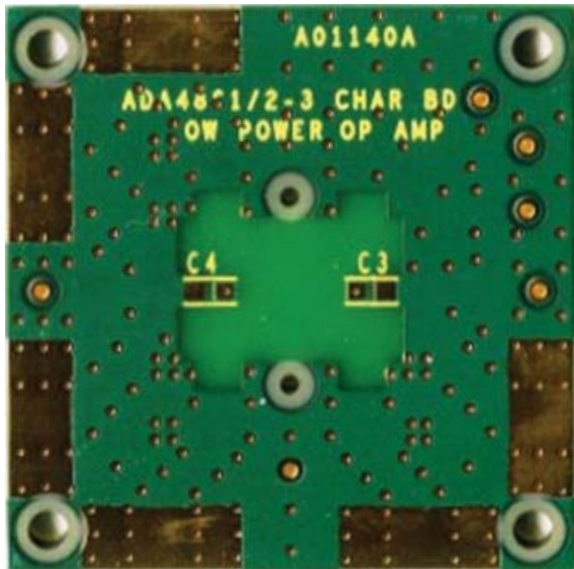
### GENERAL DESCRIPTION

The EB-O14R-3Z universal evaluation board is designed to help users evaluate the triple, high speed op amps offered in 14-lead SOIC packages. The EB-O14R-3Z is a bare board (that is, there are no components soldered to the board) that enables users to quickly prototype a variety of triple op amp circuits, which minimizes risk and reduces time to market. Figure 1 shows the component side of the bare evaluation board, and Figure 2 shows the circuit side of the bare evaluation board.

The evaluation board is a 2-layer printed circuit board (PCB) that accepts SMA edge-mounted connectors on the inputs and outputs for efficient connection to test equipment or other circuitry. The ground plane, component placement, and supply bypassing are designed to minimize parasitic inductances and capacitances.

Figure 3 shows the evaluation board schematic. The PCB layout pattern for the component side is shown in Figure 4, and the PCB layout pattern for the circuit side is shown in Figure 5.

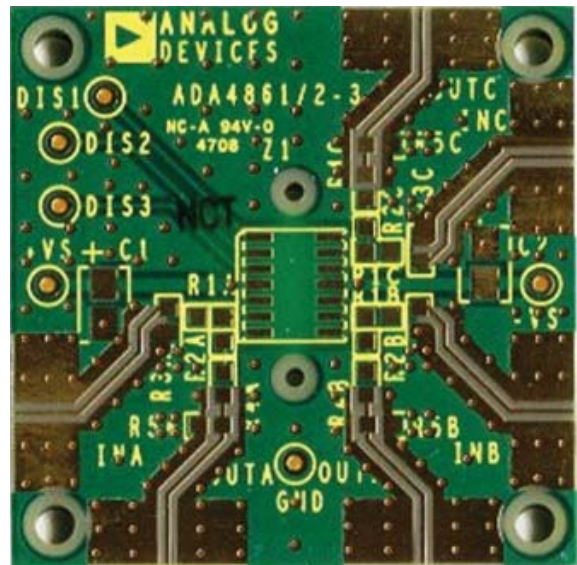
### EVALUATION BOARD COMPONENT AND CIRCUIT SIDE DIAGRAMS



**NOTES**  
1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELLING ON YOUR BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

Figure 1. EB-O14R-3Z Component Side of Evaluation Board

089296-001



**NOTES**  
1. THE EVALUATION BOARD SILKSCREEN PART NUMBER LABELLING ON YOUR BOARD MAY BE DIFFERENT FROM WHAT IS SHOWN HERE.

Figure 2. EB-O14R-3Z Circuit Side of Evaluation Board

089296-002

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**REVISION HISTORY**

3/10—Revision 0: Initial Version

# EVALUATION BOARD SCHEMATIC AND ARTWORK

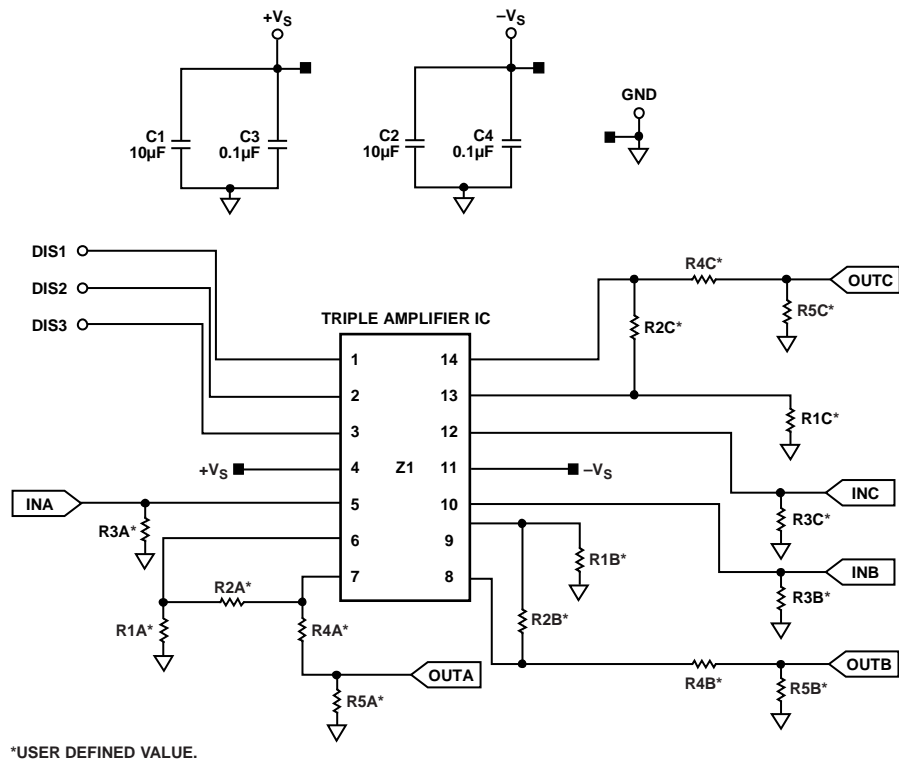


Figure 3. EB-O14R-3Z Universal Evaluation Board Schematic

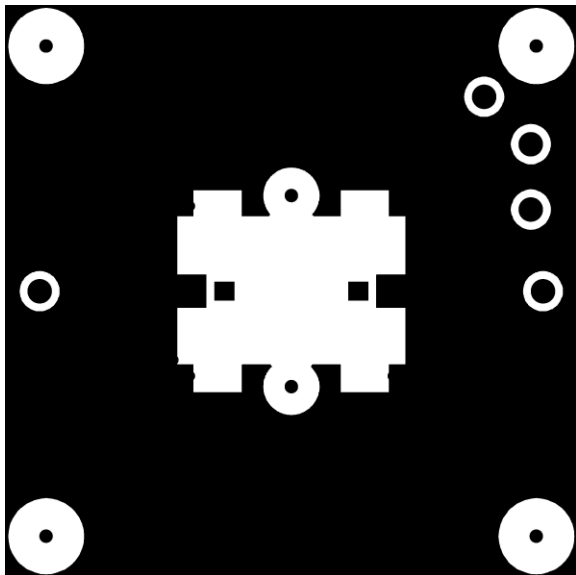


Figure 4. Board Layout Pattern, Component Side

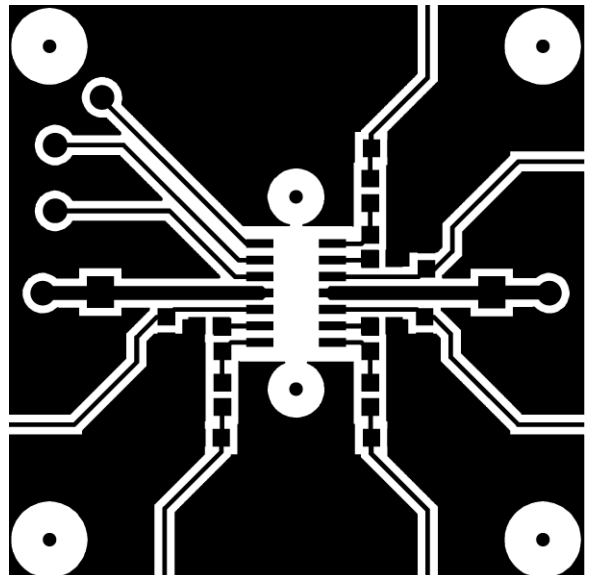


Figure 5. Board Layout Pattern, Circuit Side

## ORDERING INFORMATION

### BILL OF MATERIALS

Table 1.

Quantity	Reference Designator	Description	Package
6	+V <sub>S</sub> , -V <sub>S</sub> , DIS1, DIS2, DIS3, GND	Test point	TP
2	C1, C2	10 µF capacitor	C3548
2	C3, C4	User-defined capacitor	C0805
6	INA, INB, INC, OUTA, OUTB, OUTC	SMA/SMT	SMA/SMT
15	R1A, R1B, R1C, R2A, R2B, R2C, R3A, R3B, R3C, R4A, R4B, R4C, R5A, R5B, R5C	User-defined resistor	R0805
1	Z1	Triple amplifier IC	14-lead SOIC



#### ESD Caution

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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