PIC16(L)F1826/1827 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F1826/1827 family devices that you have received conform functionally to the current Device Data Sheet (DS41391**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1826/1827 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A7**).

Data Sheet clarifications and corrections start on page 12, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1826/1827 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	DEVICE ID<13:0>(1),(2)						
	DEV<8:0>	Revision ID for Silicon Revision					
		A2	A3	A4	A5	A6	A7
PIC16F1826	10 0111 100	0 0010	0 0011	0 0100	0 0101	0 0110	0 0111
PIC16LF1826	10 1000 100	0 0010	0 0011	0 0100	0 0101	0 0110	0 0111
PIC16F1827	10 0111 101	0 0010	0 0011	0 0100	0 0101	0 0110	0 0111
PIC16LF1827	10 1000 101	0 0010	0 0011	0 0100	0 0101	0 0110	0 0111

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC12(L)F1822/PIC16(L)F182X Memory Programming Specification"* (DS41390) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)					
				A2	A3	A4	A5	A6	A7
Data EE Memory	Memory Endurance	1.1	Erase/Write endurance limited.	X	X				
Program Flash Memory (PFM)	Endurance	2.1	Erase/Write endurance limited.	X	X				
Timer1	Timer0 Gate Source	3.1	Toggle mode works improperly.	X	X				
Oscillator	HS mode	4.1	Frequency/Voltage range.	X	X	X	X	X	X
Oscillator	HFINTOSC Ready/ Stable bit	4.2	Bits remained set to '1' after initial trigger.	X	X	X	X	X	X
Oscillator	Oscillator Start-up Timer (OST) bit	4.3	OST bit remains set.	X	X	X	X		
ADC	ADC Conversion	5.1	ADC Conversion may not complete.	X	X				
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	6.1	PWM 0% duty cycle direction change.	X	X				
Enhanced Capture Compare PWM (ECCP)	Enhanced PWM	6.2	PWM 0% duty cycle port steering.	X	X				
Resets	Power-on Reset (POR)	7.1	Reset under low-power conditions.		X				
Timer1	T1 Gate Toggle mode	8.1	T1 gate flip-flop does not clear.	X	X				
BOR	Wake-up from Sleep	9.1	Device resets on wake-up from Sleep (LF devices only).	X	X	X			
Enhanced Universal Synchronous Asynchronous Receiver (EUSART)	16-Bit High-Speed Asynchronous mode	10.1	Works improperly at maximum rate.	X	X	X	X	X	X
Enhanced Universal Synchronous Asynchronous Receiver (EUSART)	Auto-Baud Detect	10.2	Auto-Baud Detect may store incorrect count value in the SPBRG registers.	X	X	X	X		

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A7**).

1. Module: Data EE Memory

1.1 Data EE Memory Endurance

The typical write/erase endurance of the Data EE Memory is limited to 10k cycles.

Work around

Use error correction method that stores data in multiple locations.

Affected Silicon Revisions

A2	A3	A4	A5	A6	A7		
X	X						

2. Module: Program Flash Memory (PFM)

2.1 Program Flash Memory Endurance

The typical write/erase endurance of the PFM is limited to 1k cycles when V_{DD} is above 3.0V.

Work around

Use an error correction method that stores data in multiple locations.

Affected Silicon Revisions

A2	A3	A4	A5	A6	A7		
X	X						

3. Module: Timer1

3.1 Timer1 Gate Toggle Mode with Timer0 as Gate Source

Timer1 Gate Toggle mode provides unexpected results when Timer0 overflow is selected as the Timer1 gate source. We do not recommend using Timer0 overflow as the Timer1 gate source while in Timer1 Gate Toggle mode or when Toggle mode is used in conjunction with Timer1 Gate Single-Pulse mode.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5	A6	A7		
X	X						

4. Module: Oscillator

4.1 HS Oscillator Frequency

The Standard Operating Conditions for the HS Oscillator are as follows:

Characteristic	Min.	Typ†	Max.	Units	Conditions	Operating Temperature
Oscillator Frequency	1	—	20	MHz	HS Oscillator mode, V_{DD} > 2.3V	-40°C ≤ T_A ≤ +85°C
Oscillator Frequency	1	—	20	MHz	HS Oscillator mode, V_{DD} ≥ 2.8V	-40°C ≤ T_A ≤ +125°C

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5	A6	A7		
X	X	X	X	X	X		

4.2 OSCSTAT bits: HFIOFR and HFIOFS

When HFINTOSC is selected, the HFIOFR and HFIOFS bits will become set when the oscillator becomes ready and stable. Once these bits are set, they become “stuck”, indicating that HFINTOSC is always ready and stable. If the HFINTOSC is disabled, the bits fail to be cleared.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5	A6	A7		
X	X	X	X	X	X		

4.3 Oscillator Start-up Timer (OST) bit

During the Two-Speed Start-up sequence, the OST is enabled to count 1024 clock cycles. After the count is reached, the OSTS bit is set and the system clock is held low until the next falling edge of the external crystal (LP, XT or HS mode), before switching to the external clock source.

When an external oscillator is configured as the primary clock and Fail-Safe Clock mode is enabled (FCMEN = 1), any of the following conditions will result in the Oscillator Start-up Timer (OST) failing to restart:

- $\overline{\text{MCLR}}$ Reset
- Wake from Sleep
- Clock change from INTOSC to Primary Clock

This anomaly will manifest itself as a clock failure condition for external oscillators, which takes longer than the clock failure time-out period to start.

Work around

None.

Affected Silicon Revisions

A2	A3	A4	A5	A6	A7		
X	X	X	X				

5. Module: ADC

5.1 Analog-to-Digital Conversion

An ADC conversion may not complete under these conditions:

1. When FOSC is greater than 8 MHz and it is the clock source used for the ADC converter.
2. The ADC is operating from its dedicated internal FRC oscillator and the device is not in Sleep mode (any FOSC frequency).

   When this occurs, the ADC Interrupt Flag (ADIF) does not get set, the GO/DONE bit does not get cleared, and the conversion result does not get loaded into the ADRESH and ADRESL result registers.

   Work around

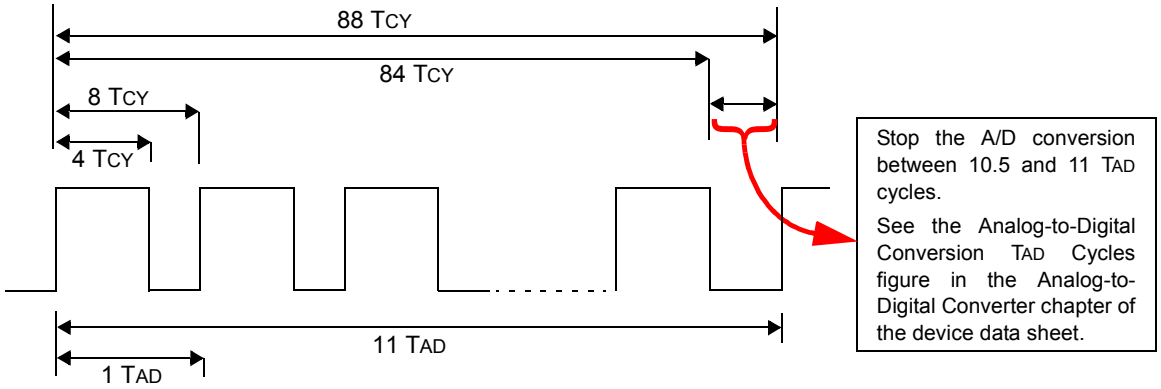
   Method 1: Select the system clock, FOSC, as the ADC clock source and reduce the FOSC frequency to 8 MHz or less when performing ADC conversions.

   Method 2: Select the dedicated FRC oscillator as the ADC conversion clock source and perform all conversions with the device in Sleep.

   Method 3: This method is provided if the application cannot use Sleep mode and requires continuous operation at frequencies above 8 MHz. This method requires early termination of an ADC conversion. Provide a fixed time delay in software to stop the A-to-D conversion manually, after all ten bits are converted, but before the conversion would complete automatically. The conversion is stopped by clearing the GO/DONE bit in software. The GO/DONE bit must be cleared during the last ½ TAD cycle, before the conversion would have completed automatically. Refer to Figure 1 for details.

FIGURE 1: INSTRUCTION CYCLE DELAY CALCULATION EXAMPLE

FOSC = 32 MHz
TCY = 4/32 MHz = 125 nsec
TAD = 1 µsec, ADCS = FOSC/32



See the ADC Clock Period (TAD) vs. Device Operating Frequencies table, in the Analog-to-Digital Converter section of the device data sheet.

In Figure 1, 88 instruction cycles (TCY) will be required to complete the full conversion. Each TAD cycle consists of eight TCY periods. A fixed delay is provided to stop the A/D conversion after 86 instruction cycles and terminate the conversion at the correct time as shown in the figure above.

Note: The exact delay time will depend on the TAD divisor (ADCS) selection. The TCY counts shown in the timing diagram above apply to this example only. Refer to Table 3 for the required delay counts for other configurations.

EXAMPLE 1: CODE EXAMPLE OF INSTRUCTION CYCLE DELAY

```
BSF    ADCON0, ADGO   ; Start ADC conversion
                      ; Provide 86
                        instruction cycle
                        delay here
BCF    ADCON0, ADGO   ; Terminate the
                        conversion manually
MOVF   ADRESH, W      ; Read conversion
                        result
```

For other combinations of FOSC, TAD values and Instruction cycle delay counts, refer to Table 3.

TABLE 3: INSTRUCTION CYCLE DELAY COUNTS BY TAD SELECTION

TAD	Instruction Cycle Delay Counts
FOSC/64	172
FOSC/32	86
FOSC/16	43

Affected Silicon Revisions

A2	A3	A4	A5	A6	A7		
X	X						

6. Module: Enhanced Capture Compare PWM (ECCP)

6.1 Enhanced PWM

When the PWM is configured for Full-Bridge mode and the duty cycle is set to 0%, writing the PxM<1:0> bits to change the direction has no effect on PxA and PxC outputs.

Work around

Increase the duty cycle to a value greater than 0% before changing directions.

Affected Silicon Revisions

A2	A3	A4	A5	A6	A7		
X	X						

6.2 Enhanced PWM

In PWM mode, when the duty cycle is set to 0% and the STRxSYNC bit is set, writing the STRxA, STRxB, STRxC and the STRxD bits to enable/disable steering to port pins has no effect on the outputs.

Work around

Increase the duty cycle to a value greater than 0% before enabling/disabling steering to port pins.

Affected Silicon Revisions

A2	A3	A4	A5	A6	A7		
X	X						

7. Module: Resets

7.1 Reset under Low-Power Conditions

This issue pertains only to the F product version, PIC16F1826/1827. The LF product version, PIC16LF1826/1827, is not affected by this issue in any way.

When employing any one of the low-power oscillators (ECL mode, LP mode, LFINTOSC, or Timer1 Oscillator as alternate system clock source) at temperatures of -20°C or colder while, at the same time, the source voltage supplied to the VDD pin drops below 2.7V, the device may experience a Power-on Reset (POR). Also, when the source voltage supplied to the VDD pin is below 2.7V, at temperatures of -20°C or colder, and a SLEEP instruction is executed, the device may experience a Power-on Reset (POR) upon entering Sleep mode, regardless of the type of clock source being used or which power-managed mode is being employed.

Work around

There are three separate work-arounds and one recommendation available to avoid this Reset condition. Employing any one of these will avoid this RESET condition.

1. Enabling the Brown-out Reset (BOR) circuitry.
2. Enabling the Fixed Voltage Reference (FVR) module.
3. Maintaining a source voltage (VDD) to the device above 2.7V when operating at temperatures of -20°C or colder.
4. Use the LF product version (PIC16LF1826/1827) when the VDD required is between 1.8V and 3.6V.

The ‘Affected Silicon Revisions’ below refers only to the F product version, PIC16F1826/1827.

Affected Silicon Revisions

A2	A3	A4	A5	A6	A7		
	X						

8. Module: Timer1

8.1 Timer1 Gate Toggle mode

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal. To perform this function, the Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the gate signal. Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When working properly, clearing either the T1GTM bit or the TMR1ON bit would also clear the output value of this flip-flop, and hold it clear. This is done in order to control which edge is being measured. The issue that exists is that clearing the TMR1ON bit does not clear the output value of the flip-flop and hold it clear.

Work around

Clear the T1GTM bit in the T1GCON register to clear and hold clear the output value of the flip-flop.

Affected Silicon Revisions

A2	A3	A4	A5	A6	A7		
X	X						

9. Module: BOR

9.1 BOR Reset

This issue affects only the PIC16LF1826/1827 devices. The device may undergo a BOR Reset when waking-up from Sleep and BOR is re-enabled. A BOR Reset may also occur the moment the software BOR is enabled.

Under certain voltage and temperature conditions and when either SBODEN or BOR_NSLEEP is selected, the devices may occasionally Reset when waking-up from Sleep or BOR is enabled.

Work around

Method 1: In applications where BOR use is not critical, turn off the BOR in the Configuration Word.

Method 2: Set the FVREN bit of the FVRCON register. Maintain this bit on at all times.

Method 3: When BOR module is needed only during run-time, use the software-enabled BOR by setting the SBODEN option on the Configuration Word. BOR should be turned off by software before Sleep, then follow the below sequence for turning BOR on after Wake-up:

a. Wake-up event occurs;

b. Turn on FVR (FVREN bit of the FVRCON register);

c. Wait until FVRRDY bit is set;

d. Wait 15 µs after the FVR Ready bit is set;

e. Manually turn on the BOR.

Method 4: Use the software-enabled BOR as described in Method 3, but use the following sequence:

a. Switch to internal 32 kHz oscillator immediately before Sleep;

b. Upon wake-up, turn on FVR (FVREN bit of the FVRCON register);

c. Manually turn on the BOR;

d. Switch the clock back to the preferred clock source.

Note: When using the software BOR, follow the steps in Methods 3 or 4 above when enabling BOR for the first time during program execution.

Affected Silicon Revisions

A2	A3	A4	A5	A6	A7		
X	X	X					

10. Module: Enhanced Universal Synchronous Asynchronous Receiver (EUSART)

10.1 16-Bit High-Speed Asynchronous Mode

The EUSART provides unexpected operation when the 16-Bit High-Speed Asynchronous mode is selected and the Baud Rate Generator Data register values are loaded with zero. We do not recommend using this configuration for EUSART communication. The configuration is shown below in the following table:

Configuration Bits			BRG Data Registers	
SYNC	BRG16	BRGH	SPBRGH Value	SPBRGL Value
0	1	1	00000000	00000000

Work around

Ensure that the SPBRGH or the SPBRGL register is loaded with a non-zero value.

Affected Silicon Revisions

A2	A3	A4	A5	A6	A7		
X	X	X	X	X	X		

10.2 Auto-Baud Detect

When using automatic baud detection (ABDEN), on occasion, an incorrect count value can be stored at the end of auto-baud detection in the SPBRGH:SPBRGL (SPBRG) registers. The SPBRG value may be off by several counts. This condition happens sporadically when the device clock frequency drifts to a frequency where the SPBRG value oscillates between two different values. The issue is present regardless of the baud rate Configuration bit settings.

Work around

When using auto-baud, it is a good practice to always verify the obtained value of SPBRG, to ensure it remains within the application specifications. Two recommended methods are shown below.

For additional Auto-Baud information, see Technical Brief TB3069*, "Use of Auto-Baud for Reception of LIN Serial Communications Devices: Mid-Range and Enhanced Mid-Range"*.

EXAMPLE 2: METHOD 1 – EUSART AUTO-BAUD DETECT WORK AROUND

In firmware, define default, minimum and maximum auto-baud (SPBRG) values according to the application requirements.

For example, if the application runs at 9600 baud at 16 MHz then, the default SPBRG value would be (assuming 16-bit/ Asynchronous mode) 0x67. The minimum and maximum allowed values can be calculated based on the application. In this example, a +/-5% tolerance is required, so tolerance is 0x67 * 5% = 0x05.

```
#define SPBRG_16BIT   *((*int)&SPBRG;                // define location for 16-bit SPBRG value

const int DEFAULT_BAUD = 0x0067;                     // Default Auto-Baud value
const int TOL = 0x05;                                // Baud Rate % tolerance
const int MIN_BAUD = DEFAULT_BAUD - TOL;             // Minimum Auto-Baud Limit
const int MAX_BAUD = DEFAULT_BAUD + TOL;             // Maximum Auto-Baud Limit
   •
   •
   •
ABDEN = 1;                                           // Start Auto-Baud
while (ABDEN);                                       // Wait until Auto-Baud completes

if((SPBRG_16BIT > MAX_BAUD)||(SPBRG_16BIT < MIN_BAUD))
{                                                    // Compare if value is within limits
    SPBRG_16BIT = DEFAULT_BAUD);                     // if out of spec, use DEFAULT_BAUD
}
   •                                                // if in spec, continue using the
   •                                                // Auto-Baud value in SPBRG
   •
```

EXAMPLE 3: METHOD 2 – EUSART AUTO-BAUD DETECT WORK AROUND

Similar to Method 1, define default, minimum and maximum auto-baud (SPBRG) values. In firmware, compute a running average of SPBRG. If the new SPBRG value falls outside the minimum or maximum limits, then use the current running average value (Average_Baud), otherwise use the auto-baud SPBRG value and calculate a new running average.

For example, if the application runs at 9600 baud at 16 MHz then, the default SPBRG value would be (assuming 16-bit/ Asynchronous mode) 0x67. The minimum and maximum allowed values can be calculated based on the application. In this example, a +/-5% tolerance is required, so tolerance is 0x67 * 5% = 0x05.

```
#define SPBRG_16BIT   *((*int)&SPBRG;                // define location for 16-bit SPBRG value

const int DEFAULT_BAUD = 0x0067;                     // Default Auto-Baud value
const int TOL = 0x05;                                // Baud Rate % tolerance
const int MIN_BAUD = DEFAULT_BAUD - TOL;             // Minimum Auto-Baud Limit
const int MAX_BAUD = DEFAULT_BAUD + TOL;             // Maximum Auto-Baud Limit

int Average_Baud;                                    // Define Average_Baud variable
int Integrator;                                      // Define Integrator variable
   •
   •
   •
Average_Baud = DEFAULT_BAUD;                         // Set initial average Baud rate
Integrator = DEFAULT_BAUD*15;                        // The running 16 count average
   •
   •
   •
ABDEN = 1;                                           // Start Auto-Baud
while (ABDEN);                                       // Wait until Auto-Baud completes

Integrator+ = SPBRG_16BIT;
Average_Baud = Integrator/16;
if((SPBRG_16BIT > MAX_BAUD)||(SPBRG_16BIT < MIN_BAUD))
{                                                    // Check if value is within limits
    SPBRG_16BIT = Average_Baud;                      // If out of spec, use previous average
}
else                                                 // If in spec, calculate the running
{                                                    // average but continue using the
    Integrator+ = SPBRG_16BIT;                       // Auto-Baud value in SPBRG
    Average_Baud = Integrator/16;
    Integrator- = Average_Baud;
}
   •
   •
   •
```

Affected Silicon Revisions

A2	A3	A4	A5	A6	A7		
X	X	X	X				

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41391**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Temperature Indicator

In Register 14-1: FVRCON: Fixed Voltage Reference Control Register, the TSEN and TSRNG bits that enable and select the range for the temperature indicator module are missing. The corrected register table is shown below.

REGISTER 14-1: FVRCON: FIXED VOLTAGE REFERENCE CONTROL REGISTER

R/W-0/0	R-q/q	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
FVREN	FVRRDY(1)	**TSEN(3)**	**TSRNG(3)**	CDAFVR<1:0>		ADFVR<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7 **FVREN:** Fixed Voltage Reference Enable bit
0 = Fixed Voltage Reference is disabled
1 = Fixed Voltage Reference is enabled

bit 6 **FVRRDY:** Fixed Voltage Reference Ready Flag bit(1)
0 = Fixed Voltage Reference output is not ready or not enabled
1 = Fixed Voltage Reference output is ready for use

bit 5 TSEN: Temperature Indicator Enable bit(3)
0 = Temperature Indicator is disabled
1 = Temperature Indicator is enabled

bit 4 TSRNG: Temperature Indicator Range Selection bit(3)
0 = VOUT = VDD - 2VT (Low Range)
1 = VOUT = VDD - 4VT (High Range)

bit 3-2 **CDAFVR<1:0>:** Comparator and DAC Fixed Voltage Reference Selection bit
00 = Comparator and DAC Fixed Voltage Reference Peripheral output is off.
01 = Comparator and DAC Fixed Voltage Reference Peripheral output is 1x (1.024V)
10 = Comparator and DAC Fixed Voltage Reference Peripheral output is 2x (2.048V)(2)
11 = Comparator and DAC Fixed Voltage Reference Peripheral output is 4x (4.096V)(2)

bit 1-0 **ADFVR<1:0>:** ADC Fixed Voltage Reference Selection bit
00 = ADC Fixed Voltage Reference Peripheral output is off.
01 = ADC Fixed Voltage Reference Peripheral output is 1x (1.024V)
10 = ADC Fixed Voltage Reference Peripheral output is 2x (2.048V)(2)
11 = ADC Fixed Voltage Reference Peripheral output is 4x (4.096V)(2)

Note 1: FVRRDY is always ‘1’ on devices with LDO (PIC16F1826/27).
2: Fixed Voltage Reference output cannot exceed VDD.
3: See Section 15.0, “Temperature Indicator Module”, for additional information.

2. Module: Oscillator

5.5 Fail-Safe Clock Monitor

5.5.3 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, executing a SLEEP instruction or changing the SCS bits of the OSCCON register. When the SCS bits are changed, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON. When the OST times out, the Fail-Safe condition is cleared **after successfully switching to the external clock source. The OSFIF bit should be cleared prior to switching to the external clock source. If the Fail-Safe condition still exists, the OSFIF flag will again become set by hardware**.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (10/2009)

Initial release of this document.

Rev B Document (02/2010)

Added PIC16F1826 and PIC16F1827 to this errata; Added Rev. A3 for PIC16F/LF1826/1827.

Data Sheet Clarifications: Added Modules 1 thru 5.

Rev C Document (05/2010)

Added Modules 5, 6 and 7.

Rev D Document (06/2010)

Removed Module 6 (Oscillator); Added Modules 7 (Resets) and 8 (Timer1).

Data Sheet Clarifications: Removed Modules 1 to 5.

Rev E Document (07/2010)

Revised Module 5.1; Other minor corrections.

Rev F Document (09/2010)

Added Silicon Revision A4.

Rev G Document (02/2011)

Added Module 9.

Rev H Document (05/2011)

Added Silicon Revision A5.

Data Sheet Clarifications: Added Module 1.

Rev J Document (02/2012)

Updated Table 1; Added Modules 4.2, 4.3 and 4.4' Added Module 10; Other minor corrections.

Data Sheet Clarifications: Added Module 2, Oscillator.

Rev K Document (07/2012)

Added MPLAB X IDE; Removed the Clock Switching module.

Rev L Document (11/2013)

Added Silicon Revision A6; Other minor corrections.

Rev M Document (03/2014)

Added Silicon Revision A7.

Note the following details of the code protection feature on Microchip devices:

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Printed on recycled paper.

ISBN: 9781620779828

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Fax: 44-118-921-5820

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