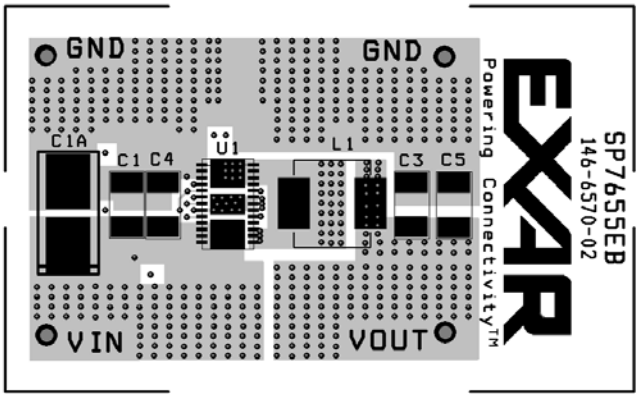
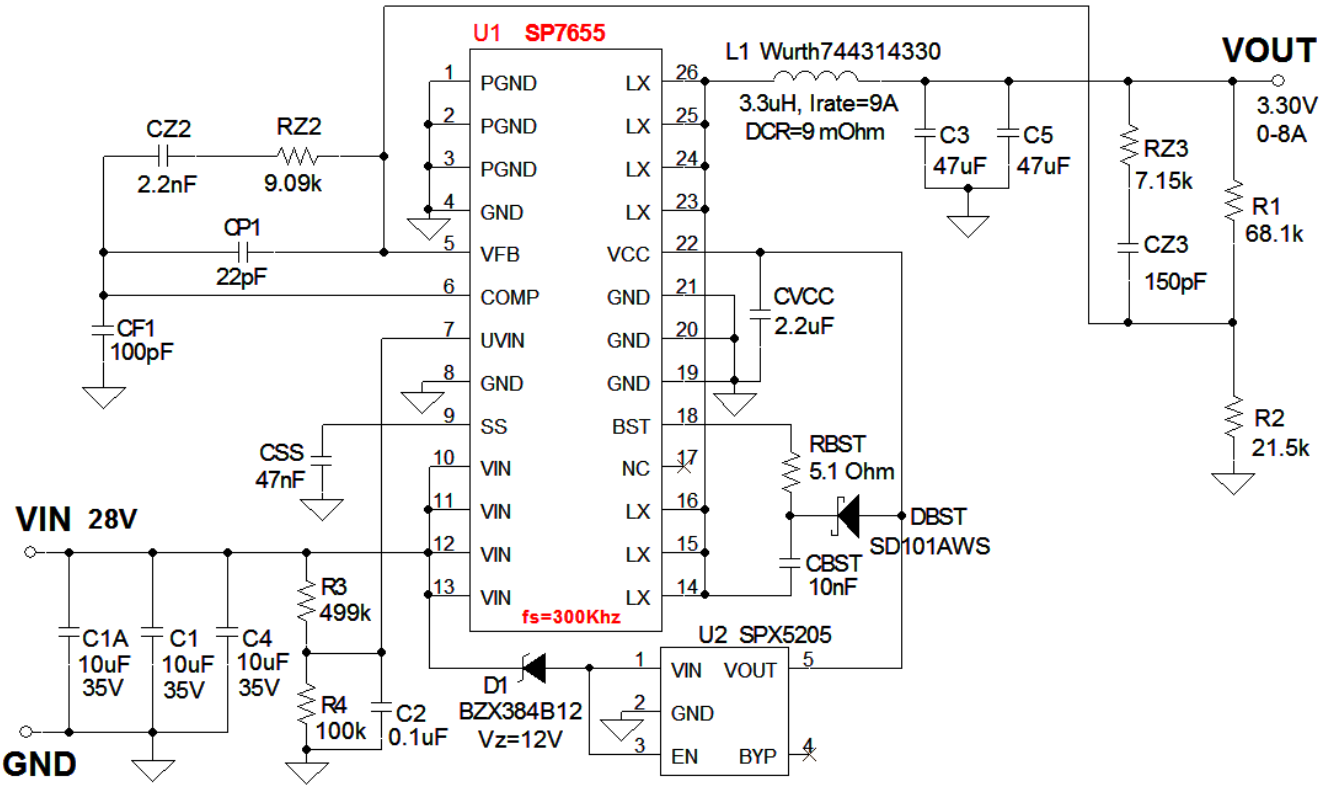
SP7655
Evaluation Board Manual

- Easy Evaluation for the SP7655ER 28V Input, 0 to 8A Output Synchronous Buck Converter
- Built in Low Rds(on) Power FETs
- UVLO Detects Both VCC and VIN
- High Integrated Design, Minimal Components
- High Efficiency: 86%
- Feature Rich: UVIN, Programmable Softstart, External VCC Supply and Output Dead Short Circuit Shutdown



SP7655EB SCHEMATIC



USING THE EVALUATION BOARD

1) Powering Up the SP7655EB Circuit

Connect the SP7655 Evaluation Board with an external +28V power supply. Connect with short leads and large diameter wire directly to the “VIN” and “GND” posts. Connect a Load between the VOUT and GND2 posts, again using short leads with large diameter wire to minimize inductance and voltage drops.

2) Measuring Output Load Characteristics

VOUT ripple can best be seen touching probe tip to the pad for C3 and scope GND collar touching GND side of C3 using short wrapped wire around collar – avoid a GND lead on the scope which will increase noise pickup.

3) Using the Evaluation Board with Different Output Voltages

While the SP7655 Evaluation Board has been tested and delivered with the output set to 3.30V, by simply changing one resistor, R2, the SP7655 can be set to other output voltages. The relationship in the following formula is based on a voltage divider from the output to the feedback pin VFB, which is set to an internal reference voltage of 0.80V.
Standard 1% metal film resistors of surface mount size 0603 are recommended.

$$Vout = 0.80V (R1 / R2 + 1) \Rightarrow R2 = R1 / [(Vout / 0.80V) – 1]$$

Where R1 = 68.1KΩ and for Vout = 0.80V setting, simply remove R2 from the board. Furthermore, one could select the value of R1 and R2 combination to meet the exact output voltage setting by restricting R1 resistance range such that $50K\Omega \leq R1 \leq 100K\Omega$ for overall system loop stability.

Note that since the SP7655 Evaluation Board design was optimized for 24V down conversion to 3.30V, changes of output voltage and/or input voltage will alter performance from the data given in the Power Supply Data section. In addition, the SP7655ER provides short circuit protection by sensing Vout at GND.

POWER SUPPLY DATA

The SP7655ER is designed with a very accurate 1.0% reference over line, load and temperature. Figure 1 data shows a typical SP7655 Evaluation Board Efficiency plot, with efficiencies up to 86% (Including generation of 5V Vcc) and output currents to 8A. SP7655ER Load Regulation is shown in Figure 2 of only 0.5% change in output voltage from 0.5A load to 8A load. Figures 3 and 4 illustrate a 4A to 8A and 0A to 8A Load Step. Start-up Response in Figures 5 and 6 show a controlled start-up with different output load behavior when power is applied where the input current rises smoothly as the Softstart ramp increases. Figure 7 and 8 show output voltage ripple less than 50mV at 8A load and less than 35mV at no load.

While data on individual power supply boards may vary, the capability of the SP7655ER of achieving high accuracy over a range of load conditions shown here is quite impressive and desirable for accurate power supply design.

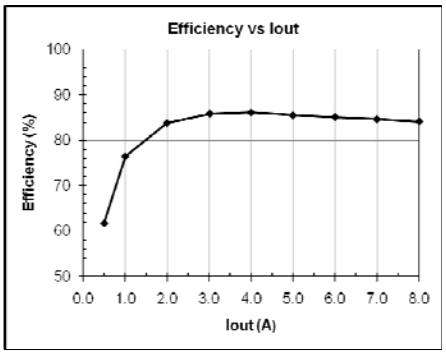


Figure 1. Efficiency vs Load

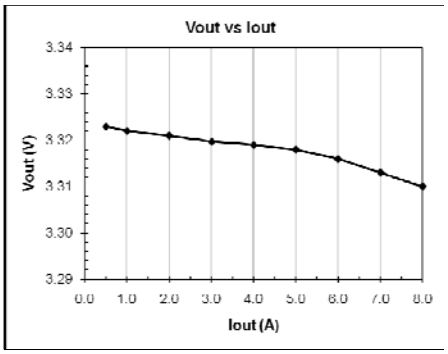


Figure 2. Load Regulation

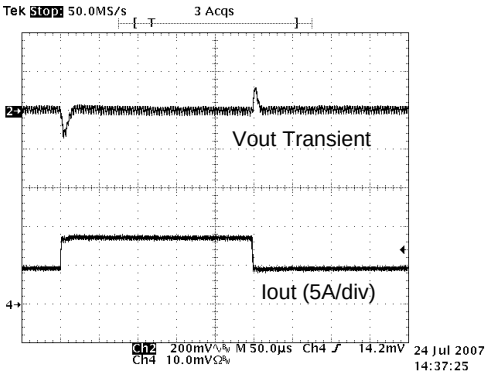


Figure 3. Load Step Response: 4->8A

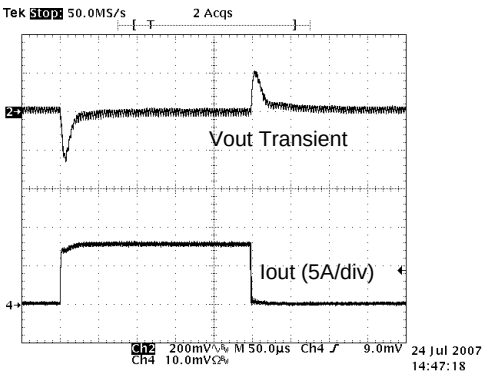


Figure 4. Load Step Response: 0->8A

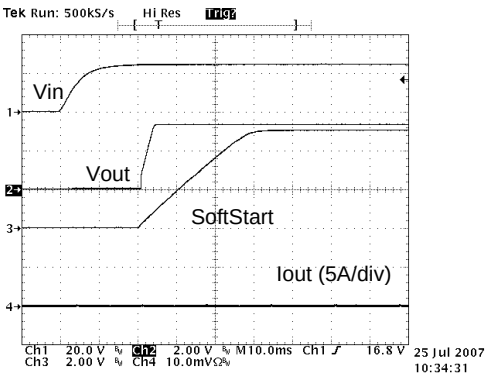


Figure 5. Start-Up Response: No Load

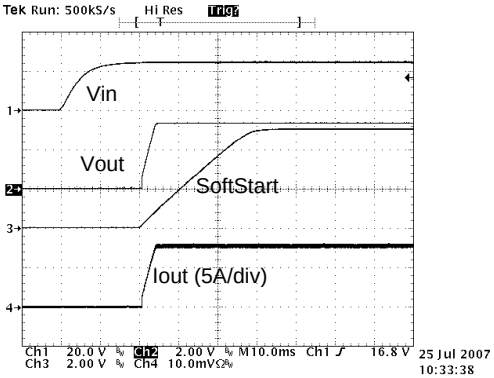


Figure 6. Start-Up Response: 8.0A Load

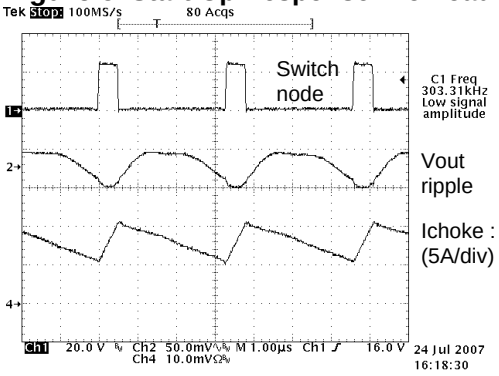


Figure 7. Output Ripple: 8A Load

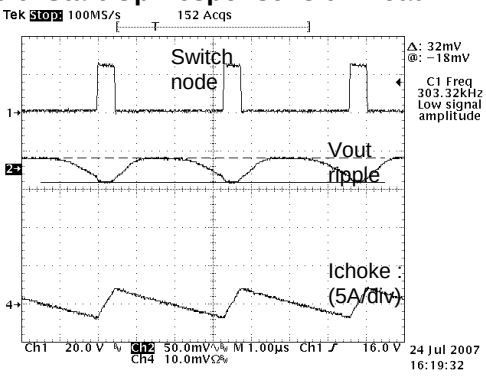
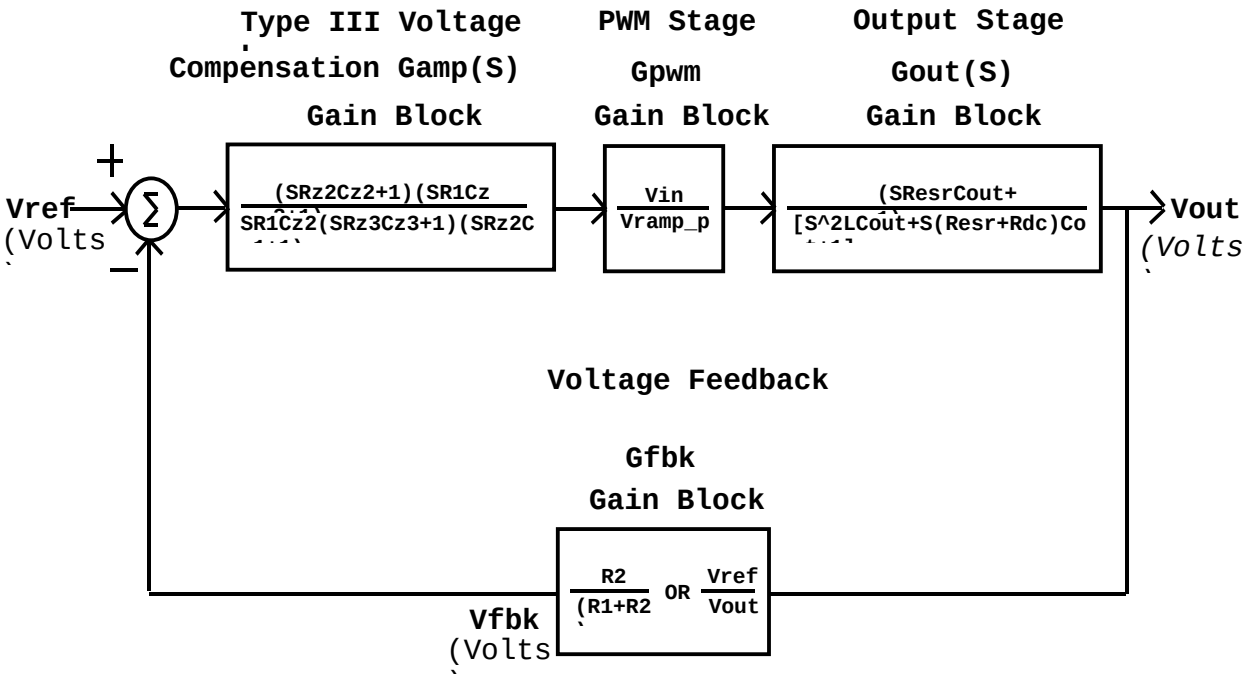


Figure 8. Output Ripple: No Load

TYPE III LOOP COMPENSATION DESIGN

The open loop gain of the SP7655EB can be divided into the gain of the error amplifier **Gamp(s)**, PWM modulator **Gpwm**, buck converter output stage **Gout(s)**, and feedback resistor divider **Gfbk**. In order to crossover at the selecting frequency **fco**, the gain of the error amplifier has to compensate for the attenuation caused by the rest of the loop at this frequency. The goal of loop compensation is to manipulate the open loop frequency response such that its gain crosses over 0dB at a slope of –20dB/dec. The open loop crossover frequency should be higher than the ESR zero of the output capacitors but less than 1/5 to 1/10 of the switching frequency **fs** to insure proper operation. Since the SP7655EB is designed with Ceramic Type output capacitors, a Type III compensation circuit is required to give a phase boost of 180° in order to counteract the effects of the output **LC** under damped resonance double pole frequency.



Definition

Resr := Output Capacitor Equivalent Series Resitance

Rdc := Output Inductor DC Resistance

Vramp_pp := SP7655 Internal RAMP Amplitude Peak to Peak Voltage

Condition

Cz2 >> Cp1 and R1 >> Rz3

Output Load Resistance >> Resr and Rdc

Figure 9. Voltage Mode Control Loop with Loop Dynamic for Type III Compensation

The simple guidelines for positioning the poles and zeros and for calculating the component values for Type III compensation are as follows:

a. Choose **fco** = fs / 5

b. Calculate **fp_LC**
fp_LC = 1 / 2π [(L) (C)] ^ 1/2

c. Calculate **fz_ESR**
fz_ESR = 1 / 2π (Resr) (Cout)

d. Select **R1** component value such that 50kΩ ≤ R1 ≤ 100kΩ

e. Calculate **R2** base on the desired Vout
R2 = R1 / [(Vout / 0.80V) – 1]

f. Select the ratio of **Rz2 / R1** gain for the desired gain bandwidth
Rz2 = R1 (Vramp_pp / Vin_max) (fco / fp_LC)

g. Calculate **Cz2** by placing the zero at ½ of the output filter pole frequency
Cz2 = 1 / π (Rz2) (fp_LC)

h. Calculate **Cp1** by placing the first pole at ESR zero frequency
Cp1 = 1 / 2π (Rz2) (fz_ESR)

i. Calculate **Rz3** by setting the second pole at ½ of the switching frequency and the second zero at the output filter double pole frequency
Rz3 = 2 (R1) (fp_LC) / fs

j. Calculate **Cz3** from **Rz3** component value above
Cz3 = 1 / π (Rz3) (fs)

k. Choose 100pF ≤ **Cf1** ≤ 220pF to stabilize the SP7655ER internal Error Amplify

As a particular example, consider this SP7655EB design with a **Type III** Voltage Loop Compensation component selection:

Vin = 24V
Vout = 3.30V @ 0 to 8A load
Select **L = 2.2uH** => yield ≈ 40% of maximum 8A output current ripple.
Select **Cout = 47uF Ceramic** capacitor (Resr ≈ **4mΩ**)
fs = 300khz SP7655 internal Oscillator Frequency
Vramp_pp = 1.0V SP7655 internal Ramp Peak to Peak Amplitude

Step by step design procedures:

a. **fco** = 300khz / 5 = 60khz

b. **fp_LC** = 1 / 2π [(2.2uH)(47uF)]^1/2 ≈ 15.6khz

c. **fz_ESR** = 1 / 2π (4mΩ)(47uF) ≈ 846Khz

d. **R1** = 68.1kΩ, 1%

e. **R2** = 68.1kΩ / [(3.30V / 0.80V) – 1] ≅ 21.5kΩ, 1%

f. **Rz2** = 68.1kΩ (1.0V / 28V) (60khz / 15.6khz) ≈ 9.09kΩ, 1%

g. **Cz2** = 1 / π (9.09kΩ) (15.6khz) ≈ 2200pF, X7R

h. **Cp1** = 1 / 2π (9.09 kΩ) (846Khz) ≈ 22pF

i. **Rz3** = 2 (68.1kΩ) (15.6khz) / 300khz ≈ 7.15kΩ, 1%

j. **Cz3** = 1 / π (7.15kΩ) (300khz) ≅ 150pF, COG

k. **Cf1** = 100pF to stabilize SP7650ER internal Error Amplify

PC LAYOUT DRAWINGS

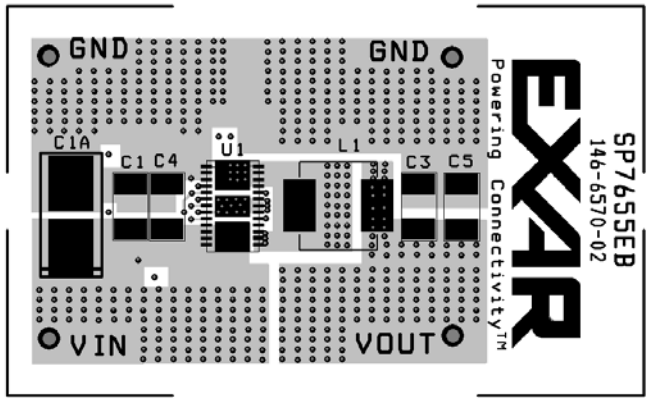


Figure 10.SP7655EB Top layer Component Placement

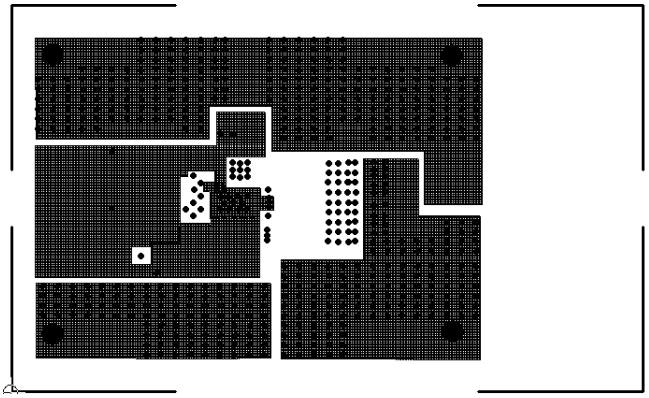


Figure 11. SP7655EB PC Layout 2nd Layer

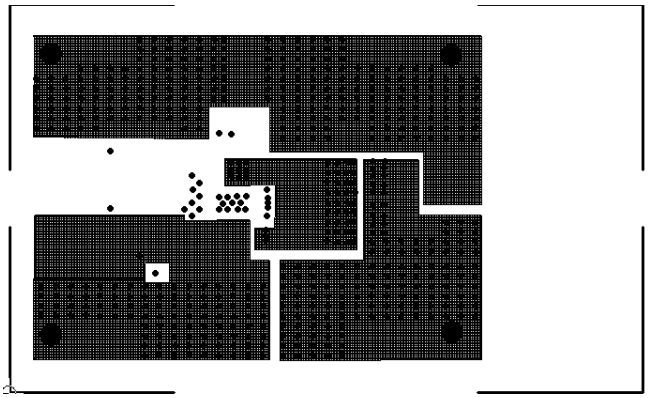


Figure 12. SP7655EB PC Layout 3rd Layer

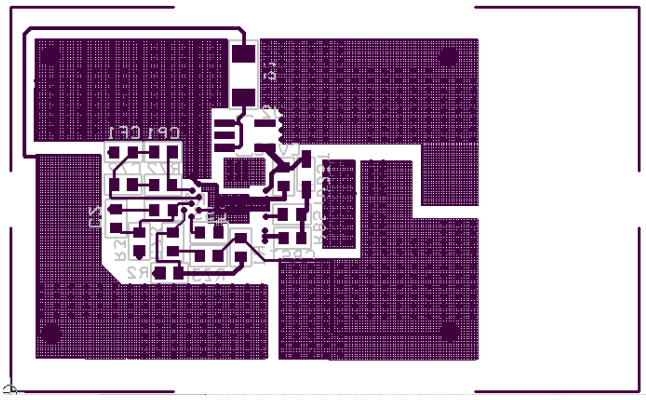


Figure 13. SP7655EB PC Layout Bottom layer

Figure 14.SP7655EB Bottom layer Component Placement

Table 1: SP7655EB List of Materials

SP7655 Vin=24V Evaluation Board Rev. 02 List of Materials							
Line No.	**Ref. Des.**	**Qty.**	**Manuf.**	**Part Number**	**Layout Size**	**Component**	**Vendor**
1	PCB	1	Exar	146-6570-02	1.75"X2.75"	SP7655EB evaluation board	www.exar.com
2	U1	1	Exar	SP7655EU	DFN-26	2-FETs 300KHZ Buck Ctrl	www.exar.com
3	U2	1	Exar	SPX5205M5-5.0	SOT-23-5	150mA LDO Voltage Reg.	www.exar.com
4	DBST	1	Vishay	SD101AWS	SOD-323	15mA Schottky Diode	www.vishay.com
5	D1	1	Vishay	BZX384B12	SOD-323	12V, 500mW Zener Diode	www.vishay.com
6	L1	1	Wurth Elektronik	744314330	7X7mm	3.3uH Coil 9A 9 mohm	www.we-online.com
7	C1,C1A,C4	1	muRata	GRM32ER1H106K	1210	10uF Ceramic X7R 50V	www.muRata.com
8	C2	1	muRata	GRM188R71E104K	0603	0.1uF Ceramic X7R 25V	www.muRata.com
9	C3,C5	2	muRata	GRM32ER61A476K	1210	47uF Ceramic X5R 10V	www.muRata.com
10	CVCC	1	muRata	GRM188R61A225K	0603	2.2uF Ceramic X5R 10V	www.muRata.com
11	CBST	1	muRata	GRM188R71H103K	0603	0.01uF Ceramic X7R 50V	www.muRata.com
12	CSS	1	muRata	GRM188R71E473K	0603	47,000pF Ceramic X7R 25V	www.muRata.com
13	CP1	1	muRata	GRM1885C1H220J	0603	22pF Ceramic C0G 50V	www.muRata.com
14	CZ2	1	muRata	GRM1885C1H222J	0603	2,200pF Ceramic C0G 50V	www.muRata.com
15	CF1	1	muRata	GRM1885C1H101J	0603	100pF Ceramic C0G 50V	www.muRata.com
16	CZ3	1	muRata	GRM1885C1H151J	0603	150pF Ceramic C0G 50V	www.muRata.com
17	RZ2	1	Vishay	CRCW06039K09F	0603	9.09K Ohm Thick Film Res 1%	www.vishay.com
18	R2	1	Vishay	CRCW060321K5F	0603	21.5K Ohm Thick Film Res 1%	www.vishay.com
19	RZ3	1	Vishay	CRCW06037K15F	0603	7.15K Ohm Thick Film Res 1%	www.vishay.com
20	R1	1	Vishay	CRCW060368K1F	0603	68.1K Ohm Thick Film Res 1%	www.vishay.com
21	R3	1	Vishay	CRCW0603499KF	0603	499K Ohm Thick Film Res 1%	www.vishay.com
22	RBST	1	Vishay	CRCW06035R10F	0603	5.1 Ohm Thick Film Res 1%	www.vishay.com
23	R4	1	Vishay	CRCW0603100KF	0603	100K Ohm Thick Film Res 1%	www.vishay.com
24	VIN, VOUT, GND, GND2	4	Mill-Max Mfg. Corp.	0300-1-15-01-47-01-10-0	.042" Dia	Terminal Posts	www.mil-max.com

ORDERING INFORMATION

Model	**Temperature Range**	**Package Type**
SP7655EB	-40°C to +85°C	SP7655 Evaluation Board
SP7655ER	-40°C to +85°C	26-pin DFN