Si3452/3

QUAD HIGH-VOLTAGE PORT CONTROLLER FOR POE AND POE+ PSES

Features

- Each Si3452/3 High Voltage Port Controller supports four PSE power interfaces
- Programmable current limits for PoE (15.4 W), PoE+ (30 W), and proprietary systems (up to 40 W) per port
- I^2C interface requires no external MCU for easy, low-cost management of 4 to 48 ports by the host system.
- Unique high-voltage component integration simplifies design, lowers power dissipation, minimizes external BOM, and reduces PCB footprint
  - Internal low-R_{ON} power FETs with current sense circuitry
  - Integrated transient voltage surge-suppressors
  - DC disconnect (Si3453) or proprietary dV/dt™ disconnect (Si3452) sensing methods
- Programmable architecture supports IEEE 802.3af (PoE) and pre-standard IEEE 802.3at (PoE+) PSEs
  - Programmable current limits for PoE (350 mA) and PoE+ (600 mA), and custom limits to 850 mA
  - Per-port current and voltage monitoring for sophisticated power management and control
  - Power policing mode
  - Robust multi-point detection
  - Supports 1-Event and 2-Event classification algorithms
- Comprehensive, robust fault protection circuitry
  - Supply under voltage lockout (UVLO)
  - Output current limit and short circuit protection
  - Foldback current limiting
  - Dual-threshold thermal overload protection
  - Fault source reporting for intelligent port management
- Extended operating temperature range: –10 to 85 ºC
- Compact, 6×6 mm^2, 40-pin QFN package. RoHS-compliant

Applications

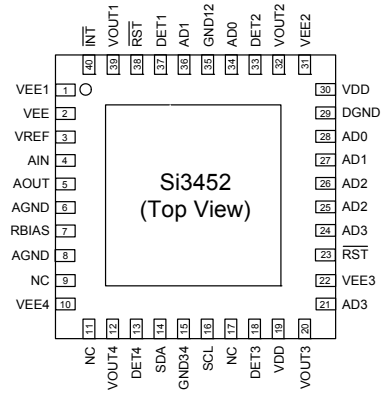
- Power over Ethernet Endpoint switches and Midspans for IEEE Std 802.3af and 802.3at
- Supports high power PDs, such as:
  - Pan/Tilt/Zoom security cameras
  - 802.11n WAPs
  - Multi-band, multi-radio WAPs
  - Security and RFID systems
  - Industrial automation systems
  - Networked audio
- IP Phone Systems and iPBXs
- Metropolitan area networked WAPs, cameras, and sensors
- WiMAX ASN/BTS and CPE/ODU systems

Ordering Information:

See page 29.

Pin Assignments

40-pin QFN



See "8. Pin Descriptions" on page 26.

Description

When connected directly to the host system or configured in Auto mode, each Si3452/3 high voltage port controller provides all of the critical circuitry and sophisticated power measurement functionality for the high voltage interfaces of four complete PSE ports. The Si3452/3 fully integrates robust, low-R_{ON} (0.3 Ω typ.) power MOSFET switches; low power dissipation current sensing circuitry; and transient voltage surge-suppression devices.

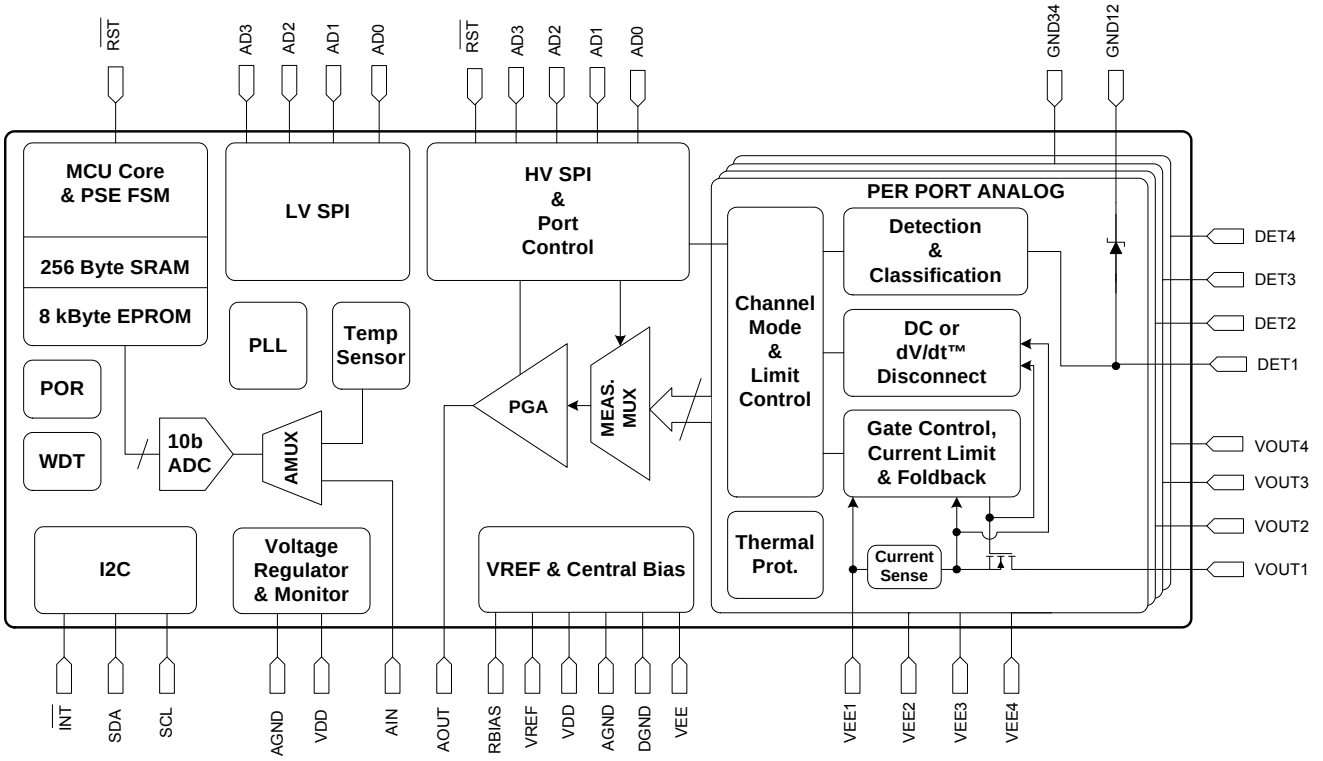
The on-chip current sense circuitry and power MOSFETs provide programmable scaling of current limits to match either PoE (350 mA, 15.4 W), PoE+ (600 mA, 30 W) and extended (800 mA, 40 W) power requirements on a per-port basis. Designed for use in Endpoint PSE (e.g., Ethernet switches) or Midspan PSE (e.g., inline power injectors) applications, each Si3452/3 also performs the IEEE-required powered device (PD) detection, classification, and disconnect functionality.

The flexible architecture enables powered device disconnect detection using either DC disconnect (Si3453), or Silicon Laboratories' proprietary dV/dt™ disconnect (Si3452) sensing algorithm. dV/dt disconnect is an alternative to DC disconnect that requires no additional BOM components, does not dissipate extra device power, and fully interoperates with all powered devices. Also provided are multi-point detection algorithms, and per-port current and voltage monitoring.

Intelligent protection circuitry includes power supply under voltage lockout (UVLO); port output current limiting and short circuit protection; thermal overload sensing and port shutdown; and transient voltage surge-suppressors capable of protecting the Si3452/3 from a variety of harsh surge events seen on the RJ-45 interface.

To maximize system design flexibility and minimize cost, each Si3452/3 connects directly to a system host controller through an I^2C serial interface, eliminating the need for an external MCU. The Si3452/3 can be set to one of 12 unique addresses, allowing control of up to 48 ports on a single I^2C bus.

Functional Block Diagram



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1. Electrical Specifications

Unless noted otherwise, specifications apply over the operating temperature range with VDD = +3.3 V, and VEE = –48 V relative to GND.

VDD pins should be electrically shorted. AGND pins, DGND, GND12, and GND34 should be electrically shorted ("GND"). VEE, VEE1, VEE2, VEE3, and VEE4 should be electrically shorted ("VEE").

VPort for any port is measured from GND to the respective VOUTn.

Table 1. Absolute Maximum Ratings[1]

Type	Description	Rating	Unit
Supply voltages	VEE to GND	–62 to +0.3	V
	VDD to GND	–0.3 to +3.6	V
	VDD1 to VDD2	–0.3 to +0.3	V
	Any VEE to any other VEE	–0.3 to +0.3	V
	Any GND to any other GND	–0.3 to +0.3	V
Voltage on digital pins	SDA, SCL, ADn, $\overline{RST}$, $\overline{INT}$	(GND – 0.3) to (VDD + 0.3)	V
Voltage on analog pins	VREF, AIN, AOUT, RBIAS, OSC	(GND – 0.3) to (VDD + 0.3)	V
	VOUTn, DETn	(VEE – 0.3) to (GND + 0.3)	V
DETn peak currents during surge events[2]		±5	A
Maximum continuous power dissipation[3]		1.2	W
Maximum junction temperature		125	°C
Ambient storage temperature		–55 to 150	°C
Lead temperature (soldering, 10 seconds maximum)		260	°C

Notes:

1. Functional operation should be restricted to those conditions specified in the Recommended Operating Conditions section of this data sheet. Functional operation or specification compliance is not implied at these conditions. Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device.
2. See IEEE Std 802.3-2005, clause 33.4 for a description of surge events.
3. If all ports are on with 600 mA load, the power dissipation is <1.2 W. At 85 °C ambient with the expected 32 °C/W thermal impedance, the junction temperature would be 123.4 °C, which is within the 125 °C maximum rating.

Table 2. Recommended Operating Conditions

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Operating temperature	T_A		–10	—	85	°C
Thermal impedance*	θ_{JA}	No airflow	—	32	—	°C/W
		1 m/s airflow	—	28	—	
Power Supply Voltages						
V_{EE} supply voltage	V_{EE}	For IEEE 802.3af (15.4 W) apps.	–57	–48	–45	V
		For IEEE 802.3at (30 W) apps.	–57	–54	–51	
V_{DD} supply voltage	V_{DD}		3.0	3.3	3.6	V
Power Supply Currents						
V_{EE} supply current	I_{EE}	All ports on, excluding load current.	—	4	—	mA
		All ports in shutdown mode	—	1	5	
V_{DD} supply current	I_{DD}		—	10	—	mA

***Note:** Modeled with six parts, evenly spaced on a 30 x 120 mm^2, four-layer board with 25 thermal vias to a Vneg plane on the back.

Table 3. UVLO, and Reset Specifications

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{DD} reset threshold	V_{RST}		—	1.75	—	V
V_{DD} power-on ramp*		Ramp from 0 V to 1.8 V	—	—	1	ms
$\overline{RST}$ input high voltage			0.7 x V_{DD}	—	—	V
$\overline{RST}$ input low voltage			—	—	0.8	V
RST input leakage		$\overline{RST}$ = 0 V	—	—	40	µA
Reset time delay	T_{RSTDLY}	Time between end of reset and beginning of normal operation	—	—	TBD	msec
Reset assertion time	T_{RST}	$\overline{RST}$ low time to generate system reset	15	—	—	µs
V_{EE} monitor accuracy	V_{EEMON}	Measured V_{EE} relative to actual V_{EE} for V_{EE} (–44 to –57 V)	–1.5	—	1.5	V
V_{EE} UVLO threshold	V_{UVLO}	Point at which VEE UVLO is declared. VEE going negative VEE going positive	 — —	 –36 –33	 — —	V

***Note:** If V_{DD} ramp time is slower than 1 msec, hold the reset pins low until V_{DD} is above 3.0 V to insure proper reset operation.

Table 4. Detection Specifications

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Detection current limit	I_{LIM_DET}	Measured with DETn shorted to GND	—	3	5	mA
Detection voltage, when R_{DET} = 25 kΩ	V_{DET1} V_{DET2} V_{DET3}		— — —	–4.0 –8.0 –4.0	— — —	V
Detection slew rate			—	—	0.1	V/µs
Detection probe duration	T_{PROBE}		10	—	30	ms
Detection probe cycle time	T_{DET}		—	—	500	ms
Minimum valid signature resistance	R_{DET_MIN}		15	—	19	kΩ
Maximum valid signature resistance	R_{DET_MAX}		26.5	—	33	kΩ
Resistance at which open circuit is declared	R_{OPEN}		100	—	400	kΩ
Resistance at which short circuit is declared	R_{SHORT}		150	—	400	Ω
Valid detect capacitance	C_{DET_VALID}		—	—	150	nF
Invalid detect capacitance	C_{DET_INVALD}		10	—	—	µF

Table 5. Classification Specifications

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Class event voltage	V_{CLASS}	0 mA < I_{Port} < 45 mA	–15.5	—	–20.5	V
Mark event voltage	V_{MARK}	0 mA < I_{Port} < 5 mA	–7	—	–10	V
Classification current limit	I_{LIM_CLASS}	Measured with DETn shorted to GND	55	—	100	mA
Classification current regions		Class 0 Class 1 Class 2 Class 3 Class 4 Overcurrent	0 8 16 25 35 51	— — — — — —	5 13 21 31 45 —	mA
Classification delay	T_{CLASS_DLY}	Time from end of valid detect cycle to classification begin	—	5	—	ms
Classification event time	T_{CLE}	Width of valid V_{CLASS} probe for 1-Event or 2-Event classification	10	—	30	ms
Mark event time	T_{ME}	Width of mark between classification events	—	8	—	ms

Table 6. VOUT Drive and Power-on Specifications

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Max output resistance (port on)	R_{ON}	I_{Port} ≤ 720 mA	—	0.3	0.6	Ω
VOUTn operating current limit	I_{LIM}	PoE (≤15.4 W) mode PoE+ (>15.4 W) mode	400 800	425 850	450 —	mA
Overload current threshold	I_{CUT}	Class 0 Class 1 (class policing enabled)[1] Class 2 (class policing enabled)[1] Class 3 Class 4[2]	350 91 160 350 600	— — — — —	— — — — —	mA
Over current time limit[3]	T_{OVLD}	Load current ≥ I_{CUT} or I_{LIM}	50	—	75	ms
VOUTn turn-on slew	T_{RISE}	10% to 90%	15	70	—	µs
Power turn on timing	T_{PON}	Time from end of valid detect to power on	—	—	400	ms
VOUTn leakage current	I_{OUT_LEAK}	Port in shutdown	—	10	—	µA

Notes:

1. In auto mode, class policing is automatically enabled. In manual mode, I_{CUT} must be programmed manually. See "5.4. Port Configuration (Registers 0x0A–0x011)" on page 18 for more information.
2. 600 mA is consistent with the IEEE 802.3at draft standard. I_{CUT} is user-programmable in 3.2 mA increments to over 800 mA for non-standard applications.
3. For 2x mode and extreme overload or short-circuit events, T_{OVLD} will dynamically decrease to prevent excessive FET heating. This is consistent with the 802.3at draft.

Table 7. DC- and dV/dt™ Disconnect Specifications

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Load current to prevent disconnect	I_{ON}		10	—	—	mA
Load current to guarantee disconnect	I_{OFF}	dc disconnect	—	—	5	mA
		dV/dt™ disconnect	—	—	2	mA
Disconnect delay	T_{DCDV_DLY}	Time from I_{OFF} load current to port turn off	300	—	400	ms

Table 8. Port Measurement and Monitoring Specifications

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Port current measurement offset	I_{OFFSET}	$0 \le I_{PORT} \le I_{CUT}$. For final I_{PORT} reading, add offset to % of reading tolerance.	–2	—	2	mA
Port current measurement tolerance	$\%_{TOL}$		–4	—	4	%

Table 9. SMBus (I^2C) Electrical Specifications

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Input low voltage	V_{IL}	SCL, SDA pins @ –10 °C	—	—	0.9	V
		SCL, SDA pins @ full temp range			0.8	
Input high voltage	V_{IH}	SCL, SDA pins	0.7 × V_{DD}	—	—	V
Output low voltage	V_{OL}	SCL, SDA pins, driving ≤ 8.5 mA	—	—	0.6	V
Input leakage current	I_L	SCL, SDA pins	—	—	40	µA

Table 10. Address Pin Electrical Specifications*

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Input low voltage	V_{IL}	AD0, AD1, AD2, AD3 pins			0.8	V
Input high voltage	V_{IH}	AD0, AD1, AD2, AD3 pins	0.7 x V_{DD}	—	—	V
Input leakage current	I_H, I_L	AD0, AD1, AD2, AD3 pins	–10	—	10	µA

***Note:** At power-up, these pins are logic inputs. A 10 kΩ pull up or pull down resistor is used for address selection. After address recognition, the pins are used for internal communications.

Table 11. SMBus (I^2C) Timing Specifications (see Figure 1)

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Serial bus clock frequency	f_{SCL}		0	—	400	kHz
SCL high time	t_{SKH}		600	—	—	ns
SCL low time	t_{SKL}		1.3	—	—	µs
SCL, SDA rise time	t_{R_SCL}		20	—	300	ns
SCL, SDA fall time	t_{F_SCL}		20	—	150	ns
Bus free time	t_{BUF}	Between START and STOP conditions.	1.3	—	—	µs
Start hold time	t_{STH}	Between START and first low SCL.	600	—	—	ns
Start setup time	t_{STS}	Between SCL high and START condition.	600	—	—	ns
Stop setup time	t_{SPS}	Between SCL high and STOP condition.	600	—	—	ns
Data hold time	t_{DH}		150	—	—	ns
Data setup time	t_{DS}		200	—	—	ns
Time from hardware or software reset until start of I^2C traffic.	t_{RESET}	Reset to start condition	TBD	—	—	ms

Notes:
1. Not production tested (guaranteed by design).
2. All timing references measured at V_{IL} and V_{IH}.
3. The Si3452/3 will stretch (pull down on) SCK during the ACK time period if required. The maximum SCL stretching is 10 µsec; so, SCL only needs to be bidirectional for I^2C bus speeds over 50 kHz.

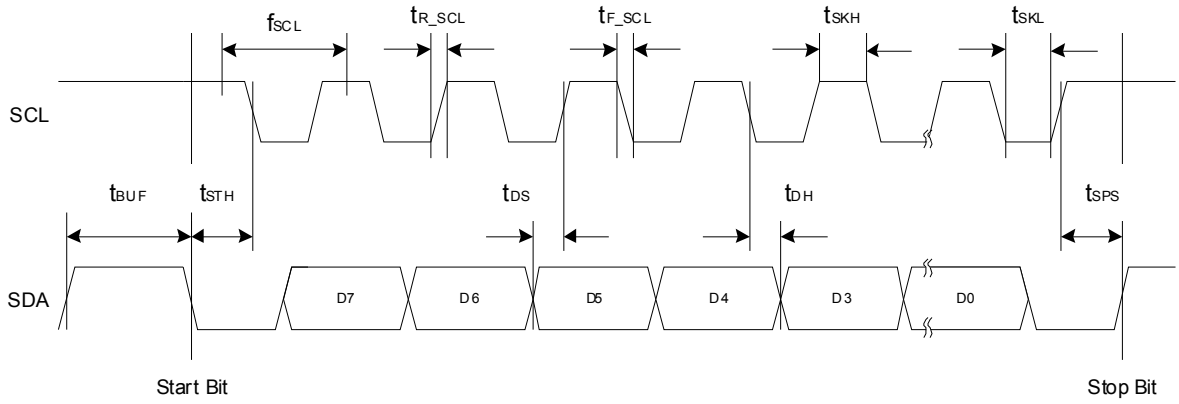

Figure 1. I^2C Timing Diagram

Table 12. Interrupt ($\overline{INT}$) Specifications

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Output low voltage	V_{OL}	$\overline{INT}$ pin driving ≤ 8.5 mA	—	—	0.6	V

Table 13. Input Voltage Reference Specifications

Description	Symbol	Test Conditions	Min	Typ	Max	Unit
Nominal VREF input			—	1.1	—	V
Reference tolerance			—	1	TBD	%
VREF loading		Input current	—	—	TBD	µA

2. PSE System-Level Diagrams

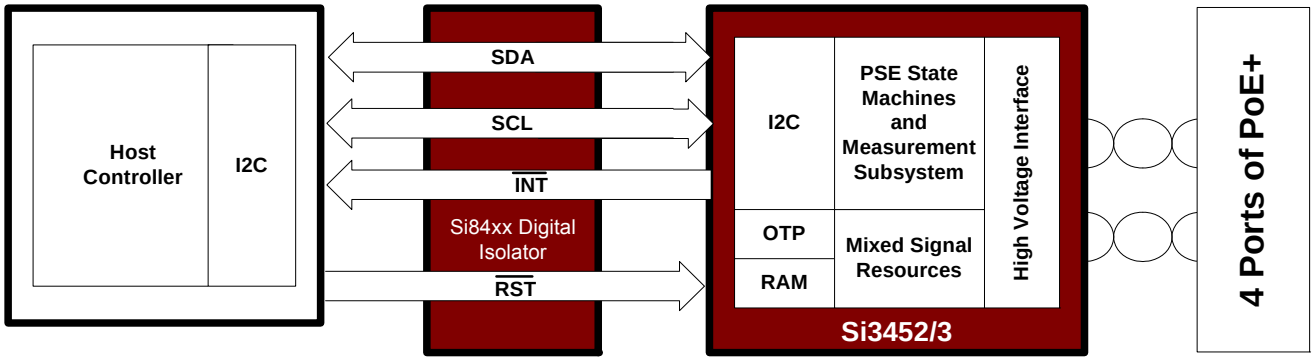

Figure 2. 4-Port System with Direct Host Connection

3. PSE Application Diagrams

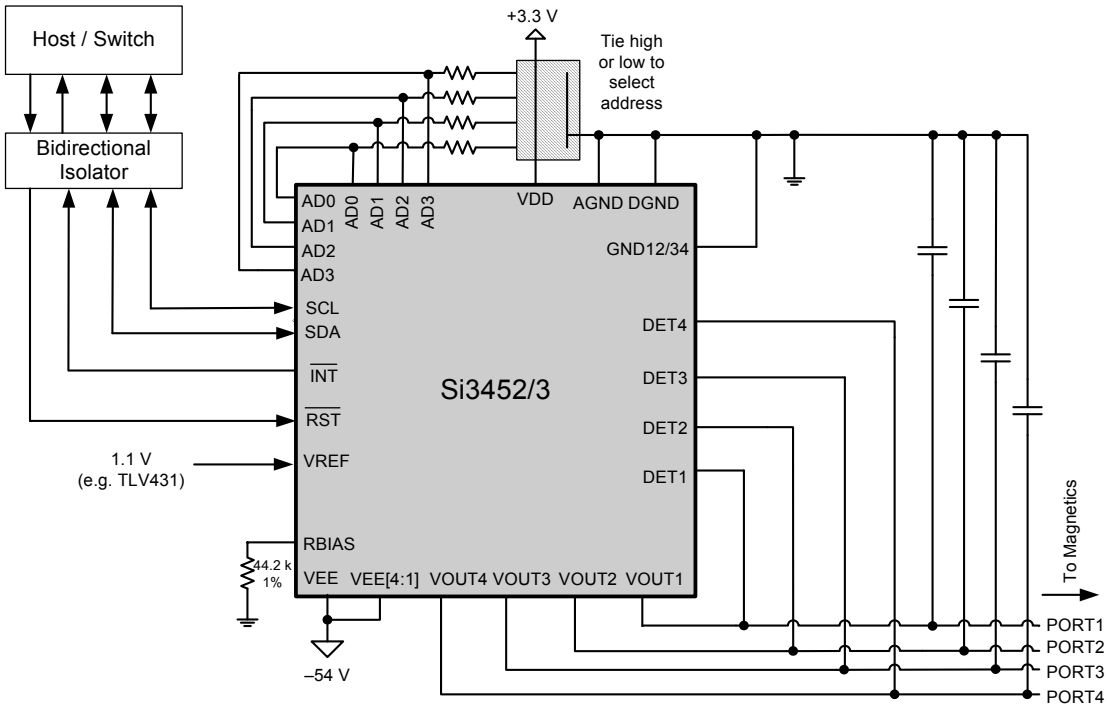

Figure 3. 4-Port Application Diagram Using DC– or dV/dt Disconnect and I²C Host Interface

4. Functional Description

Integrating four independent high voltage PSE port interfaces, the Si3452/3 high voltage port controller enables an extremely flexible solution for virtually any PoE or PoE+ PSE application. The Si3452/3 provides all of the high voltage Power over Ethernet PSE functions.

Each port of the Si3452/3 integrates all high voltage PSE controller functions needed for a quad-port PoE design, including the power MOSFET, efficient current sensing circuitry, transient voltage surge-suppressor, and multiple detect and disconnect circuits. When the DC disconnect or dV/dt disconnect sensing methods are selected, the external BOM is typically only a single filter capacitor on each high voltage port.

When a PD device has been properly detected and classified, the port is powered by a –54 V nominal supply with continuous monitoring of voltage and current for feedback to the host system.

In addition to the required IEEE features, the Si3452/3 includes many additional features:

- Per port current / voltage monitoring and measurement
- Support for 1-Event and 2-Event classification algorithms
- Start up in shutdown mode or auto mode
- Alternative A (Endpoint) or Alternative B (Midspan) detection timing

4.1. Detection

The Si3452/3 has per-port signature detection that satisfies the IEEE Std 802.3™-2005 specifications. However, by utilizing a 3-point voltage-forced detection method, the Si3452/3 yields robust recognition of valid and invalid powered device (PD) signatures, properly identifying signatures often mischaracterized by other detection techniques.

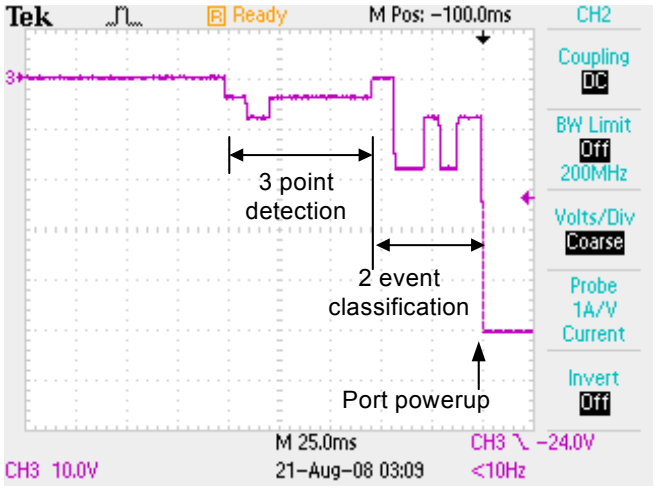

Figure 4. PSE Sequencing (3-point Detection Followed by 2-Event Classification and Powerup)—Vport relative to GND

The detection circuitry performs the function of setting the output voltage on any channel to the proper value for detection or classification, and then measuring the resulting line current.

A typical detection cycle consists of applying 4 V, then 8 V, and back to 4 V with the current limit set to 3 mA. The current is measured after appropriate settling time. For a valid PD, the detection signature must be compliant with the detection voltage both increasing and decreasing.

4.2. Classification

Following a successful PD detection, the classification phase will be automatically initiated in all operational modes. During this phase a single measurement will be made at 18 V to determine how much power the PD device will draw under maximum loads per the IEEE 802.3af and 802.3at standards. The current limit during this test mode is 60 mA nominal.

The Si3452/3 supports 1-Event and 2-Event classification. When operating in PoE (≤15.4 W) mode, 1-Event classification is used. Operation in PoE+ (>15.4 W) mode results in 2-Event classification probes. The 1-Event classification is compliant to IEEE standard 802.3-2005. 2-Event classification is compliant to draft IEEE P802.3at.

4.3. Port Turn-on and Power FETs

The FET is turned on with a gate drive that results in a very low-noise turn-on waveform with a slew rate of less than 1 V/µsec (See Figure 5).

The power FET switch on each port has been sized to have a typical ON resistance of approximately 0.3 Ω. The shunt resistor for current measurement has also been set to 0.1 Ω. Including interconnection and process variation, the total resistance to VEE for a port that is on is 0.6 Ω (max). This limits the maximum power dissipation per channel to < 250 mW, when the operating current is 600 mA, the maximum current allowed by the IEEE 802.3at PoE+ standard.

The FET has a programmable operating current limit. Each channel can be set to support output currents of 400 mA or 800 mA minimum.

In addition to the normal current limit, there is a short circuit current shutdown approximately 25% greater than the nominal current limit. If there is a transient current surge where the current ramps up faster than the programmed current limit can respond, the gate drive voltage is clamped immediately to V_{EE}. The clamp is enabled for at least 10 µs, which allows the normal current circuitry to respond.

Another important protection feature is fold back current limiting. When V_{OUT} is near V_{EE}, the current limit is at maximum. As the Vds of the driver switch increases (and V_{OUT} is closer to ground) the current limit goes to its lowest level. The amount of the fold back current is scaled proportionally with the programmed current limit.

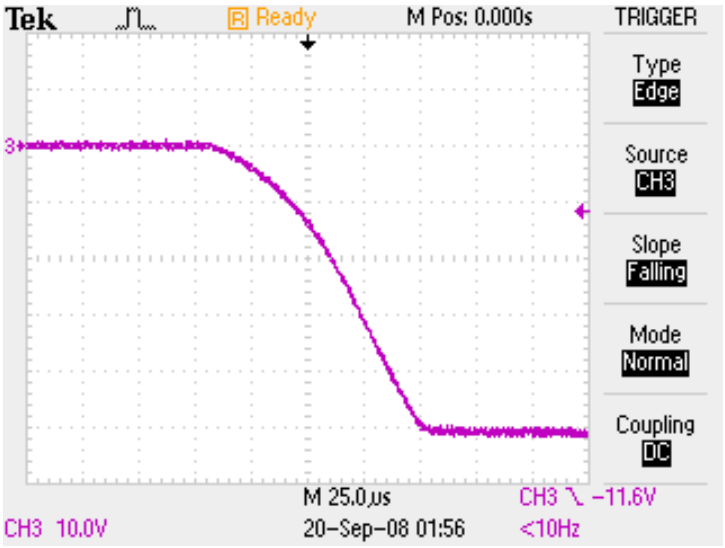

Figure 5. Turn-On Waveform—Vport relative to GND

4.4. Disconnect Detection

4.4.1. dV/dt Disconnect (Si3452)

The dV/dt™ disconnect function can be used to detect a disconnected device without using dc disconnect or ac disconnect.

In dV/dt™ disconnect mode, the FET current limit is switched to 7.5 mA. If the FET voltage increases, a load is assumed to be present and the FET current limit is automatically switched back to its pre-selected value. If, after 350 ms, the FET voltage has not increased, there is no load present, and the FET is turned off.

In addition to operating in a manner functionally distinct from DC disconnect, dV/dt disconnect requires no additional external components and fully interoperates with all powered device DC Maintain Power Signatures. For more information, see "AN399: dV/dt Disconnect and the IEEE 802.3 PoE Standard".

4.4.2. DC Disconnect (Si3453)

The port current is continuously monitored by the Si3452/3. The Si3452/3 can dynamically change the measurement scale to achieve accuracy over a wide range of currents.

As defined in the IEEE 802.3 PoE standard the PSE should disconnect if the port current is less than a nominal 7.5 mA for more than 350 ms.

4.5. Transient Voltage Surge Suppression

The Si3452/3 features robust on-chip surge protectors on each port; this is an industry first. This unique protection circuitry acts as an active device which can withstand lightning transients as well as large ESD transient events. When the port voltage exceeds its protection limit and the current reaches a triggering threshold, current is shunted from the port to the ground pins.

Internal circuitry is provided to protect the line outputs from externally coupled fault currents. These are transient currents of up to 5 A peak.

The operation of the protection circuits depends on the operating mode of the channel switch and the direction of the fault current. The clamping operation is performed on the detect pin.

The switch itself will also be protected by the current limit. If the transient lasts long enough to heat up the die, then the temperature sense circuit will shut off the switch, and all the fault current will flow through the clamp diode.

4.6. Temperature Sense

A temperature sense signal is used in conjunction with the current limit status signals from the gate drive blocks. Any channel that is generating excess heat is assumed to be operating in current limit mode, with both high voltage drop and high current.

If the port is in PoE mode, an overload will generally not result in thermal shutdown before the 60 ms I_{CUT} period. If the port is in PoE+ mode, an overload may cause the port to shut down prior to the 60 ms I_{CUT} period. In either case, the event is reported as I_{CUT}. The faster shutdown in PoE+ mode is consistent with and specifically allowed by the 802.3at draft and provides much more robust overload protection than is possible with external FETs.

In addition, there is a thermal shutdown if the package temperature exceeds 120 °C. If this threshold is reached, all output drivers are turned off and detection modes are disabled. This secondary threshold limit guards against the possibility that the overheating is not caused by a driver operating in current limit.

4.7. Port Measurement and Monitoring

VEE monitoring in conjunction with port current monitoring allows measurement of port power. Port power monitoring, dynamic power allocation via LLDP*, and port power policing allows efficient power supply sizing.

The Si3452/3 is factory calibrated and temperature compensated for the following measurements:

- Port current measurement. These measurements are auto ranged and scaled to a 16 bit number at 100 uA per bit. Port current accuracy is ±4% ± 2 mA.
- V_{EE} is measured with a scale of 64 V. The measurement is reported as a 16 bit number scaled at 1 mV per bit. V_{EE} measurement accuracy is ±4% over the valid V_{EE} range.

***Note:** LLDP = Link Layer Discovery Protocol. Refer to IEEE 802.3at (draft) and IEEE 802.1AB for more information.

4.8. SMBus/I²C Interface Details

The I²C interface is a two-wire, bi-directional serial bus. The I²C is compliant with the System Management Bus Specification (SMBus), version 1.1, and compatible with the I²C serial bus. Reads and writes to the interface by the system controller are byte oriented with the I²C interface autonomously controlling the serial transfer of the data. A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus. The I²C interface may operate as a master and/or slave, and may function on a bus with multiple masters. The I²C provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and START/STOP control and generation.

A typical I²C transaction consists of a START condition followed by an address byte (Bits7–1: 7-bit slave address; Bit0: R/W direction bit), one or more bytes of data, and a STOP condition. Each byte that is received (by a master or slave) must be acknowledged (ACK) with a low SDA during a high SCL (see Figure 6). If the receiving device does not ACK, the transmitting device will read a NACK (not acknowledge), which is a high SDA during a high SCL.

The direction bit (R/W) occupies the least-significant bit position of the address byte. The direction bit is set to logic 1 to indicate a "READ" operation and cleared to logic 0 to indicate a "WRITE" operation. All transactions are initiated by a master, with one or more addressed slave devices as the target. The master generates the START condition and then transmits the slave address and direction bit. If the transaction is a WRITE operation from the master to the slave, the master transmits the data a byte at a time waiting for an ACK from the slave at the end of each byte.

For READ operations, the slave transmits the data waiting for an ACK from the master at the end of each byte. At the end of the data transfer, the master generates a STOP condition to terminate the transaction and free the bus. Figure 6 illustrates a typical SMBus/I²C transaction.

Silicon Laboratories recommends the use of bidirectional digital isolators, such as the Si840x, to isolate the I2C communications interface between the Si3452/3 high voltage port controllers and the system host controller.

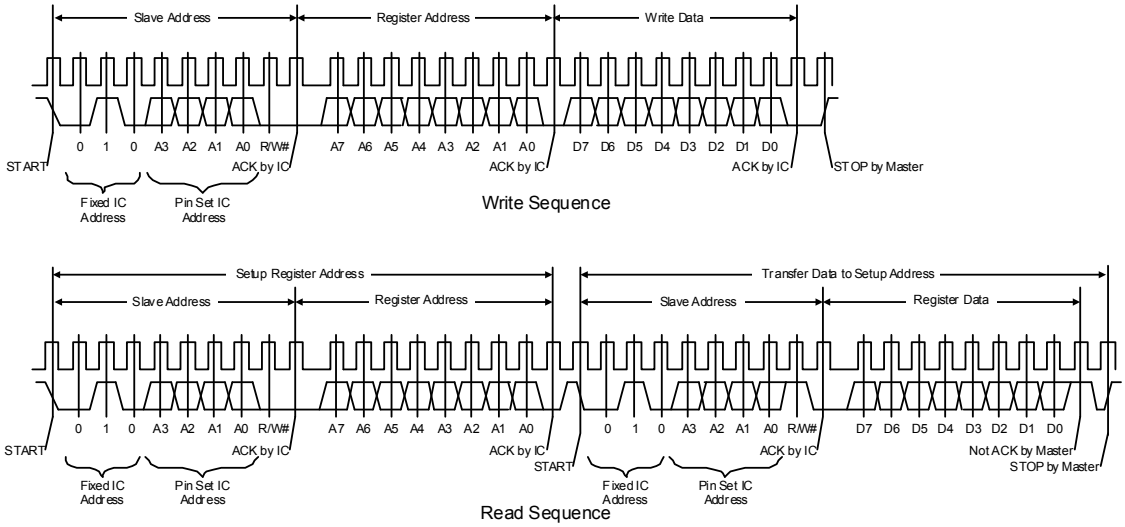

Figure 6. Typical I²C Bus Transactions

4.8.1. Address Pins

Table 14. Address Pin Assignment

Pin #	Pin Name
21	AD3
24	AD3
25	AD2
26	AD2
27	AD1
28	AD0
34	AD0
36	AD1

Pins with the same name must be externally connected and then tied high or low via a weak (10 kΩ) pull up or pull down to establish the device address at power up. The Si3452/3 powers up in either Auto mode or Shutdown mode depending on the ordering part number. For more information, see "11. Ordering Guide" on page 32.

4.8.2. Address Format

The address byte of the I^2C communication protocol has the following format:

- Bit[0] R/W bit (0 = write, 1 = read)
- Bit[1..4] the Si3452/3 address
- Bit[5..7] 010b

The device will also respond to the global address 0x30

Table 15 lists the valid device addresses:

Table 15. Address Selection

AD3	AD2	AD1	AD0	Address	Valid
0	0	0	0	0x20	Y
0	0	0	1	0x21	Y
0	0	1	0	—	N
0	0	1	1	—	N
0	1	0	0	0x24	Y
0	1	0	1	0x25	Y
0	1	1	0	—	N
0	1	1	1	—	N
1	0	0	0	0x28	Y
1	0	0	1	0x29	Y
1	0	1	0	0x2A	Y
1	0	1	1	0x2B	Y
1	1	0	0	0x2C	Y
1	1	0	1	0x2D	Y
1	1	1	0	0x2E	Y
1	1	1	1	0x2F	Y

4.8.3. ARA

For I^2C operation, the Si3452/3 provides an Alert Response Address to the master when the Slave address is 0x0C and the $\overline{INT}$ pin is asserted. When these conditions are met, this IC begins to provide its address followed by a one. During this transaction, the IC monitors its SDA pin's level to determine if the read value matches what this IC is writing on the SDA pin. If the value matches for the entire transfer, then the Si3452/3 de-asserts its $\overline{INT}$ pin. If a mismatch is detected, the Si3452/3 immediately aborts the transaction and floats its SDA pin until the IC needs to respond to another bus transaction) and continues to assert its $\overline{INT}$.

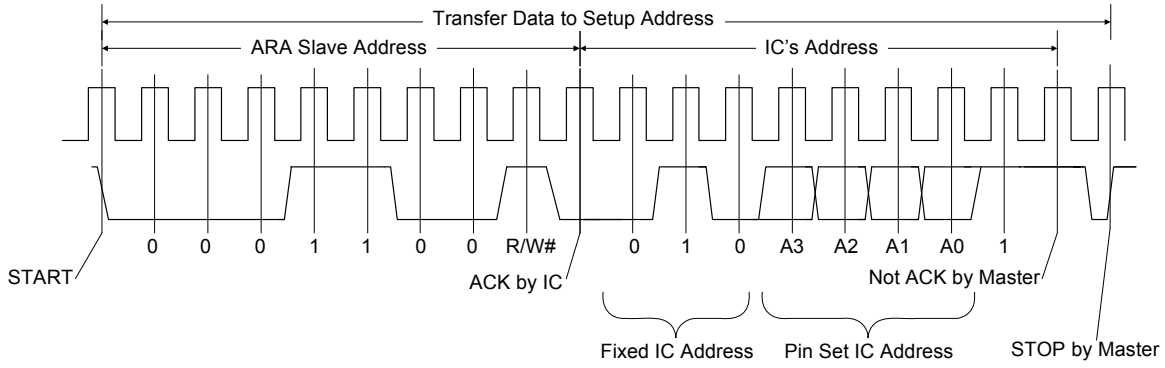

Figure 7. ARA Transaction

After the $\overline{INT}$ pin is de-asserted, it is assumed the host will read the appropriate COR read registers to clear the interrupt source. Any new interrupt source after the $\overline{INT}$ pin is cleared will not generate a new interrupt until the original interrupt source is cleared.

5. Register Interface

The registers types are described in the following sections.

5.1. Interrupt (Registers 0x00–0x01)

An interrupt ($\overline{INT}$ pin low) is generated if any bit of the Interrupt register (register 0x00) is true. The Interrupt register contains the information about which port is generating the interrupt or if the interrupt is due to a global event.

The port interrupt is generated by the port event register masked by the event mask register.

Port event = (t_{START} event AND t_{START} mask) OR (tI_{CUT} event AND tI_{CUT} mask) OR (CLASS_event AND CLASS_mask) OR (DET_EVENT AND DET_MASK) OR (Pgood_event AND Pgood_MASK) OR (Penable_event AND Penable_mask)

The device event bit of the Interrupt register is set if there is a V_{EE} or a temperature event in register 0x1D.

5.2. Port Event (Registers 0x02–0x05)

This register contains bits that become true if the event has occurred. The registers are Clear On Read (COR) so that reading these registers will clear the $\overline{INT}$ pin if the $\overline{INT}$ pin is being held low due to a port event.

"t_{START}" is an event bit indicating an overload occurred for all but 5 msec of the initial 60 msec start up time.

"tI_{CUT}" is an event bit indicating an overload condition has existed for greater than 60 msec after the first 60 msec. tI_{CUT} has a 16:1 up down counter so that if the overload is present at less than a 6.66% cycle the port will not shut down. Overload is defined as $I>I_{CUT}$ or port voltage not within 2 V of V_{EE}. The port is turned off on this event. A tI_{CUT} event is also generated if the port is shutdown due to an overload or due to the protection clamp turning on. If the port is set to auto mode it will attempt to re-power after >750 msec if there is a good detection signature.

"Rgood CLS" indicates classification has been completed. Classification is only attempted after an Rgood so if this bit is set it indicates detection gave an Rgood and classification is complete.

“DET compl“ indicates the completion of a detection cycle. Normally this bit will be masked. The DET complete bit would be used for legacy detection via modified link pulses. If the link pulse is returned indicating a PD is present then normally a detection is done and the port is powered only if the result is not a short. In some cases it may be desirable to deny power to a port where an overload has been detected until the port is unplugged. In this case, the Ropen result will be used to indicate the port has been unplugged and detection and classification can resume.

“Disconnect event“ indicates a disconnect has occurred. DC power was removed due to the dV/dt™ or DC disconnect. Overload conditions or loss of V_{EE} turns off ports but does not generate a disconnect event.

“Pgood“ indicates the port has been turned on and did not shut down during the Tstart time.

“Penable“ indicates a port has been turned on.

5.3. Port Status (Registers 0x06–0x09)

These registers specify the port status. They are read only.

“Pwr good“ indicates the port has been turned on, and the port voltage is within 2 V of V_{EE}.

“Pwr Enable“ indicates the port has been turned on.

The 3 class status bits indicate the last classification result for that port. If a classification has not been done or if the port is shutdown with no new classification result, the class status is reported as unknown.

The 3 detect status bits indicate the last detection result for that port. If a detection has not been done or if the port is shutdown with no new detection result, the detection status is reported as unknown.

5.4. Port Configuration (Registers 0x0A–0x011)

These registers indicate the port configuration. They are read/write.

The “PoE+“ bit specifies the dc current limit at either 425 mA or 850 mA nominal.

“Disconnect enable“ must be set for power to be removed if there is a disconnect. The disconnect type (based on dc disconnect or based on Silicon Laboratories proprietary dV/dt disconnect) is determined by the ordering part number.

“Port mode“ is set according to the following table.

Table 16. Port Mode Selection

Port Mode Setting B1, B0	Mode	Description
00b	Shutdown	The power is shutdown with no detection pulses. A command to manually power the port is ignored.
01b	Manual	The port can be powered by the manual power command.
10b	Semiauto	Detection is done and classification is done for Rgood but the port does not power.
11b	Auto	Detection Classification and Port powering are all automatic with no host intervention required. I_{CUT} and I_{LIM} are automatically set according to the PoE+ mode and classification result.

I_{CUT} is the nominal current level at which the port will automatically power down if I_{CUT} is exceeded for 60 msec. It can be set with 3.2 mA resolution. The accuracy of current measurement is approximately 5% so I_{CUT} is normally set 7% higher than the supported current level. I_{CUT} is automatically set based on the classification result and PoE+ mode. The automatically set I_{CUT} level is appropriate for a 44 V minimum system power supply for classes 0–3 and for a 50 V minimum power supply for PoE+ mode.

If the Si3452/3 is in the semi-auto mode, I_{CUT} will not be updated according to the classification result. This means that if it is desired to set I_{CUT} at port turn on, this should be done before the port is turned on.

Once a port is turned on, I_{CUT} can be changed dynamically. It is often un-desirable to use a low value of I_{CUT} during port turn on because inrush can trigger the I_{CUT} event. For this reason, it is normal to allow the port to turn on with the automatic I_{CUT} setting and then later change this value after port current has stabilized and also if the PD and PSE have negotiated for a different I_{CUT} value based on the PoE L2 power negotiation protocol (LLDP).

The Si3452/3 supports 2-Event classification as defined in the IEEE 802.3at draft. 2-event classification is an alternative to L2 power management where the PSE advertises it is capable of PoE powering by generating two classification pulses. 2-Event classification is only supported for auto mode. If the Si3452/3 is in auto mode and the first event classification result is class 4, the mark, second event and second mark are performed. Power is applied only if the second event is also class 4. If the second event is not class 4, the classification error is reported and the port will not power.

If the port is in manual mode, classification is done prior to turning on the port. It is not possible to turn on a port that gives classification overload or gives unequal results for 2-Event classification.

5.5. Command and Return Registers (Registers 0x12–0x1C)

The global command register enables manual port turn on or turn off, chip reset, port reset and measurement of port current and V_{EE}. It is a Write only register. See Table 23 on page 23 for a list of all available commands.

If the command results in a numerical return value, that value is stored in the measurement registers which are read only. Each of the five possible measurements results in a 2 byte return value and that value is stored in a unique register. V_{EE} is encoded in mV units so the full scale is 65.535 V and Iport is encoded in 100 µA units so the full scale is 6.5535 A.

The data for the return value is only updated after a command. This means, that the numerical value of the port current or V_{EE} voltage in the measurement register will be the value at the time the command was issued. If the port turns off due to an overload or disconnect the port current register contents will not be set to zero. If a command to read port current is issued and the port is off, the return value will be zero.

5.6. Device Status Register (0x1D)

The device event bits are listed in Table 17.

Table 17. Device Status Bits

Bit	Description
B6 - OverTemp	The Si3452/3 has per port thermal shutdown sensors as well a global thermal shutdown at a slightly higher temperature. The global thermal shutdown bit of the device event register is set if this occurs.
B5 - V_{EE} UVLO	V_{EE} UVLO. The part is put in it's reset state if V_{EE} is not in a valid range.

The Device status register is RO. The V_{EE}, UVLO, and overtemp bits reflect the device status. They are set if V_{EE} or temperature is out of range and reset if the V_{EE} or temperature is in range. Bit 6 of the Interrupt register is set if there is a change in the overtemp status (bit 6 of 0x1D), and bit 5 of the Interrupt register is set if there is a change in the V_{EE} UVLO status (bit 5 of 0x1D). Reading register 0x1D clears these bits of the Interrupt register but does not clear the device status register.

In addition, bit B0 indicates whether or not detection back off is used. For PSEs that are wired as Alternative B (power on the spare pair, typically used for midspans), the time between detection pulses is increased to slightly over two seconds to avoid interference with Alternative A (power on the data pair, typically used for endpoints). Bit B0 can be toggled using the command code 0x10.

Table 18. Si3452/3 Register Map

Address	Register Name	Type	B7	B6	B5	B4	B3	B2	B1	B0	POWER_UP
Interrupts											
0x00	Interrupt Reg 1	RO		Overtemp change	V_{EE} UVLO change		Port 4 event	Port 3 event	Port 2 event	Port 1 event	0x00
0x01	Interrupt Mask 1	RW	Device status mask	t_{START} mask	tI_{CUT} mask	Rgood CLS mask	DET compl mask	Disconnect mask	PwrGood mask	PwrEn mask	0x85
Port Events											
0x02	Port 1 Events	COR		t_{START} Event	tI_{CUT} Event	Rgood CLS	DET compl	Disconnect Ev	PwrGood Change	PwrEn Change	0x00
0x03	Port 2 Events	COR		t_{START} Event	tI_{CUT} Event	Rgood CLS	DET compl	Disconnect Ev	PwrGood Change	PwrEn Change	0x00
0x04	Port 3 Events	COR		t_{START} Event	tI_{CUT} Event	Rgood CLS	DET compl	Disconnect Ev	PwrGood Change	PwrEn Change	0x00
0x05	Port 4 Events	COR		t_{START} Event	tI_{CUT} Event	Rgood CLS	DET compl	Disconnect Ev	PwrGood Change	PwrEn Change	0x00
Status											
0x06	Port 1 Status	RO	PwrGood Status	PwrEnable Status	CLS Stat B2	CLS Stat B1	CLS Stat B0	DET Stat B2	DET Stat B1	DET Stat B0	0x00
0x07	Port 2 Status	RO	PwrGood Status	PwrEnable Status	CLS Stat B2	CLS Stat B1	CLS Stat B0	DET Stat B2	DET Stat B1	DET Stat B0	0x00
0x08	Port 3 Status	RO	PwrGood Status	PwrEnable Status	CLS Stat B2	CLS Stat B1	CLS Stat B0	DET Stat B2	DET Stat B1	DET Stat B0	0x00
0x09	Port 4 Status	RO	PwrGood Status	PwrEnable Status	CLS Stat B2	CLS Stat B1	CLS Stat B0	DET Stat B2	DET Stat B1	DET Stat B0	0x00
Configuration											
0x0A	Port 1 Config	RW					PoE+	Discon En	Port Mode B1	Port Mode B0	00000100b
0x0B	Port 2 Config	RW					PoE+	Discon En	Port Mode B1	Port Mode B0	00000100b
0x0C	Port 3 Config	RW					PoE+	Discon En	Port Mode B1	Port Mode B0	00000100b
0x0D	Port 4 Config	RW					PoE+	Discon En	Port Mode B1	Port Mode B0	00000100b
0x0E	Port 1 I_{CUT}	RW	B7	B6	B5	B4	B3	B2	B1	B0	0x75
0x0F	Port 2 I_{CUT}	RW	B7	B6	B5	B4	B3	B2	B1	B0	0x75
0x10	Port 3 I_{CUT}	RW	B7	B6	B5	B4	B3	B2	B1	B0	0x75
0x11	Port 4 I_{CUT}	RW	B7	B6	B5	B4	B3	B2	B1	B0	0x75

Table 18. Si3452/3 Register Map (Continued)

Address	Register Name	Type	B7	B6	B5	B4	B3	B2	B1	B0	POWER_UP
Global Device											
0x12	Command Register	WO				CMD Code B2	CMD Code B1	CMD Code B0	CMD Param B1	CMD Param B0	0x00
0x13	V_{EE} MSB	RO									0x00
0x14	V_{EE} LSB	RO									0x00
0x15	Current P1 MSB	RO									0x00
0x16	Current P1 LSB	RO									0x00
0x17	Current P2 MSB	RO									0x00
0x18	Current P2 LSB	RO									0x00
0x19	Current P3 MSB	RO									0x00
0x1A	Current P3 LSB	RO									0x00
0x1B	Current P4 MSB	RO									0x00
0x1C	Current P4 LSB	RO									0x00
0x1D	Device Status	RO		OverTemp	V_{EE} UVLO					Alternative B Timing	0x00
Revision											
0x60	Hardware Revision	RO									
0x61	Firmware Revision	RO									
0x62	Firmware Revision	RO									
0x63	Firmware Revision	RO									

Table 19. Si3452/3 Detect Encoding

Value	Condition
000b	Unknown
001b	Short
010b	Reserved
011b	RLOW
100b	Good
101b	Rhigh
110b	Ropen
111b	Reserved

Table 20. Si3452/3 Class Encoding

Value	Condition
000b	Unknown
001b	Class 1
010b	Class 2
011b	Class 3
100b	Class 4
101b	Probes Not Equal
110b	Class 0
111b	Class Overload

Table 21. Si3452/3 Port Mode Encoding

Value	Condition
00b	Shutdown
01b	Manual
10b	Semiauto
11b	Auto

Table 22. Si3452/3 Port Configuration

PoE+ bit	Class	Auto Mode Setting of I_{CUT} Register	I_{CUT} Nominal	Ilim Nominal*
0 or 1 don't care	1	0x1E	97 mA	425 mA
0 or 1 don't care	2	0x35	170 mA	425 mA
0 or 1 don't care	0/3	0x75	375 mA	425 mA
0	4	0x75	375 mA	425 mA
1	4	0xC9	640 mA	850 mA
***Note:** During initial port turn-on (T_{START} time of 60 msec), the current limit is set to 425 mA, even in PoE+ mode.				

Table 23. Si3452/3 Command Codes

Command	Command Codes	CMD Register	[B4..B2]	[B1..B0] Command Parameter	2 Byte Return Value
Power on port	0x01	0x04 | port no	001b	2 bit port number	
Power off port	0x02	0x08 | port no	010b	2 bit port number	
Reset port	0x03	0x0C | port no	011b	2 bit port number	
Toggle detection back-off timing*	0x04	0x10	100b	NA	
Reset chip	0x05	0x14	101b	NA	
Get V_{EE}	0x06	0x18	110b	NA	V_{EE} in mV units
Read port current	0x07	0x1C | port no	111b	2 bit port number	Port current in 100 µA units
***Note:** This command toggles bit 0 or Register 0x10. When bit zero is set, the detection back-off of 2 seconds is implemented (alternative B or "midspan" mode).					

6. Operational Notes

6.1. Port Turn On

Ports are normally powered by either putting the Si3452 in the auto mode and allowing the Si3452 to control the powering sequence, or by putting the Si3452 in the manual mode and issuing a turn-on command.

If the port is turned on by putting it in auto mode, the Si3452/3 will take care of all specified timing, and it will take care of the two-event classification if the first event result is class 4 and PoE+ mode is enabled. However, if automatic mode operation is not desired after port turn on, the port should be set to semi-auto or manual mode once it has powered.

If the port is turned on by putting it in manual mode, the normal sequence is to start with the port in semi auto mode and interrupt on a classification complete, which indicates that there is a valid PD signature and a classification result is available. Based on the classification result, the host can make a decision to apply power or not. The IEEE standard requires that a port be powered within 400 msec of a valid detect complete. It is also desirable to power the port prior to the start of the next detection pulse, which can occur in as little as 300 msec. Therefore, it is recommended that ports be powered in under 250 msec from the class complete interrupt when using the manual mode turn on command.

Using manual mode turn-on, detection is not done prior to port turn on, but classification is always performed just prior to port turn on. A port that presents an invalid classification signature will not be turned on. 2-event classification is performed if the first event result is class 4 and the port is enabled for PoE+ mode. The port is not turned on if the classification result is overload or if PoE+ mode is enabled and the second event result is not class 4. The manual mod classification step does not generate a classification complete flag because it is assumed that the classification was already done in semi-auto mode, and the host has already made the decision to grant power.

If a port turn-on command is issued in semi-auto or auto mode, the port will power, but this is not desireable because IEEE-compliant timing is not assured.

6.2. Changing the Interrupt Mask

The INT register and $\overline{\text{INT}}$ pin are always synchronized. However, there can be up to a 5 msec delay between an event that causes or clears an interrupt and the update of the register and pin.

Thus, if the INT mask register is changed to clear an interrupt or to block an interrupt source, there can be up to a 5 msec delay between the change of the INT mask register and the resultant change in the INT register and $\overline{\text{INT}}$ pin.

Generally, use of the mask register to clear interrupts is not recommended; it is better to clear an interrupt by reading the appropriate COR register.

7. PCB Layout Guidelines

Due to the high current of up to 800 mA per port, the following board layout guidelines apply. In addition, contact Silicon Laboratories. for access to complete PSE reference design databases including recommended layouts.

The VEE1, VEE2, VEE3 and VEE4 pins can carry up to 800 mA and are connected to a V_{EE} bus. The V_{EE} bus for a 24 port PCB layout could thus carry as much as 20 A current. With 2 oz. copper on an outer layer, a bus of 0.4 inches is needed. For an inner layer, this increases to 1 inch wide bus. Use of large or multiple vias is required for properly supporting the 800 mA per channel operating current. The VEE pin does not carry high current and can be connected directly to the bus as well. The best practice is to devote an entire inner layer for V_{EE} power routing.

Similarly, GND1/2 and GND3/4 pins can carry up to 1.6 A per pin and the GND return bus should be at least as wide as the V_{EE} bus as above. The best practice is to devote an entire inner layer for ground power routing. The ground power plane does not generally have a high frequency content (other than external faults) so it is generally acceptable to use the ground power plane as a ground signal plane and tie AGND and GND12, GND34 to this plane as well.

The VOUTn pins carry up to 800 mA dc and up to 5 A in faults, so a 20 mil trace with wide or multiple vias are also recommended. The VDETn pins also carry fault current so this pin connection to VOUTn needs to use 20 mil traces and wide or multiple vias where needed.

The VDD currents are not large so it is acceptable to route the VDD nodes on one of the outer layers.

If care is taken to avoid disruption of the high current paths, VDD can be globally routed on one of the power planes and then locally routed on an inner or outer layer.

To avoid coupling between surge events and logic signals, it is recommended that VOUTn traces be routed on the opposite side as the I^2C interface pins.

The thermal pad of the Si3452/3 is connected to VEE. At full IEEE 802.3at current of 600 mA on each port the dissipation of the Si3452/3 is up to 1.2 W; so, multiple vias are required to conduct the heat from the thermal pad to the VEE plane. As many as 36 small vias provide the best thermal conduction.

8. Pin Descriptions

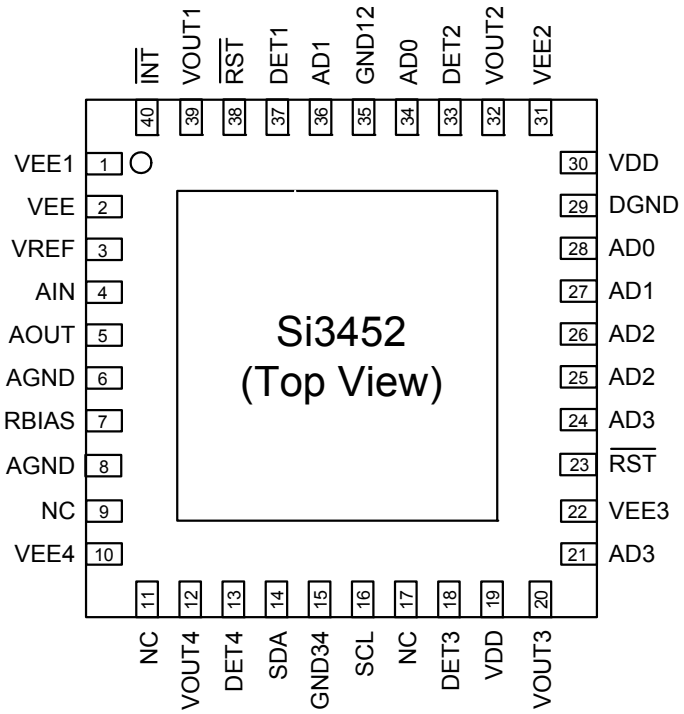

Table 24. Si3452/3 Pin Descriptions

Pin #	Name	Type	Description
1	VEE1	Supply	Driver 1 VEE supply. Short to VEE, VEE2/3/4.
2	VEE	Supply	Global PoE (–48 V nom.) or PoE+ (–54 V nom.) supply. Short to VEE1/2/3/4.
3	VREF	Analog input	1.1 V nom. voltage reference from reference generator (for example, TLV431 or power management unit).
4	AIN	Analog input	Measurement data converter input. Short to AOUT.
5	AOUT	Analog output	Measurement multiplexer subsystem output. Short to AIN.
6	AGND	Ground	Analog ground reference. Short to AGND pin 8, GND12/34, DGND.
7	RBIAS	Analog input	External 44.2 kΩ (±1%) resistor to ground sets internal bias currents.
8	AGND	Ground	Analog ground reference. Short to AGND pin 6, GND12/34, DGND.
9	NC	No connect	Do not connect (float).
10	VEE4	Supply	Driver 4 VEE supply. Short to VEE, VEE1/2/3.
11	NC	No connect	Do not connect (float).
12	VOUT4	Analog I/O	Port 4 power FET switch output. When on, provides a low impedance path to VEE4.
13	DET4	Analog I/O	Connection for port 4 detection, classification, and transient surge protection. This pin is tied to VOUT4.

Table 24. Si3452/3 Pin Descriptions (Continued)

Pin #	Name	Type	Description
14	SDA	Digital I/O	I^2C data pin
15	GND34	Ground	Ground supply for protection clamps. Short to AGND, GND12, DGND.
16	SCL	Digital I/O	I^2C clock pin
17	NC	No connect	Do not connect (float).
18	DET3	Analog I/O	Connection for port 3 detection and classification. See DET4 for detailed description.
19	VDD	Supply	+3.3V (±10%) isolated supply. Short to VDD pin 30.
20	VOUT3	Analog I/O	Port 3 power FET switch output. When on, provides a low impedance path to VEE3.
21	AD3	Digital I/O	Chip address bit 3 pin, read after reset. Address set with defined resistor dividers. Pin also used for internal communications. Short to AD3 pin 24.
22	VEE3	Supply	Driver 3 VEE supply. Short to VEE, VEE1/2/4.
23	$\overline{\text{RST}}$	Digital input	Active low digital reset. Short to $\overline{\text{RST}}$ pin 38.
24	AD3	Digital I/O	Chip address bit 3 pin, read after reset. Address set with a 10 kΩ pull-up or pull-down resistor. Also used for internal communications. Short to AD3 pin 21.
25	AD2	Digital I/O	Chip address bit 2 pin, read after reset. Address set with a 10 kΩ pull-up or pull-down resistor. Also used for internal communications. Short to AD2 pin 26.
26	AD2	Digital I/O	Chip address bit 2 pin, read after reset. Address set with a 10 kΩ pull-up or pull-down resistor. Also used for internal communications. Short to AD2 pin 25.
27	AD1	Digital I/O	Chip address bit 1 pin, read after reset. Address set with a 10 kΩ pull-up or pull-down resistor. Also used for internal communications. Short to AD1 pin 36.
28	AD0	Digital I/O	Chip address bit 0 pin, read after reset. Address set with a 10 kΩ pull-up or pull-down resistor. Also used for internal communications. Short to AD0 pin 34.
29	DGND	Ground	Digital ground reference. Short to AGND, GND12/34
30	VDD	Supply	+3.3 V isolated supply. Short to VDD pin 19.
31	VEE2	Supply	Driver 2 VEE supply. Short to VEE, VEE1/3/4.
32	VOUT2	Analog I/O	Port 2 power FET switch output. When on, provides a low impedance path to VEE2.
33	DET2	Analog I/O	Connection for port 2 detection and classification. See DET4 for detailed description.
34	AD0	Digital I/O	Chip address bit 0 pin. See description for- and short to AD0 pin 28.
35	GND12	Ground	Ground supply for protection clamps. Short to AGND, GND34, DGND.
36	AD1	Digital I/O	Chip address bit 1 pin. See description for- and short to AD1 pin 27.
37	DET1	Analog I/O	Connection for port 1 detection and classification. See DET4 for detailed description.
38	$\overline{\text{RST}}$	Digital input	Active low digital reset. Short to $\overline{\text{RST}}$ pin 23.

Table 24. Si3452/3 Pin Descriptions (Continued)

Pin #	Name	Type	Description
39	VOUT1	Analog I/O	Port 1 power FET switch output. When on, provides a low impedance path to VEE1.
40	$\overline{\text{INT}}$	Digital output	Active low interrupt output pin.

9. Package Outline: 40-Pin QFN

The Si3452/3 is packaged in an industry-standard, RoHS compliant 6 x 6 mm^2, 40-pin QFN package.

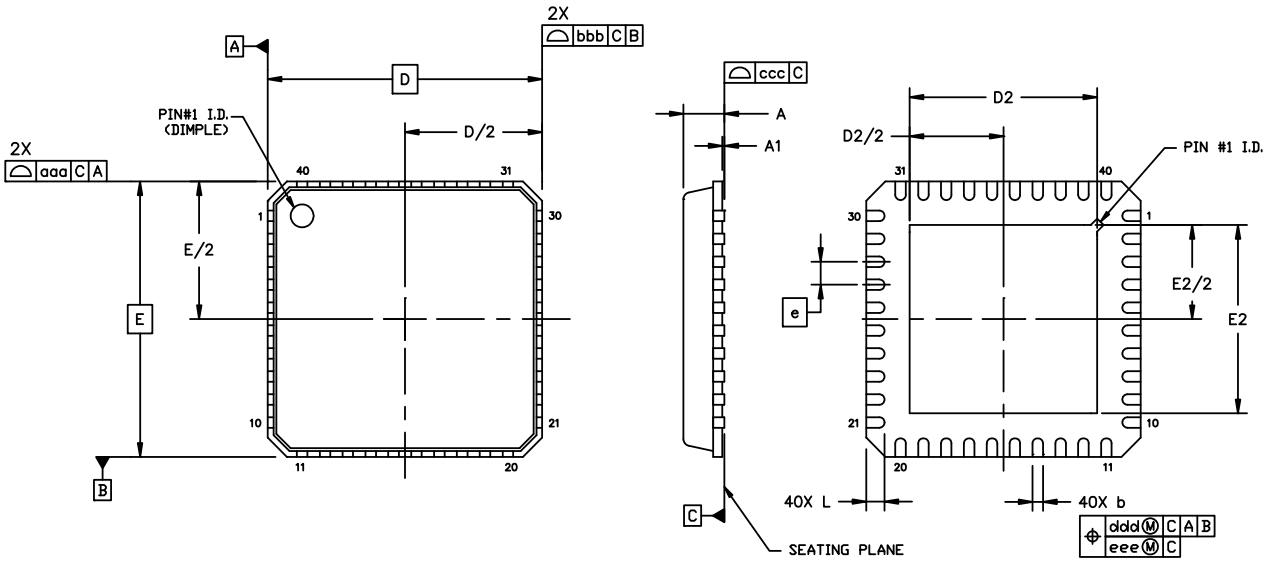

Figure 8. 40-Pin QFN Mechanical Diagram

Table 25. Package Diagram Dimensions

Dimension	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D		6.00 BSC.	
D2	3.95	4.10	4.25
e		0.50 BSC.	
E		6.00 BSC.	
E2	3.95	4.10	4.25
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.10	
eee		0.05	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, Variation VJJD-2
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

10. Recommended PCB Footprint

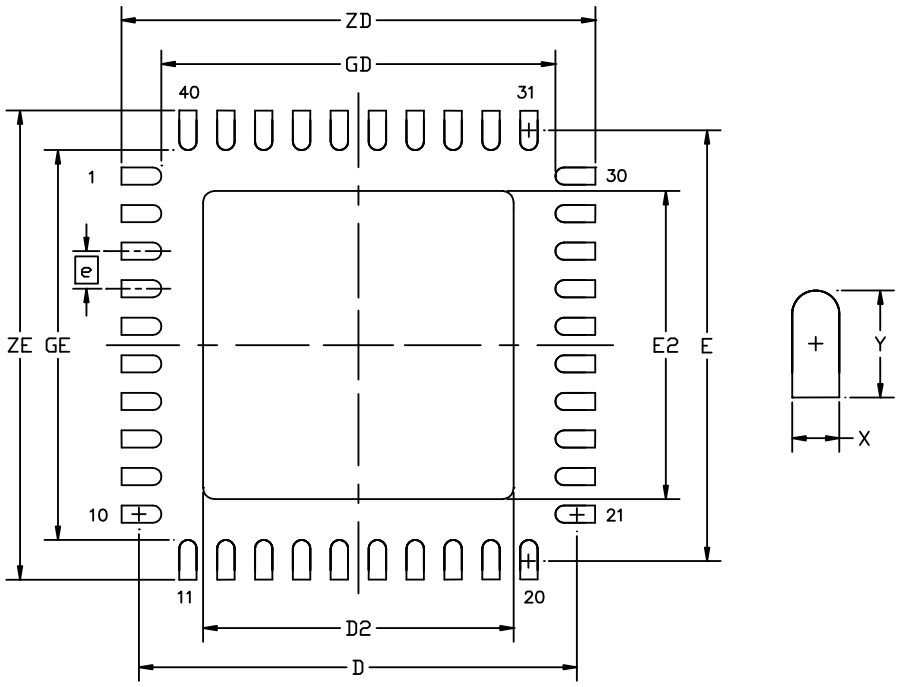

Figure 9. PCB Land Pattern

Table 26. PCB Land Pattern Dimensions

Dimension	Min	Max
e	0.50 BSC	
E	5.42 REF	
D	5.42 REF	
E2	4.00	4.20
D2	4.00	4.20
GE	4.53	—
GD	4.53	—
X	—	0.28
Y	0.89 REF	
ZE	—	6.31

Table 26. PCB Land Pattern Dimensions (Continued)

Dimension	Min	Max
ZD	—	6.31

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on IPC-SM-782 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
9. A 4x4 array of 0.80 mm square openings on 1.05 mm pitch should be used for the center ground pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. The recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

11. Ordering Guide

Ordering Part Number[1]	Detect Timing	Power Supported[2]	Powerup Mode[3]	Disconnect Method	Firmware Revision	Package[4] and Temp. Range
Si3452-B01-GM	Configurable	Configurable	Shutdown	dV/dt™ disconnect	01	40-pin 6mm × 6mm QFN. –10 to 85 °C ambient operating temperature.
Si3452A-B01-GM	Endpoint	PoE (15.4W)	Auto			
Si3452B-B01-GM	Midspan					
Si3452C-B01-GM	Endpoint	PoE+ (30W)				
Si3452D-B01-GM	Midspan					
Si3453-B01-GM	Configurable	Configurable	Shutdown	DC disconnect		
Si3453A-B01-GM	Endpoint	PoE (15.4W)	Auto			
Si3453B-B01-GM	Midspan					
Si3453C-B01-GM	Endpoint	PoE+ (30W)				
Si3453D-B01-GM	Midspan					

Notes:
1. Add “R” to the end of the ordering part number to denote tape-and-reel option. E.g., Si3452-B01-GMR.
2. The maximum PoE or PoE+ power applies to all ports on Auto mode devices.
3. Devices powering up into shutdown mode are intended for use with a system host that provides run-time configuration or power-management.
4. All packages are RoHS and Pb-free.

11.1. Evaluation Kits and Reference Designs

Part Number	Populated Device	Description	Related Ethernet Chipset	Type
Si3452MS8-KIT	Si3452-B01	PoE+ 8-port Midspan PSE evaluation kit. Includes PC-control interface, PD loads, cables.	None	Evaluation Kit
Si3452V1-EVB	Si3452-B01	PoE/PoE+ 24-port daughtercard	Vitesse	Reference Design
Si3452V2-EVB	Si3452-B01	PoE+ 8-port Gb-Ethernet switch	Vitesse SparX-G8e	Reference Design
Si3452M1-EVB	Si3452-B01	PoE/PoE+ 24-port daughtercard	Marvell	Reference Design

12. Device Marking Diagram

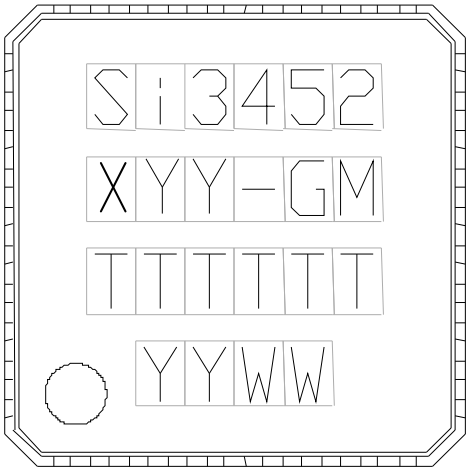

Figure 10. Device Marking Diagram

Table 27. Device Marking Table

Line #	Text Value	Description
1	Si3452	Base part number. This is not the “Ordering Part Number” since it does not contain a specific revision. Refer to "11. Ordering Guide" on page 32. for complete ordering information.
2	XYY	X = Device revision. YY = Firmware revision.
2	GM	Device type. GM = Industrial temp range; RoHS and lead-free device.
3	TTTTTT	Trace code – assigned by the assembly subcontractor.
4	O	Pin 1 identifier.
	YY	Assembly year
	WW	Assembly week.

DOCUMENT CHANGE LIST

Revision 0.4 to Revision 0.41

- VEE UVLO only. Due to the protection clamp, OVLO is not supported.
- Updated thermal information.
- Removed support for pin-selectable auto mode powerup.
- Changed device status to device event flags in Interrupt register.
- Si3452 is dv/dt™ disconnect, and Si3457 is DC disconnect.
- Added "6. Operational Notes" on page 24.
- Updated "11. Ordering Guide" on page 32.
- Added "11.1. Evaluation Kits and Reference Designs" on page 32.

Revision 0.41 to Revision 0.42

- Updated Vdd typical current.
- Updated logical levels.
- Clarified port turn on commands
- Made reset timing “TBD”. The timing for samples is approximately 50 msec. There is an objective to improve this, but the final reset time has not yet been established.

NOTES:

CONTACT INFORMATION

Silicon Laboratories Inc.

400 West Cesar Chavez
Austin, TX 78701
Tel: 1+(512) 416-8500
Fax: 1+(512) 416-9669
Toll Free: 1+(877) 444-3032

Email:PoEinfo@silabs.com
Internet: www.silabs.com