

Introduction

L5963 is a multichannel voltage regulator available in three different packages: PowerSSO-36 slug-up, PowerSSO-36 slug-down and VQFPN-48.

This document describes how to use L5963 application boards in PowerSSO-36 slug-down and VQFPN-48 packages, in order to check device's performance.

Please refer to the datasheet for a description of L5963 and its electrical characteristics (see [Section Appendix A: References](#)).

Figure 1. L5963 evaluation board

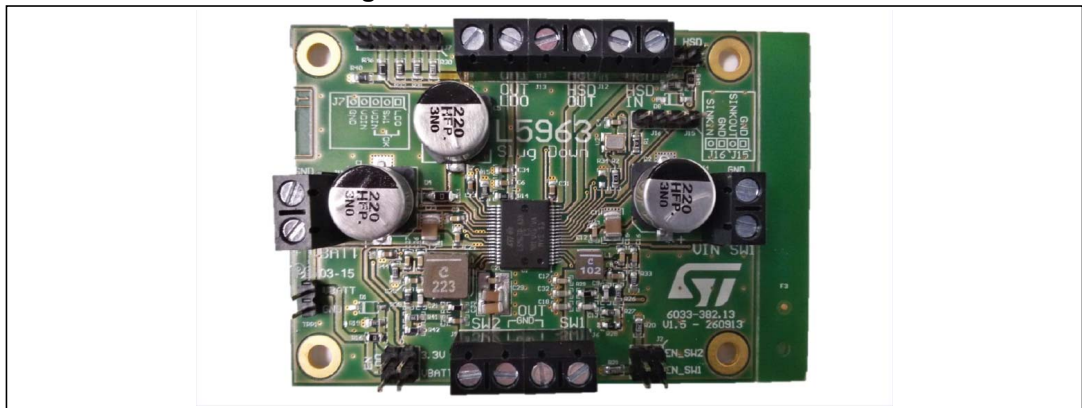
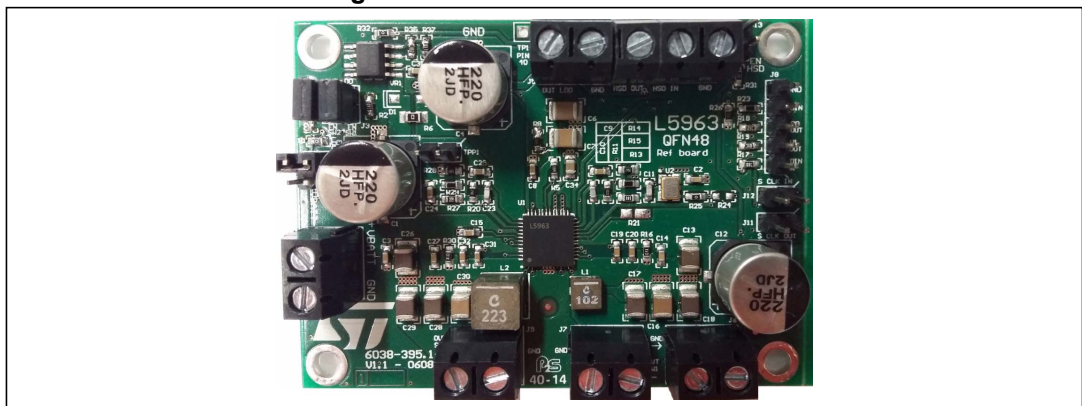


Figure 2. L5963Q evaluation board



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1 Board description

The demo boards are evaluation tools for L5963. L5963 embeds one LDO, two switching DC-DC's and one HSD (High Side Driver). For further details on the device please refer to the datasheet (see [Section Appendix A: References](#)).

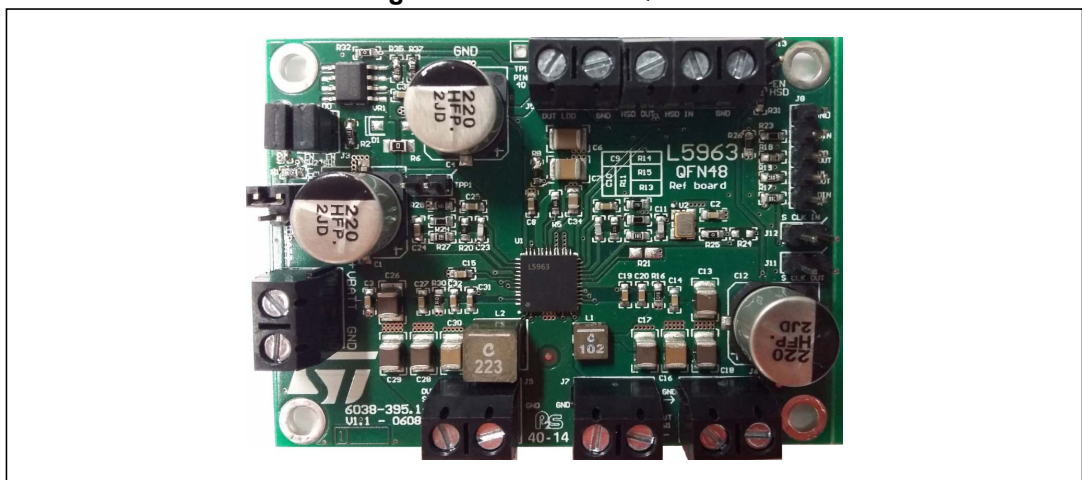
Connectors available on the board:

- **VBATT:** it is used to supply **VBATT** pin, **VINLDO** pin, and **VINSW2** pin. It is possible to apply an input voltage from 3.5 V to 26 V.
- **VINSW1:** this connector supplies **VINSW1** pin. It is possible to apply an input voltage from 3.5 V to 26 V.
- **OUTSW1:** this is the output of DC-DC1.
- **OUTSW2:** this is the output of DC-DC2.
- **OUTLDO:** this connector is the output of the LDO regulator.
- **HSDIN:** it is the input of the high-side driver.
- **HSDOUT:** it is the output of the high-side driver.

Figure 3. L5963 PCB PowerSSO-36



Figure 4. L5963 PCB QFN-48



2 Board connectors and jumper scheme

For standard operation, please make sure that jumpers are mounted in the correct position, as shown in the following pictures, and proper voltage supplies are provided.

Figure 5. L5963 PCB PowerSSO-36 jumper connections

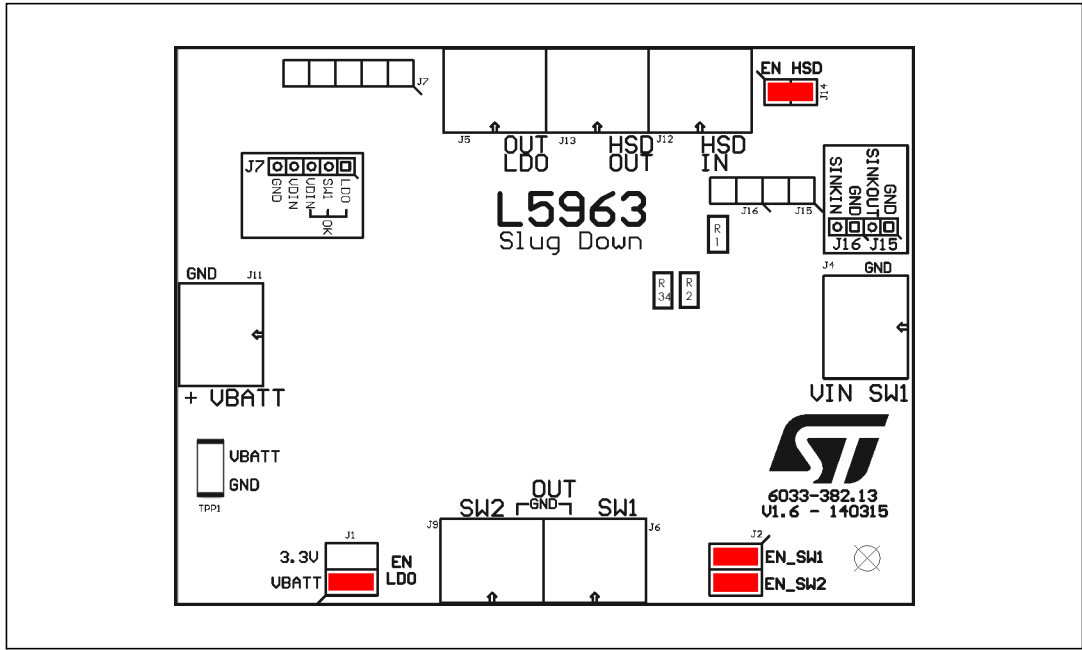
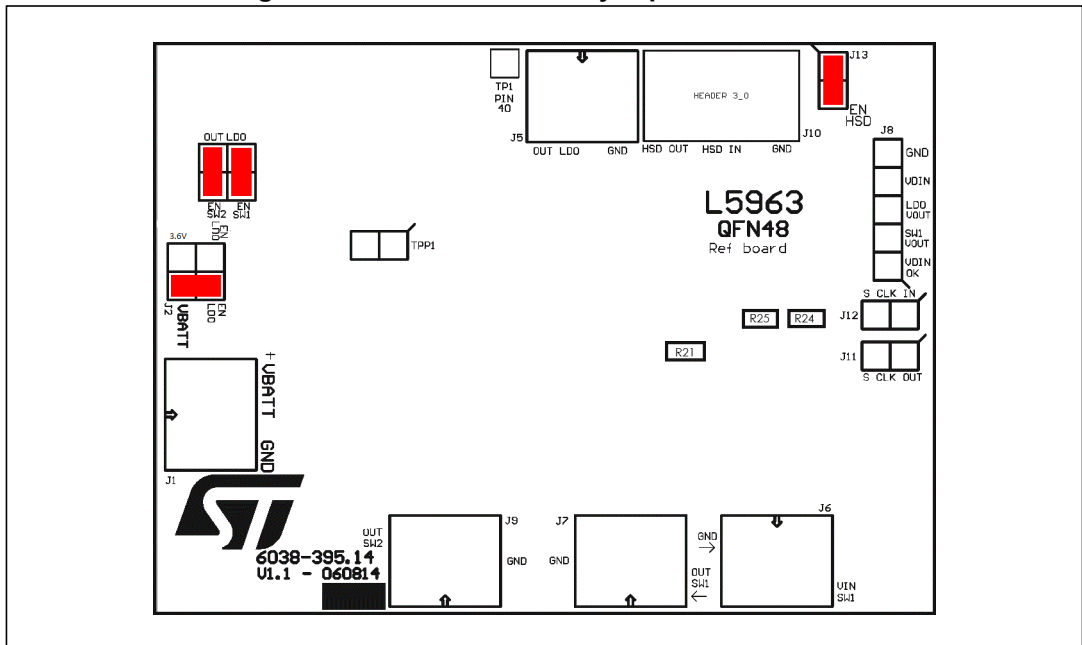


Figure 6. L5963 PCB QFN-48 jumper connections



3 Board operation

A supply voltage (battery voltage or equivalent) on **VBATT** connector is needed to operate on the board.

A test point connector, TPP1, is present on both PCB's to check the supply voltage.

3.1 LDO

The supply voltage for the LDO regulator is provided by the **VBATT** connector.

The output voltage is also present on **UTLDO** connector (max 50 mA in stand-by mode and 250 mA in normal mode).

3.1.1 How to enable the output

To enable the LDO in the PowerSSO-36 board:

- Place a jumper between "EN LDO" and "VBATT" pins of J1 to enable the LDO in stby mode (see L5963 datasheet).
- Place a jumper between "EN LDO" and "3.3 V" pins of J1 to enable the LDO in normal mode (see L5963 datasheet).

To enable the LDO in the VQFPN-48 board:

- Place a jumper between "EN LDO" and "VBATT" pins of J2 if you want to enable the LDO in stby mode (see L5963 datasheet).
- Place a jumper between pins "EN LDO" and "3.6 V" pins of J2 if you want to enable the LDO in normal mode (see L5963 datasheet).

3.2 SW1

The supply voltage for the DC-DC1 regulator is provided by the **VINSW1** connector.

The output voltage is also present on **OUTSW1** connector.

3.2.1 How to enable the output

To enable the DC-DC1 in PowerSSO-36 board:

- Place a jumper between "EN" and "SW1" pins.

Note: There's a serigraphy mistake on demo-boards till version 1.5: here you should put a jumper between pins "EN" and "SW2" to enable DC-DC1

To enable the SW1 in VQFPN-48 board:

- Place a jumper between "EN" and "SW1" pins.

3.3 SW2

The supply voltage for the DC-DC2 regulator is provided by the **VBATT** connector.

The output voltage is also present on **OUTSW2** connector.

3.3.1 How to enable the output

To enable the DC-DC2 in PowerSSO-36 board:

- Place a jumper between "EN" and "SW2" pins.

Note: There's a serigraphy mistake on demo-boards till version 1.5: here you should put a jumper between pins "EN" and "SW1" to enable DC-DC2

To enable the SW1 in VQFPN-48 board:

- Place a jumper between "EN" and "SW2" pins.

3.4 High-side driver

The HSD input is accessible on the **HSDIN** connector, while the output is accessible on the **HSDOUT** connector.

3.4.1 How to enable the output

To enable the HSD, place a jumper between pins "EN" and "HSD" on connector J14 for the PowerSSO-36 board, J13 for the VQFPN-48 board.

3.4.2 Change switching frequency

By default, in these demo boards DC-DC1 operates at 2 MHz and DC-DC2 at 250 kHz. The frequency of 2MHz is provided by an oscillator on the board.

To change the working frequency in PowerSSO-36 board:

- Invert resistors R1 and R2.
- Supply a signal with a frequency up to 2Mhz on SYNCIN pin, connector J16.
- The switching frequency divider can be changed acting on the dimension of R34, according to [Table 1](#).

To change the working frequency in VQFPN-48 board:

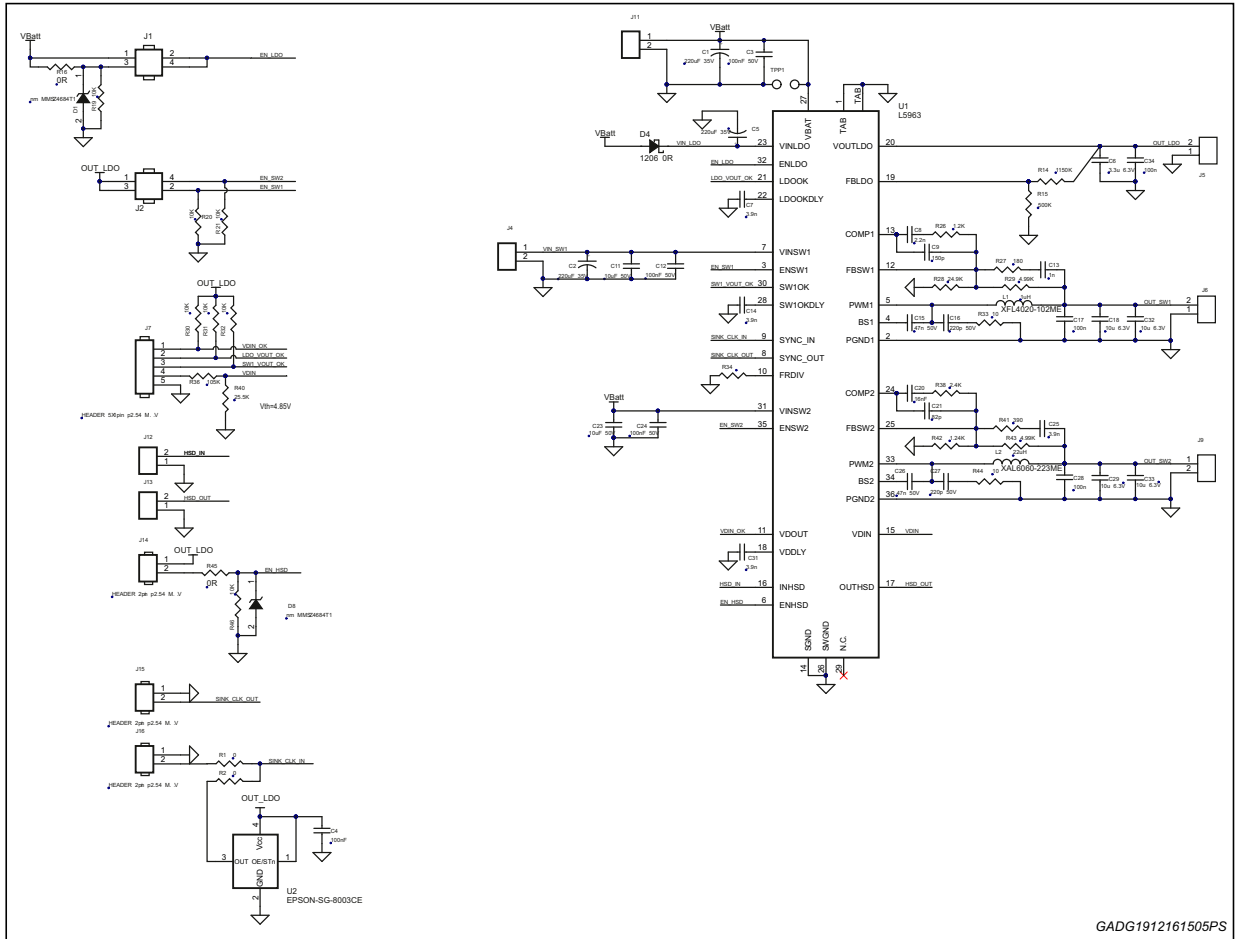
- Invert resistors R24 and R25.
- Supply a signal with a frequency up to 2Mhz on SYNCIN pin, connector J12.
- The switching frequency divider can be changed acting on the dimension of R21, according to [Table 1](#).

Table 1. Switching frequency

Fsw	R34/R21
Fsw2 = Fsw1	0 to 30 K
Fsw2 = 1/2 Fsw1	40 K to 50 K
Fsw2 = 1/4 Fsw1	85 K to 105 K
Fsw2 = 1/8 Fsw1	130 K to ∞

4 PowerSSO-36 schematic

Figure 7. PowerSSO-36 package schematic



6 Information on board use

This evaluation board/kit is intended to be used for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and it is not considered by ST Microelectronics (ST) to be a finished end product fit for general consumer use. People handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing- and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore they may not meet the technical requirements of these directives or other related directives.

Appendix A References

Dual monolithic switching regulator with LDO and HSD (Datasheet DocID028553).

Revision history

Table 2. Document revision history

Date	Revision	Changes
06-Nov-2015	1	Initial release.
10-Jan-2017	2	Updated entire document.
22-Feb-2017	3	Updated <i>Section 3: Board operation</i> .

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