VBUS OVP with a PTVS Diode

General Description

The RT9746 is an overvoltage protection devices feature a low 35mΩ (typ) RON internal FET with PTVS diode. The PTVS also protects the devices from surges up to 100V. When the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected down stream components.

The internal Over Voltage Thresholds (OVP) are preset to 6.8V typical. The RT9746 also feature an over-current protection and up to 4.5A.

The RT9746 is offered in a small WL-CSP-12B (BSC) package provides small PCB area applications.

Ordering Information

RT9746 □□

Package Type
WSC : WL-CSP-12B 1.92x1.27

OVP Threshold Option
Default : 6.8V
A : 11.5V
B : 14.5V
C : 6.2V

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

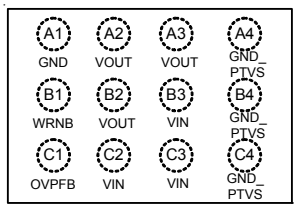
- **PTVS Diode Embedded for VBUS Surge Protection**
- **Warning Indicator for OVP or UVP**
- **28V Maximum Rating for DC Adapter**
- **Integrated Over-Voltage and Over Current Protection FET on VBUS for Fault Isolation**

Applications

- Cellular Phone
- Smart Handheld Device

Pin Configurations

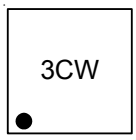
(TOP VIEW)



WL-CSP-12B 1.92x1.27 (BSC)

Marking Information

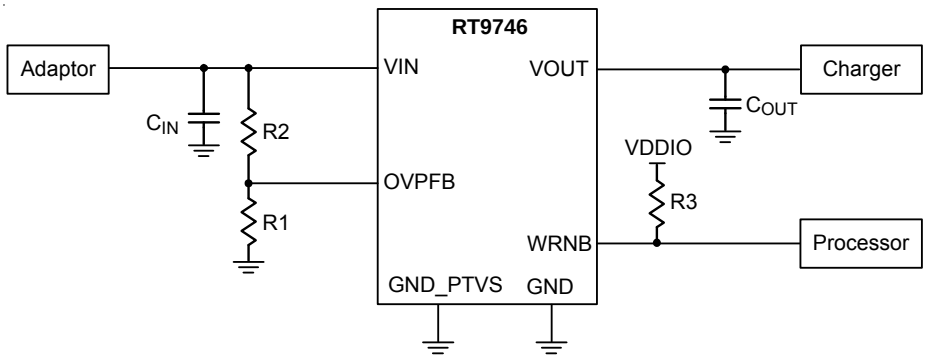
RT9746WSC



3C : Product Code

W : Date Code

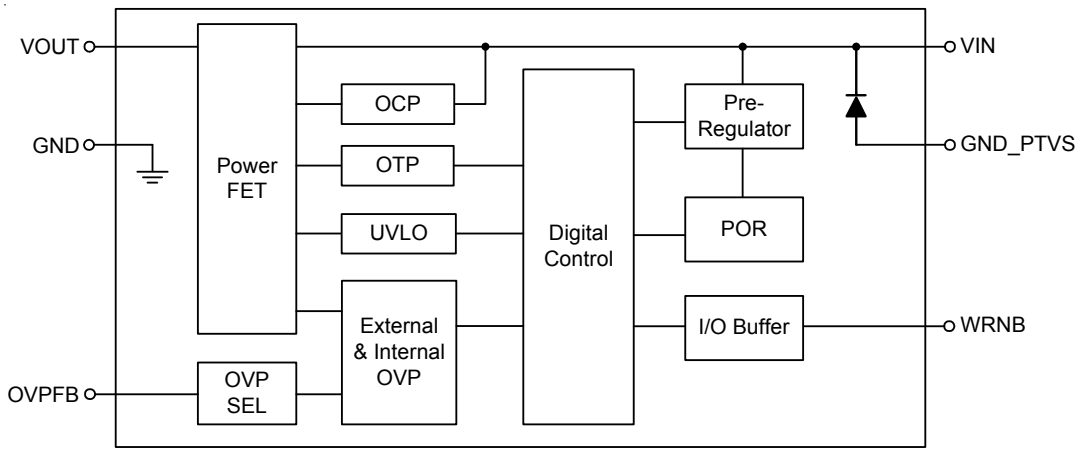
Simplified Application Circuit



Functional Pin Description

Pin No	Pin Name	Pin Function
A1	GND	Common Ground Of Internal Circuits.
A2, A3, B2	VOUT	Output from VBUS Load-Switch.
B1	WRNB	Inverse Warning Signal (OCP,OTP, OVP, UVLO) Flag Output (Open-Drain).
A4, B4, C4	GND_PTVS	Common Ground of Power TVS Diode.
B3, C2, C3	VIN	VBUS from Power Adaptor.
C1	OVPFB	External OVP Adjustment Setting. (if no used, be surely tied to GND)

Function Block Diagram



Operation

The RT9746 is a VBUS OVP protector switch. The OVP function is optimized to protect low voltage system from abnormal high input voltage (up to 28V) in handheld application. RT9746 is also embedded Power-TVS diode (PTVS) on VBUS pin for surge protection. If surge waveform is above 30V, it will be clamped to 30V due to PTVS diode. When plugging in VBUS, the OCP will be soft-start in 8ms in order to reduce in rush current and internal VOUT deglitch time is 16/32/64/128ms which is set by fuse. The OCP after soft-start is up to 4.5A for high current application.

Absolute Maximum Ratings (Note 1)

- VIN, OVPFB ---------- –0.3V to 28V
- VOUT ---------- –0.3V to 15V
- System Level with Air Discharger, VIN, GND ---------- ±15kV
- System Level with Contact Discharger, VIN, GND ---------- ±8kV
- All Other Inputs ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  WL-CSP-12B 1.92x1.27 (BSC) ---------- 1.67W
- Package Thermal Resistance (Note 2)
  WL-CSP-12B 1.92x1.27 (BSC), θ_{JA} ---------- 59.6°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V
  CDM (Charged Device Model) ---------- 2kV
- Surge (VIN) ---------- 100V

Recommended Operating Conditions (Note 4)

- USB Supply Input Voltage, VIN ---------- 3V to 6.7V
- I/O Supply Voltage (V_{DDIO}) ---------- 1.8V to 3.6V
- VOUT Capacitors ---------- 1µF to 10µF
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 5V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	TYP	Max	Unit
DC Characteristics							
Input Clamp Voltage	V_{IN_CLAMP}	I_{IN} = 10mA, T_A = 25°C		--	31	--	V
VIN Supply Current	I_{VBUS_S}	V_{BUS} = 5V, I_{OUT} = 0mA		--	130	180	µA
VIN POR Threshold Only for VOUT	V_{POR}	Rising		2.5	2.7	2.9	V
VBUS POR Hysteresis Only for VOUT	V_{POR_Hys}	Falling		--	100	--	mV
Deglitch Time of POR Only for VOUT	t_{POR}	by EFUSE setting (16/32/64/128ms)		--	32	--	ms
OVP Threshold Voltage	V_{OVP}	Rising	RT9746	6.6	6.8	7	V
			RT9746A	11.15	11.5	11.85	
			RT9746B	14	14.5	15	
			RT9746C	6	6.2	6.4	

Parameter	Symbol	Test Conditions	Min	TYP	Max	Unit
OVP Hysteresis	V_{OVP_HYS}	Falling	--	150	--	mV
OVP Propagation Delay to Turn Off VBUSOUT	t_{OVP_PD}	V_{BUS} = 5V to 10V, (6V/μs)	--	0.18	0.25	μs
OVP Recover Delay	t_{OVP_RD}	V_{BUS} = 10V to 5V	--	8	--	ms
OCP Threshold Current	I_{OCP}		--	4.5	5	A
OCP Blanking Time	t_{OCP_B}		--	180	--	μs
OCP Recover delay	t_{OCP_RD}		--	64	--	ms
OTP Threshold to turn off only for VBUS_OUT	T_{OTP_FET}	Rising (Note5)	--	160	--	°C
OTP Threshold Hysteresis only for VBUS_OUT	$T_{OTP\_FET\_HYS}$	Falling (Note5)	--	20	--	°C
OTP Recover Delay	t_{OTD_RD}		--	8	--	ms
OCP Soft-Start Time	tss		--	8	--	ms
FET On Resistance	R_{ON_FET}	I_{BUS_OUT} = 1000mA, V_{BUS} = 5V T_A = 25°C	--	35	42	mΩ
External OVP Set Threshold	V_{REF_EXT}		--	1.2	--	V
External OVP Adjustment Range	V_{OVP_EXT}		4	--	20	V
External OVP Select Threshold (Rising)	V_{OVP_SEL}		--	0.3	--	V
External OVP Select Threshold Hysteresis			--	100	--	mV
WRNB Open-Drain Impedance		V_{BUS} = 5V	--	--	15	Ω

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

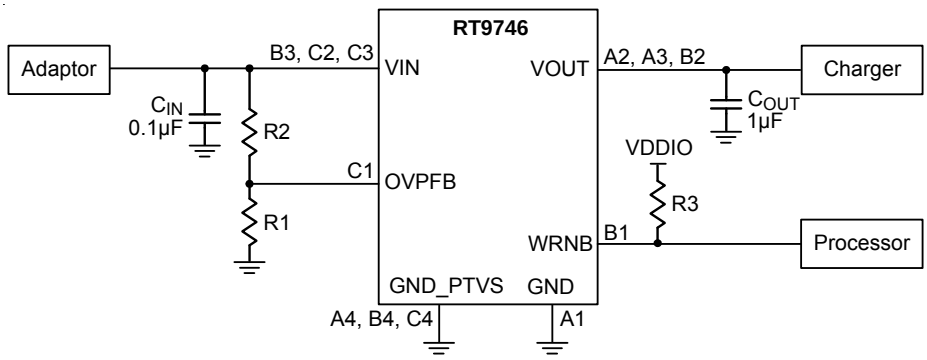
Note 2. θ_{JA} is measured at T_A = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

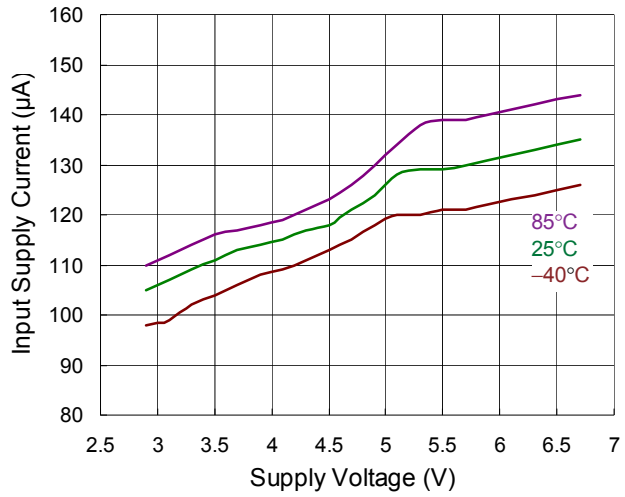
Note 5. Guaranteed by design.

Typical Application Circuit

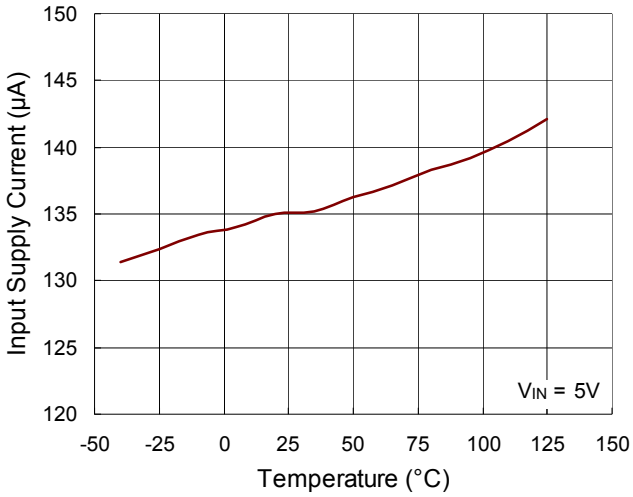


Typical Operating Characteristics

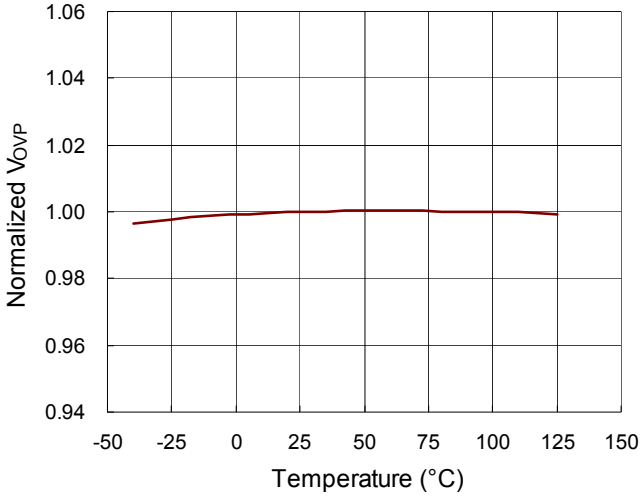
Input Supply Current vs. Supply Voltage



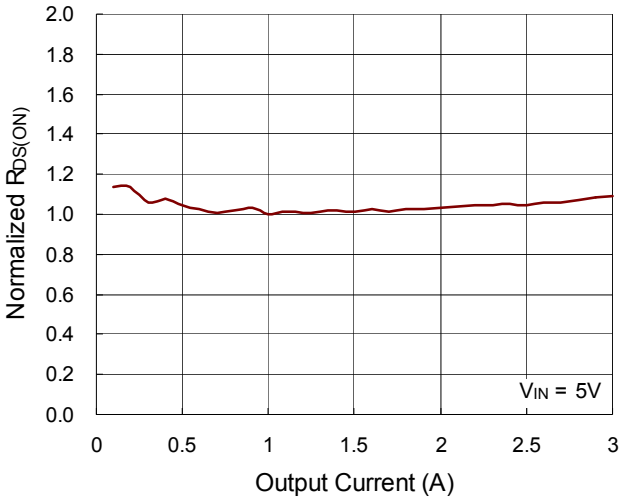
Input Supply Current vs. Temperature



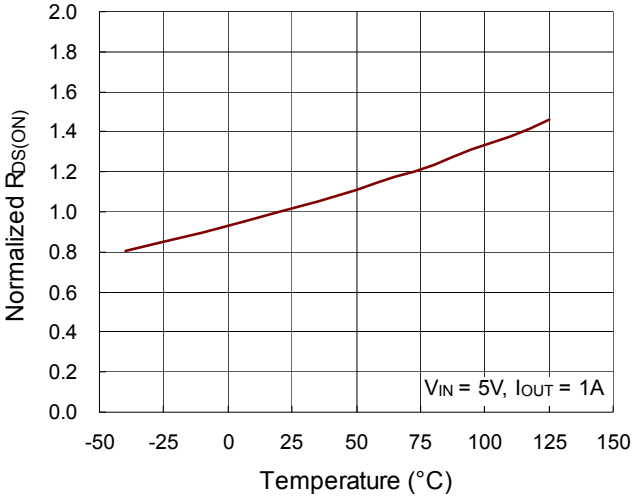
Normalized V_{OVP} vs. Temperature



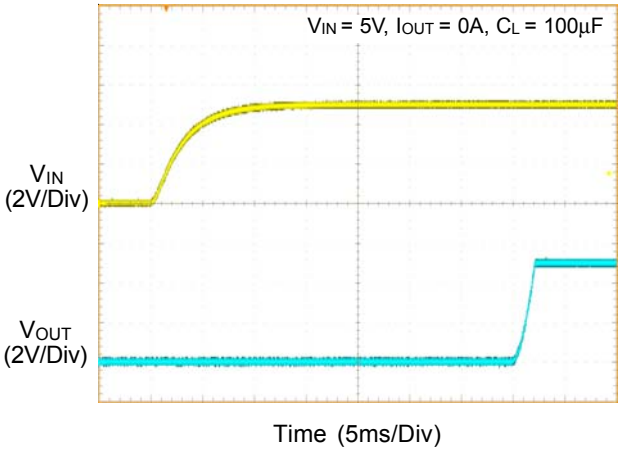
Normalized $R_{DS(ON)}$ vs. Output Current



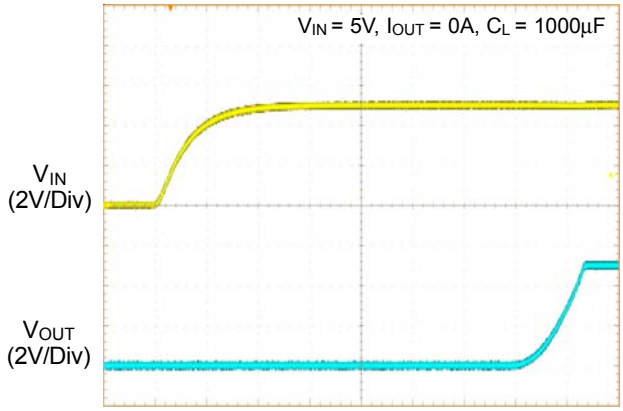
Normalized $R_{DS(ON)}$ vs. Temperature



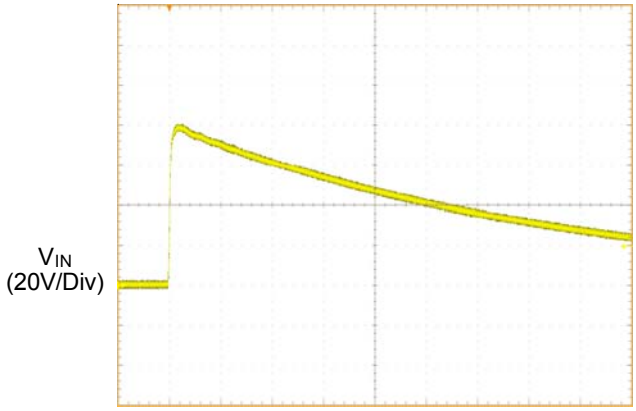
Power Up



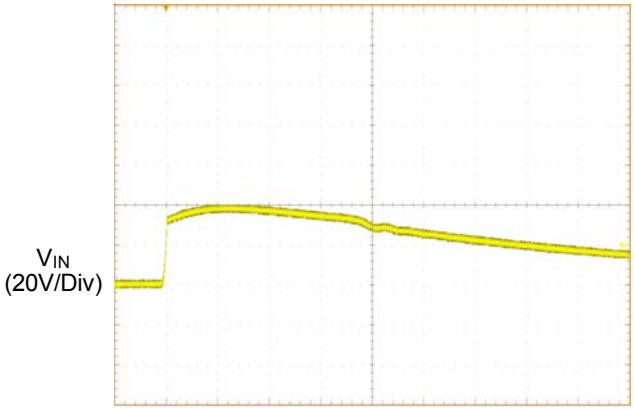
Power Up



80V Surge without RT9746



80V Surge with RT9746



Application Information

Power Up

The RT9746 has a threshold of 2.7V power on reset (POR) with a built-in hysteresis of 100mV. Before the input voltage reaches the POR threshold, the RT9746 is off. When the input voltage is over the POR threshold, the VOUT of RT9746 will delay for 32ms which includes soft-start time of 8ms. The 32ms delay allows the transient at the input during a hot insertion of the power supply to settle down before the IC starts to operate. During the soft-start transition, the RT9746 slowly turns on the internal MOSFET to reduce the inrush current.

Over Temperature Protection (OTP)

The RT9746 monitors its internal temperature to prevent thermal failures. The chip turns off the MOSFET when the junction temperature reaches 160°C. The IC will resume after the junction temperature is cooled down 20°C.

Input Over-Voltage Protection

The RT9746 provides input over-voltage protection via internal or external resistor to set OVP level. If OVPFB is connected to GND, the RT9746 uses the internal OVP level setting. If an external resistor-divider is connected to OVPFB and V_{OVPFB} exceeds the VOVP_SEL voltage, the RT9746 will adopt external OVP level setting. The OVP level VOVP is set as below.

$$V_{OVP} = V_{REF\_EXT} \times \left(1+\frac{R2}{R1}\right)$$

When the input volatge exceeds the OVP level, the RT9746 will turn off internal MOSFET around 0.18us to prevent the high input volatge from damaging the end system. When the input volatge returns to normal operation volatge range with hysteresis (internal 150mV, external 100mV), the RT9746 will turn on the MOSFET to re-enable output.

Over-Current Protection (OCP)

The RT9746 monitors the output current to prevent the output short or the charging of the battery with an excessive current. The RT9746 has a built-in 180μs delay time to prevent any transient noise triggering the OCP. If the OCP situation keeps for 180μs, the internal MOSFET will be turned off.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For WL-CSP-12B 1.92x1.27 (BSC) package, the thermal resistance, θ_{JA}, is 59.6°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C – 25°C) / (59.6°C/W) = 1.67W for WL-CSP-12B 1.92x1.27 (BSC) package

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

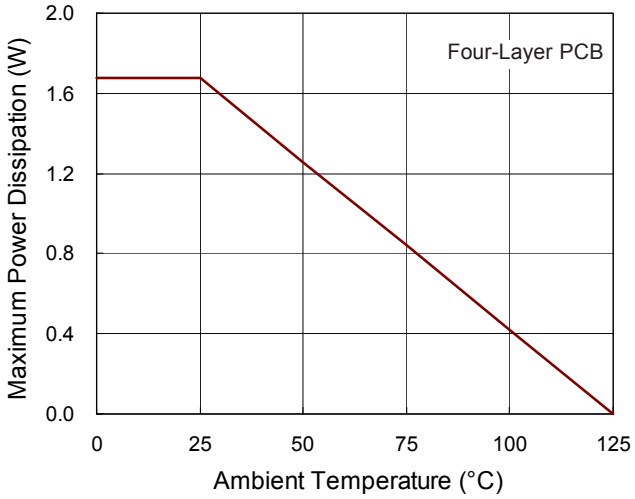
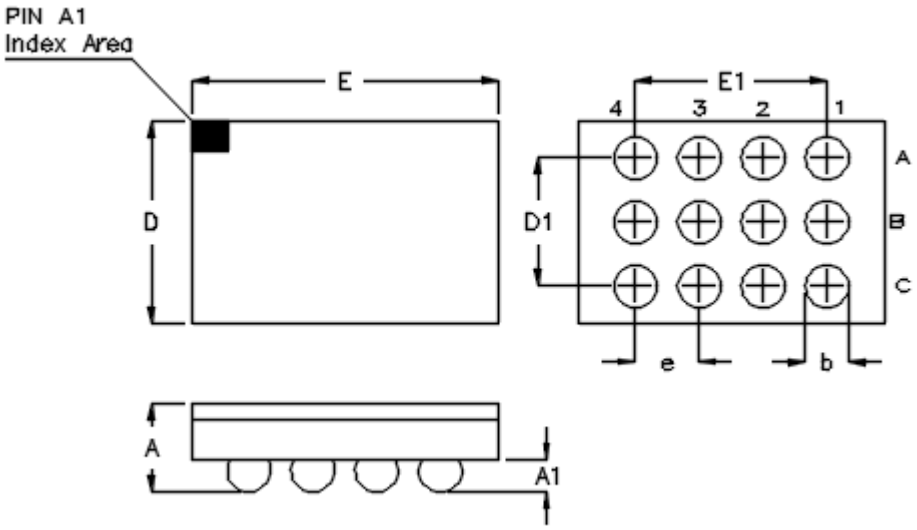


Figure 1. Derating Curve of Maximum Power Dissipation

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.220	1.320	0.048	0.052
D1	0.800		0.031	
E	1.870	1.970	0.074	0.078
E1	1.200		0.047	
e	0.400		0.016	

WL-CSP-12B 1.92x1.27 (BSC)

Richtek Technology Corporation
14F, No. 8, Tai Yuen 1st Street, Chupei City
Hsinchu, Taiwan, R.O.C.
Tel: (8863)5526789