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ACT510x

Rev 1.0, 24-Apr-2018

23V Buck-Boost Converter with Integrated MOSFETs

FEATURES

- Buck-Boost Converter with 4 Integrated Switches
- Wide VIN Range: 4V to 23V (No Dead Zone)
- *3.0V to 23V* Wide output Voltage Range
- Seamless Transition between Buck and Boost Operation
- Supports Programmable Power Supply (PPS)
- Programmable Frequency: 125KHz, 250KHz, 500kHz, and 1MHz
- 2V ~ 5V/100mA Programmable Output LDO
- +/-4% Output Constant Current Regulation (@10mΩ, 3A)
- Programmable Output Voltage and Current via both Pin and I2C
- Enable Pin for Power On/OFF Control
- Output Cord Compensation
- Programmable Output Soft-Start
- Cycle by Cycle Current Limit
- Built in ADC for Temperature, Input and Output Voltage and Current Monitoring
- 25mΩ FET from VIN to SW1
- 25mΩ FET from SW2 to VOUT
- 35mΩ FET from SW1 to PGND
- 35mΩ FET from SW2 to PGND
- Thermal Protection
- Thermally Enhanced 32-Lead 4mx4mm QFN

APPLICATIONS

- Car Charger
- Docking Stations
- Multiple Power Source Supplies
- DC UPS
- Solar Powered Devices
- Solid-State Lighting

GENERAL DESCRIPTION

The ACT510x is a buck-boost converter with 4 integrated MOSFETs. It offers a high efficiency, low component counts, compact solution for a wide input voltage range from 4V to 23V application.

The 4 internal low resistance NMOS switches minimize the size of the application circuit and reduce power losses to maximize efficiency. Internal high side gate drivers, which require only the addition of two small external capacitors, further simplify the design process. An advanced switch control algorithm allows the buck-boost converter to maintain output voltage regulation with input voltages that are above, below or equal to the output voltage. Transitions between these operating modes are seamless and free of transients and subharmonic switching.

The ACT510x output voltage can be set between 3V ~ 23V which can be configured by either external resistor divider or I2C. The output constant current limit and cord compensation makes it flexible for any kinds of protocols like USB PD, QC 3.0/4.0 etc. The system can be monitored and configured by I2C as well. The build-in ADC can be read for the information of input/output voltages and currents, die temperature, and generic input signals.

ACT510x integrated a 100mA LDO output with OCP/UVLO protection to provide power for the MCU and other peripheral components inside the system.

The ACT510x operation frequency can be configured from 125 kHz to 1MHz, makes the system design flexible for components size and efficiency optimization.

The ACT510x has been optimized to reduce input current for applications which are sensitive to quiescent current draw, such as battery-powered devices.

The AC5101 is available in 32-pin, 4 x 4 mm FCOL QFN package.

ORDERING INFORMATION

PART NUMBER	Fsw	Feedback	ADC Converter Input
ACT5101QI101-T	500kHz	Internal	YES
ACT5102QI101-T	500KHz	External	NO

PIN CONFIGURATION

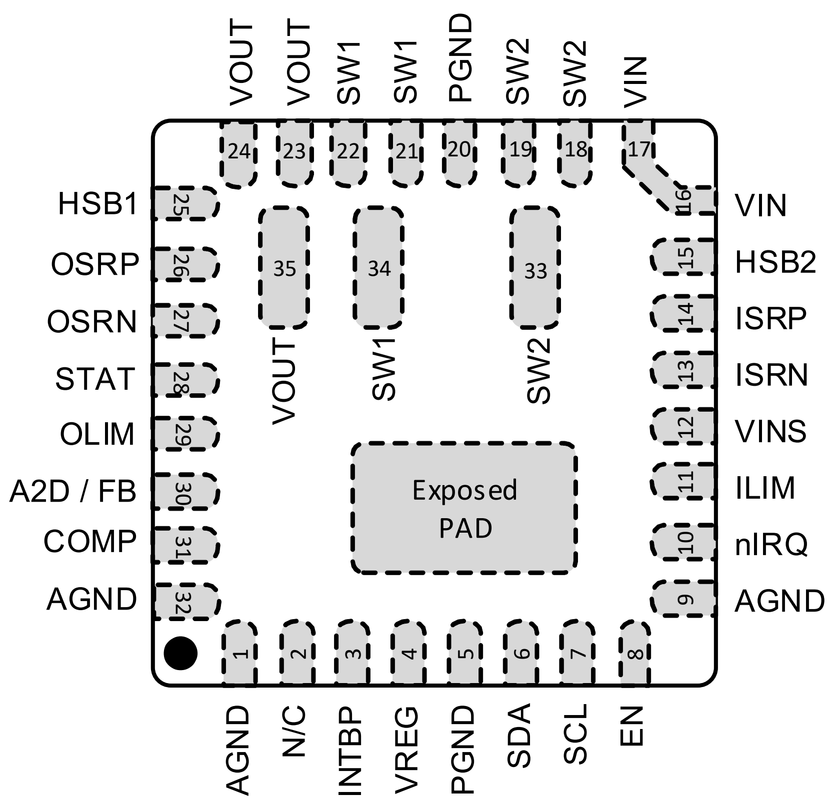


Figure 1: Pin Configuration – Top View – QFN4x4-32

PIN DESCRIPTIONS

PIN	NAME	Type	DESCRIPTION
1, 9, 32	AGND	P	Analog ground of the IC.
2	NC	I	No connect
3	INTBP	O	Internal Bypass - This should be connected to a 100nF ceramic capacitor
4	VREG	I	Internal VREG LDO output. The output voltage is programmable from 2V to 5V. Connect a 1.0uF to this pin. The maximum current capability for this pin is 100mA. The internal Overcurrent and over temp circuit shut down the converter when VREG is overloaded.
5, 20	PGND	P	Power ground of the IC.
6	SDA	I/O	I2C Interface data.
7	SCL	I	I2C Interface clock.
8	EN	I	Converter enable Input. The converter is active when this pin is pull low.
10	nIRQ	I	Interrupt IRQ open drain output.
11	ILIM	I	Input maxim current setting pin. Connect a resistor from ILIM to AGND to program the maxim input current.
12	VINS	I	VIN Sense Input
13	ISRN	I	Negative input current sense amplifier inputs. Sense resistor is optional.
14	ISRP	I	Positive input current sense amplifier inputs.
15	HSB2	P	High Side Bias Pin. This provides power to the internal high-side MOSFET gate driver. Connect a 47nF capacitor from HSB2 pin to SW2 pin.
16, 17	VIN	P	Input power pins. Decoupling capacitor should be placed from this pin to PGND.
18, 19	SW2	P	Power switching output node to external inductor.
21, 22	SW1	P	Power switching output node to external inductor.
23, 24	VOUT	P	Output pins. Decoupling capacitor should be placed from this pin to PGND.
25	HSB1	P	High Side Bias Pin. This provides power to the internal high-side MOSFET gate driver. Connect a 47nF capacitor from HSB1 pin to SW1 pin.
26	OSRP	I	Output current sense resistor positive input.
27	OSRN	I	Output current sense resistor negative input.
28	STAT	O	Open drain status output to indicate various charger operation. A LOW indicates converter is running. If converter is disabled for any reason, such as VOUT fault or VIN UV etc., STAT will go high.
29	OLIM	I	Output constant current limit setting pin. Connect a resistor from OLIM to AGND to program the output current.
30 (ACT5101)	A2D	I	A2D Input Pin
30 (ACT5102)	FB	I	Input FB pin
31	COMP	O	Error Amplifier Output. This pin is used to compensate the converter.
	Power Pad	P	Exposed pad. Must be shorted to ground on the PCB.

FUNCTIONAL BLOCK DIAGRAM

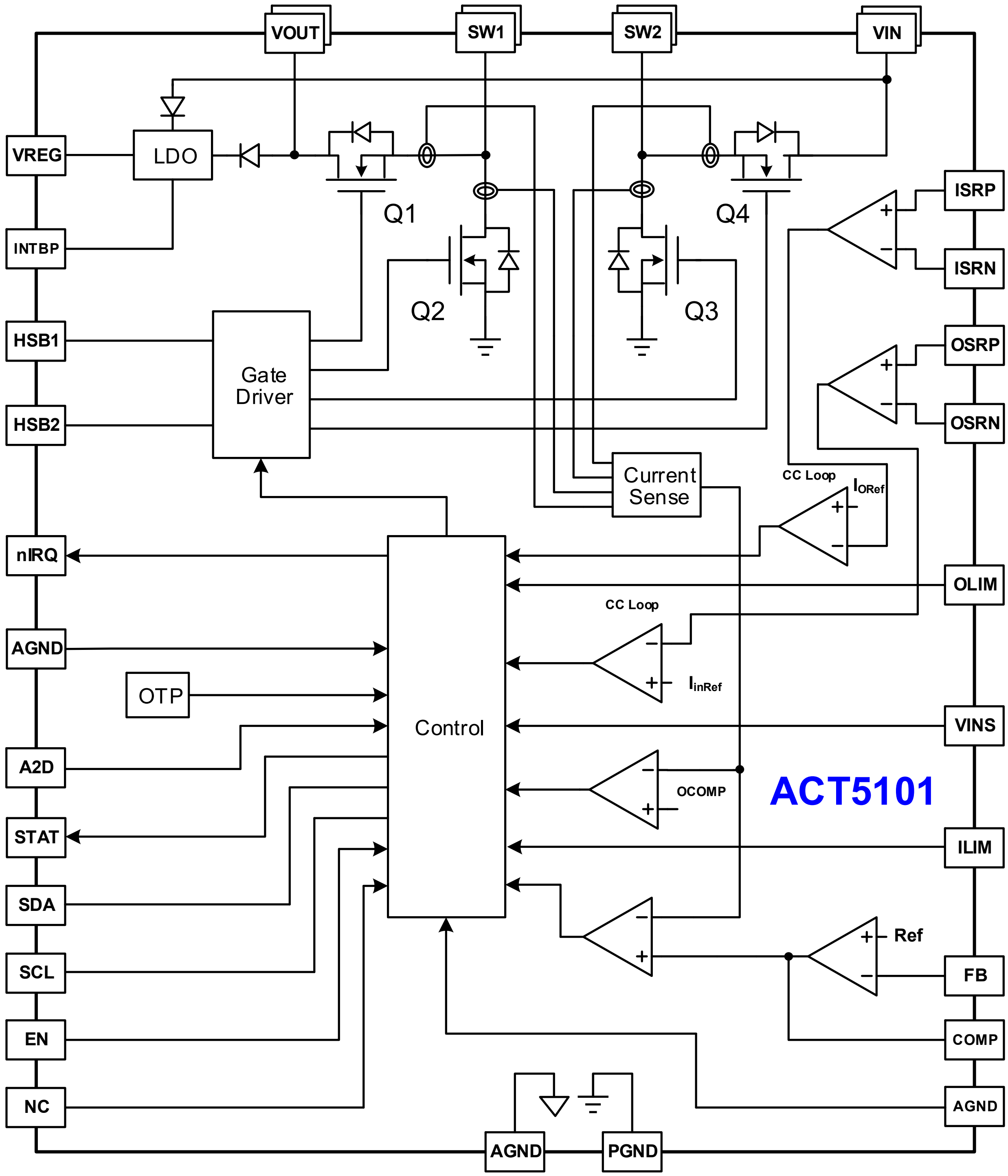


Figure 2: Function Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE	UNIT
VOUT	-0.3 to +24	V
OSRP, OSRN	-0.3 to VIN + 0.3	V
VIN	-0.3 to +23	V
ISRP, ISRN	-0.3 to VBAT + 0.3	V
VINS	-0.3 to ISRN + 0.3	V
SW1	-0.3 to VOUT + 0.3	V
SW2	-0.3 to VIN + 0.3	V
HSB1	V_{SW1} - 0.3 to V_{SW1} + 5.5	V
HSB2	V_{SW2} - 0.3 to V_{SW2} + 5.5	V
VREG	-0.3 to +6V	V
SCL, SDA, VREG, STAT, EN, nIRQ, FB, COMP, ILIM, OLIM, A2D	-0.3 to +6	V
AGND to PGND	-0.3 to +0.3	V
Junction to Ambient Thermal Resistance (θ_{JA})	35	°C/W
Operating Junction Temperature (T_J)	-40 to 150	°C
Operating Ambient Temperature Range (T_A)	-40 to 85	°C
Store Temperature	-55 to 150	°C
Lead Temperature (Soldering, 10 sec)	300	°C

Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(VIN = 5V, T_A = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Converter OPERATION						
Output Voltage Accuracy	$V_{OUT\_REG\_ACC}$	Internal Feedback VOUT_I2C Register = 1 Converter output in PWM Mode. Measured at VOUT Pin	-1		1	%
FB Reference Voltage	$V_{OUT\_REF\_ACC}$	External Feedback VOUT_I2C Register = 0	1.99	2	2.01	V
Input UV Voltage	V_{IN_UV}	VIN Rising Measured at V_{IN_UV} Register setting Measured at VINS Pin	-3.0	V_{IN_UV}	3.0	%
Input UV Voltage Hysteresis	$V_{IN\_UV\_HSYT}$	VIN Falling Measured at V_{IN_UV} measured value Measured at VINS Pin	3	4	5	%
Input OV Threshold	V_{IN_OV}	VIN Rising Measured at VINS Pin	22.75	23.5	24.25	V
Input OV Hysteresis	$V_{IN\_OV\_HYST}$	VIN Falling Measured at VINS Pin		300		mV
Output Current Range	I_{OUT_RANGE}	With I_{CHG}=100% register setting	0.5		5	A
Output Constant Current (measured at OSRN and OSRP pins) (10mΩ current sensing resistor) (20mΩ current sense resistor as option)	I_{OUT_OCP}	I_{OUT_OCP} = 0.5A to 1A	-20	I_{OUT}	+20	%
		I_{OUT_OCP} = 1A to 2A	-15	I_{OUT}	+15	%
		I_{OUT_OCP} > 2A	-10	I_{OUT}	+10	%
Output Constant Current Undervoltage Protection Threshold	V_{OUT_UVP}	VOUT Falling, Enters Hiccup Mode Internal or External Feedback control Measured at VOUT pin	2.90	3.0	3.10	V
Output Constant Current Undervoltage Protection Deglitch Time	t_{OUT_UVP}	V_{OUT} Falling		7		us
Hiccup Mode Off Time	t_{OUT_HICCUP}	Off time after V_{OUT} falls below V_{OUT_UVP}		3		sec
Over-Voltage Threshold	$V_{OUT\_OVP\_EXT}$	External Feedback VOUT_I2C Register = 0 Voltage at FB Pin	2.18	2.24	2.30	V
Over-Voltage Threshold Hysteresis	$V_{OUT\_OVP\_HYS}$	Falling Threshold		2		%
Soft Start Time	t_{OUT_SS}	Measured at Soft Start Register From 0 to 100%	-30	SOFT START Setting	30	%
Pulldown Current Source	I_{OUT_PD}	V_{OUT} Output > 2.0V	30	65	120	mA

Off Delay Current Timer	$t_{OUT\_OFF\_DLY}$	EN_DLY Enabled	-10	OFF_DLY Setting	+10	%
Off Delay Current	$I_{OUT\_OFF\_LOAD}$	OFF_LOAD=0 Converter in Buck Mode Only $V_{IN} > V_{OUT}$ + 0.5V	0.5	1	1.5	mA
		OFF_LOAD=1 Converter in Buck Mode Only $V_{IN} > V_{OUT}$ + 0.5V	4	5	6	mA
Cord Compensation Accuracy	V_{OUT_CC}	Cord Compensation Enabled CORD_COMP: 00: Disabled 01: 100mV 10: 200mV 11: 300mV Measured at VOUT Pin	-15	CORD_ COMP Setting	+15	%
Output Slew Accuracy	t_{OUT_SLEW}	Output Slew Setting OUTPUT_SLEW 00: 1.0V/ms 01: 0.5V/ms 10: 0.3V/ms 11: 0.1V/ms Internal Feedback Only VOUT_I2C Register = 1	-20	OUTPUT_SLEW Setting	+20	%
Input Current ILIM	I_{ILIM}	I_{ILIM} = 0.5A to 1A	-20	I_{ILIM}	+20	%
		I_{ILIM} = 1A to 2A	-15	I_{ILIM}	+15	%
PWM OPERATION						
Frequency Range	f_{SW}		125		1000	kHz
Operation Frequency Accuracy	f_{SW}		-10%		+10%	kHz
Maximum PWM Duty Cycle	D_{MAX}			97		%
VREG LDO						
VREG Regulation Voltage	VREG		2		5.1	V
VREG Regulation Accuracy	$VREG_{ACC}$	At Default Factory Setting	-2		2	%
VREG Dropout	$VREG_{DROPOUT}$	I_{OUT}=100mA			300	mV
VREG UVLO Threshold	$VREG_{UVLO}$	VREG Falling	85	88	91	%
VREG UVLO Hysteresis	$VREG_{UVLO\_HYST}$			2		%
VREG Current Limit	$VREG_{ILIM}$	V_{VIN} = 12V, VREG = 5V	100		200	mA
VREG Current Limit Deglitch	$VREG_{ILIM\_DG}$	In current limit		50		us
VREG Current Limit Off Time	$VREG_{ILIM\_OFF}$	After Deglitch Time		100		ms
VREG Soft Start	$VREG_{SS}$			250		us

LOGIC I/O PIN CHARACTERISTICS EN, STAT, nIRQ						
EN Input low threshold	V_{ILO}				0.4	V
EN Input high threshold	V_{IHI}		1.25			V
STAT, nIRQ Output Low Voltage	V_{OL}	Sink Current = 5 mA			0.4	V
STAT, nIRQ High Level Leakage Current	I_{OH}	Output = 5V			1	uA
I2C INTERFACE CHARACTERISTICS						
SCL, SDA Input low threshold	V_{ILO}	Design Note: Need to be sure supply current is 0 with 1.8V input on pin			0.4	V
SCL, SDA Input high threshold	V_{IHI}	Design Note: Need to be sure supply current is 0 with 1.8V input on pin	1.25			V
SDA Output Low	V_{OL}	Sink Current = 5 mA			0.4	V
SDA High Level Leakage Current	I_{OH}	Output = 5V			1	uA
SCL Clock Frequency	f_{SCL}		0		1000	kHZ
SCL Low Period	t_{SCL_LOW}		0.5			us
SCL High Period	t_{SCL_HI}		0.26			us
SDA Data Setup Time	t_{SU}		50			ns
SDA Data Hold Time	t_{HD}		0			ns
Start Setup Time	t_{ST}		260			ns
Stop Setup Time	t_{SP}		260			ns
Capacitance on SCL or SDA PIN	C_{IN}				10	pF
Pulse Width of spikes suppressed on SCL and SDA	$t_{DEGLITCH}$				50	ns
I2C Timeout Function	t_{out}	Total time required for I^2C communication to cause I^2C state machine to reset		100		ms
THERMAL REGULATION AND THERMAL SHUTDOWN						
Charger Mode Junction Temperature Regulation Accuracy	T_{REG}	Charger Mode 00: 60 °C 01: 80 °C 10: 100 °C 11: 120 °C	-20	T_{REG}	+20	°C
Thermal Shutdown Rising Temperature	T_{SHUT}	Temperature Increasing		160		°C

Thermal Shutdown Hysteresis	T_{SHUT_HYS}			30		°C
Thermal Shutdown Deglitch		Enter or Exit Thermal Shutdown		32		us
A2D Converter						
Total Error	$A2D_{ERROR}$	12 Bit Range			0.5	LSB
Conversion Time	$A2D_{tCONV}$	All 8 Channels			100	ms
Conversion Time	$A2D_{tCONV}$	1 Channel			15	ms
Input Capacitance	$A2D_{CIN}$			5		pF
A2D Full Scale Input EXT_IN	$A2D_{FS}$			2.5		V
A2D Full Scale VOUT	$A2D_{VOUT}$	Measurement input at VOUT pin		32.5		V
A2D Full Scale VIN	$A2D_{VIN}$	Measurement input at VINS Pin		25		V
A2D Full Scale OLIM, ILIM	$A2D_{OLIM}$, $A2D_{ILIM}$			2.5		V

FUNCTIONAL DESCRIPTION

1. Buck-Boost Structure

The ACT510x is a monolithic buck-boost converter with integrated FETs. Four internal low resistance NMOS switches minimize the size of the application circuit and reduce power losses to maximize efficiency. Internal high side gate drivers, which require only the addition of two small external capacitors, further simplify the design process. An advanced switch control algorithm allows the buck-boost converter to maintain output voltage regulation with input voltages that are above, below or equal to the input voltage. Transitions between these operating modes are seamless and free of transients and subharmonic switching.

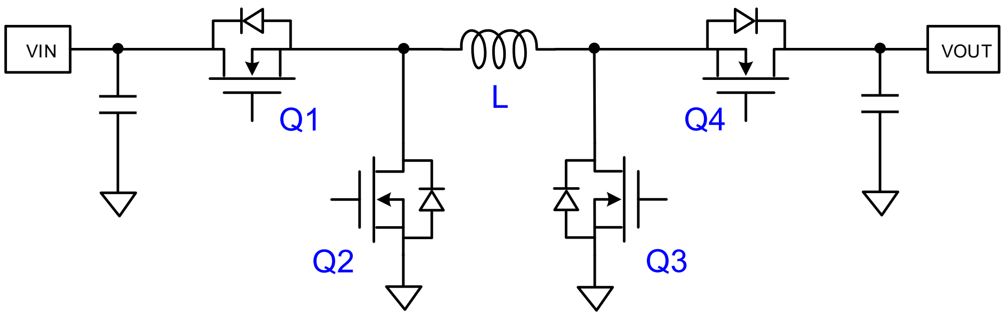


Figure 3: Diagram for 4-Switches Buck-Boost Converter

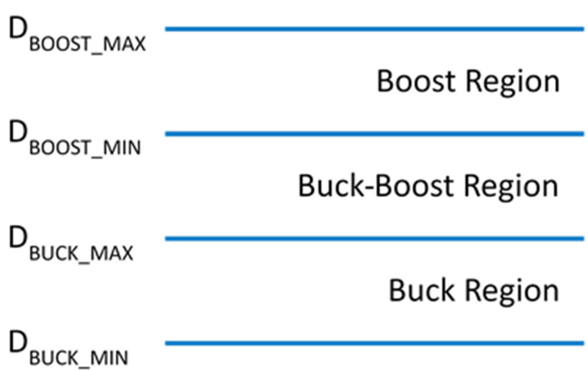


Figure 4: Operation Mode and Regions

Figure 3 shows a simplified diagram of how the four power switches are connected to the inductor, VIN, VOUT and GND. Figure 4 shows the regions of operation for the ACT510x as a function of duty cycle D. The power switches are properly controlled so the transfer between modes is continuous. When VIN approaches VOUT, the buck-boost region is reached.

Table 1: MOSFET Operation

MODE	BUCK	BUCK-BOOST	BOOST
Q1	SWITCHING	SWITCHING	ON
Q2	SWITCHING	SWITCHING	OFF
Q3	OFF	SWITCHING	SWITCHING
Q4	ON	SWITCHING	SWITCHING

2. Operation States

2.1. Reset State (RST)

The state machine for the converter always starts from the Reset State. The device waits until all the criteria below are met and then starts the Enable Delay Timer. This timer is controlled by *EN_DLY[1:0]* Register 0x0F Bits 1:0. Once the timer has expired, it will jump out of the Reset state and move to the SS state

Reset Faults:

1. VIN below VIN_UV voltage: This fault will self-clear and device will exit the Reset when the VIN is higher than the threshold.
2. VREG LDO OK – This fault will automatically clear when the VREG LDO has exited the faulted condition and UVLO is low. This includes the 100msec timeout period. Once the VREG LDO regulator is at an acceptable level, the device will exit the Reset state. Note: This fault can be masked to allow the state machine to exit the Reset while there is a fault on the VREG LDO using the *DIS_VREG_FLT* Register 0x10 Bit 1.
3. Watchdog Timer Fault: If the watchdog timer is enabled and the timer ties out, the Watchdog fault will hold the charger in the RST state until the watchdog timer is reset or cleared. It can be reset with a write to of 1 to the *WATCHDOG_RESET* Register bit or by disabling the Watchdog timer with *WATCHDOG[1:0]* Register = 00.
4. FET Overcurrent Fault: If a switching FET exceeds the cycle by cycle current limit for 8 (or 16) cycles, the FET_OC fault is latched. To clear this latch, the device must exit the operation mode and enter HIZ mode, typically by toggling the EN pin or setting the *HIZ* register to HI.
5. VIN Overvoltage: If the VIN exceeds the V_{IN_OV}, the device will enter the Reset state. The OV fault will self-clear when the VIN is below the V_{IN_OV} and exit the Reset state.
6. Die Thermal Shutdown (TSD) – If the die exceeds the T_{SHUT} (160°C) this fault will hold the converter in the FAULT state until it cools down by the T_{SHUT_HYST} (T_{SHUT} - 30°C). This fault cannot be cleared or masked. The device must cool down before exiting the Reset state. Once the device cools down, it will automatically clear this fault and exit the Reset state and resume operation.

2.2. Soft Start (SS)

The device enables the converter and ramps the soft start output in this mode. Soft start time is controllable by the *SOFT START [1:0]* Register. If a fault occurs during the soft start, it will jump back to the Reset state and disable the converter. Once the soft start is done, the device jumps to the Regulation state.

2.3.Regulation State (REG)

The normal regulation occurs in the Regulation state. If a major fault occurs during the device will jump back to the Reset state and disable the converter. During this state, the converter can be disabled with light load condition. Additionally, if the output drops below V_{OUT_UVP} (3.0V), the device will go into a hiccup mode to protect the output in a shorted condition.

2.4.Light Load Disable State (LL_DIS)

If the device senses light load in Regulation state, the converter will be disabled after the *OFF_DLY[1:0]* timer expires. During this state, the converter is disabled and there is minimal load on the VIN. To exit this state, the device must exit converter mode by the EN pin or *HIZ* register. The light load disable function can be disabled in the register bit.

2.5.Hiccup / Vout Fault State (HICCUP)

If the output cannot support the load and enters Constant Current mode in Regulation state, the output will eventually drop below the V_{OUT_UVP} (3.0V). If this occurs, the converter is disabled for 3 secs, and then automatically re-enters the Reset mode to restart the output. If there is a fault on the output, this cycle will continue until the fault is removed.

3. Device Power Up

3.1. Power-On-Reset (POR)

When VIN or VOUT is above 3.9V, the I2C bus is ready for communication and the VREF LDO is enabled. All registers are reset to the default value as listed in the register map.

3.2. HIZ Mode

The device goes into HIZ mode when EN is pin HI, or *HIZ* Register 0x00 Bit 7 is set HI. At HIZ mode, the internal bias circuits are enabled, all registers are accessible and ADC functions can be enabled. If the VREG_EN Register 0x01 Bit 2 is HI, then the VREG LDO will be enabled.

3.3. VREG LDO

The VREG LDO is powered from VIN or VOUT with a smart active diode selector circuit.

To reduce power dissipation, the VREG LDO will be powered from the lower of the VIN or VOUT. However, if the lower supply cannot provide the headroom needed to regulate VREG output, it will select the higher supply.

This smart diode selector can be overridden and manual control can be selected using the *VREG_OVERRIDE* and *VREG_SELECT* Registers 0x0B, bits 1:0.

The VREG is enabled when all the conditions are valid:

- VIN or VOUT above UVLO (3.9V)
- VREG_DIS Register is bit is set LO (Register 0x01 Bit 2)
- This register bit can be programmed from the factor to be HI or LO depending on the application requirements

The voltage of VREG LDO can be set by Register 0x11 [7:3] between 2V to 5.1V. The maximum output current is 100mA. If VREG LDO is overloaded or not within spec, converter will be shut down, and *VREG_OC_UVLO* fault bit Register 0x05 Bit 4 is set.

Additionally, if the VREG_LDO is held in current limit for more than 50usec, it will shut down for 100msec to prevent damage. It will then re-try to start after 100msec. It will continue this cycle until the current limit condition is removed. Additionally, there is a UVLO detection for the VREG output set at 88%.

If the VREG output is in current limit, or below the UVLO threshold, the converter will be in a Fault state or Reset state and not operate. This can be overwritten with *DIS_ VREG_FLT* Register 0x10 Bit 1.

To reduce inrush current, a 250usec soft-start is included. For stability, a 1uF ceramic capacitor is required on the output.

4. Host Mode and Default Mode

The ACT510x is a host controlled device, but it can operate in default mode without host management. In default mode, ACT510x can be used an autonomous converter with no host or with host in sleep. In this mode, the *WATCHDOG[1:0]* Register 0x01 Bits 1:0 must be set LO to disable the watchdog timer. Additional register bits may need to be set to allow this mode.

5. Converter Operation

The ACT510x can be enabled if the conditions are valid (see operating states for further details):

1. EN Pin is Low or *EN_OVERRIDE bit* is HI
2. *HIZ* Register bit is low
3. *EN* Register bit is HI

The output voltage can be set by the internal resistor divider or the feedback resistor divider on the FB pin using the *VOUT_I2C* Register 0X13 [3]. When the internal resistor divider network is used, the output voltage can be changed by

VOUT[10:0] voltage register. The ramp rate the output changes can be controlled by the *OUTPUT_SLEW[1:0]* register. This allows the output to conform to QC2.0/QC3.0/4.0/USB PD functions for higher output voltages.

If external feedback is used, the reference voltage on FB is 2V. The COMP pin is used for the output compensation.

Input voltage must stay above V_{IN_UV} set by *VIN_UV* Register 0x0F [7:5].

5.1. Enable Delay

Once the condition has the valid conditions for startup, the Enable Delay timer is enabled. The timer options allow an immediate startup, or to wait between 200msec and 1sec before enables the converter. This timing is controlled by the *EN_DLY[1:0]* register.

5.2. Mode Soft Start

After the Enable Delay has completed, the device starts the output using a soft start function programmable by the *SS[1:0]* Register. The time is independent of the output voltage setting if using internal feedback and or resistor settings when using external feedback.

5.3. Constant Current Output Regulation

After soft start is completed, the device monitors the current on sense resistor (OSRP and OSRN) to provide constant current regulation. When the output current exceeds threshold the value configured by the OLIM Pin and CC Register, the switching converter will regulate the maximum current in a “constant current” mode. In this case, the output voltage may drop. Constant current mode can be monitored in real time using the read only *Output_CC* Register 0x20 [5].

The current can be controlled with the external resistor on the OLIM pin and by the CC [6:0] Register 0x17 [6:0]. Current is adjustable as a percentage of the full current level set by the OLIM resistor.

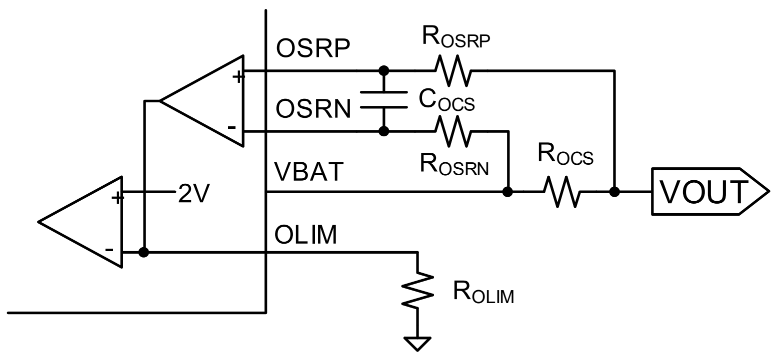


Figure 5: Charge Current Sensing and Current Limit Setting

This voltage on the OLIM pin is calculated by:

$$V_{OLIM} = R_{OCS} \times I_{CHG} \times R_{OLIM} \times 2\times10^{-3} \quad \text{Equation 1}$$

The voltage on this pin is regulated and clamped at 2V. The OLIM pin can also be used to monitor input current .The voltage on OLIM pin is proportional to the charge current.

The filter cap C_{OCS} should be 470nF, and R_{OSRP} and R_{OSRN} should be 30Ω.

If the output drops below 2.72V, a fault on the output is assumed, and the converter will disable and wait 3 seconds in the HICCUP state. After 3 seconds, the device will return to the Reset state and attempt to restart the output. If a short or high current fault is present, it will cycle again through the states until the fault is removed.

5.4. Input Current Regulation

ACT510x monitors the current on input side sense resistor (ISRP and ISRN) to provide a current limit from the input. When the input current exceeds threshold the value configured by the ILIM Pin and *INPUT_ILIM* Register 0x10 [3:2], the switching converter will regulate the output current in a “constant current” mode. In this case, the output voltage may drop. Input constant current mode can be monitored in real time using the read only *INPUT_CC* Register 0x20 [6].

Input current limit can be set by the ILIM pin and *INPUT_ILIM* [1:0] Registers 0x10 [3:2]

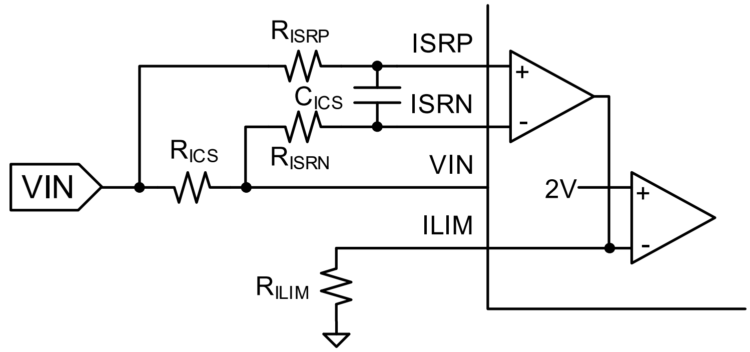


Figure 6: Input Current Sensing and Current Limit Setting

This voltage on the ILIM pin is calculated by:

$$V_{ILIM} = R_{ICS} \times I_{IN} \times R_{ILIM} \times 2 \times 10^{-3}$$ *Equation 2*

The voltage on this pin is regulated and the charger goes into input current limit mode and starts to reduce the charger current when this pin voltage reaches 2V. The ILIM pin can also be used to monitor input current .The voltage on ILIM pin is proportional to the input current.

The filter cap C_{ICS} should be 470nF, and R_{ISRP} and R_{ISRN} should be 30Ω.

If input current limit function is not needed, it can be disabled in *INPUT_ILIM* Register 0x10 [3:2].

5.5. VOUT Over-Voltage Protection

ACT510x monitors the output voltage and immediately stop switching when senses an overvoltage condition. If the OV condition lasts for 100msec, then the device will enter HIZ state.

5.6. Regulator Compensation and Inductor Selection

Table 2: L/C Selection Table

Frequency Setting	Inductor MIN (uH)	Inductor TYP (uH)	Inductor Max (uH)	C_{COMP1} (nF)	C_{COMP2} (nF)	R_{COMP} (KOhms)	C_{OUT} (uF)
125Khz	29	42	55	82	8.2	20.0	1000 / 47
250Khz	15	22	29	39	3.9	20.0	470 / 47
500KHz	7	10	13	22	2.2	20.0	220 / 47
1MHZ	4	5.6	7.28	10	1.0	20.0	100 / 47

47uF is low ESR Ceramic Type. 100uF to 1000uF is bulk electrolytic capacitor.

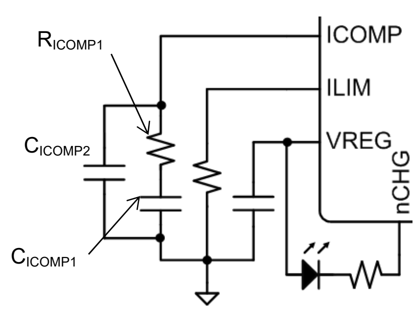


Figure 7: OTG Mode External Compensation Network

5.7. Cord Compensation

ACT510x provides cord compensation at the output. The output voltage is increased with output current to compensate the potential voltage drop across output cable. The amount of cord compensation can be adjusted with the *CORD_COMP[1:0]* register.

Table 3: Output Cord Compensation Setting

***CORD_COMP[1:0]* Setting**	**Cord Comp Value At 2.4A Load**
00	0 (Disabled)
01	100mV
10	200mV
11	300mV

The cord compensation loop should be very slow to avoid potential disturbance to the voltage loop. The voltage loop should be sufficiently stable on various cord compensation setting.

5.8. Light Load Disable

We the device is operating in BUCK mode and VIN is higher than VOUT by a minimum of 0.5V, the device can detect light load / no load case and disable the converter. The *OFF_LOAD_EN* should be set to 1 to enable this feature. The *OFF_LOAD* controls the amount of load on the output that can be detected as light load. Finally, the detection time is set by the *OFF_DLY[1:0]* setting. Once the state machine has detected a light load condition, it enters the LL_DIS state, and the converter must be re-enabled to resume operation, such as toggling the EN pin.

5.9. Output Ramp and Vout OV

To conform to various charging specification, such as QC2.0/3.0/4.0 or USB-PD, the VOUT can be dynamically changed by writing to the *VOUT[10:0]* Register, if internal feedback is used and VOUT_I2C is set to 0. The *OUTPUT_SLEW[1:0]* register is used to control the slew rate between settings when the *VOUT[10:0]* is changed. When the voltage is increased, the internal ramp and regulator can compensate and increase the voltage. However, when the voltage is decreased, and there is no external load on the output, the VOUT may not decrease fast enough to the meet the requirements of QC2.0/3.0/4.0 or USB-PD. To meet the requirement, if the *PULLDOWN_RAMP*=1, an internal 70mA load will turn on when the VOUT is required to decrease from a change in the *VOUT[10:0]* register.

If external feedback is used, and the feedback resistor is changed, the *PULLDOWN_OV* can be enabled. If this bit is set HI, whenever the VOUT goes into OV, the internal 70mA pulldown load will turn on to help regulate the output during a voltage transition.

5.10. Die Thermal Regulation

The ACT510x monitors the internal junction temperature T_J to avoid overheat the chip and limits the IC junction temperature. When the internal junction temperature exceeds the preset thermal regulation limit set by *TREG [1:0]*, the device lowers down the output constant current limit threshold to reduce the output current. The wide thermal regulation range from 80ºC to 120ºC allows the user to optimize the system thermal performance. In addition, this function can be disabled using the *TREG[1:0]*.

5.11. Status Output Pin (STAT)

The ACT510x can indicate converter state on the open drain STAT pin. The STAT pin is mainly used to drive an LED, it can be enabled/disabled by using the *EN_STAT* Register 0x0F [4].

The table below shows the general operation:

Table 4: STAT pin State

State	STAT Output Pin
Converter Enabled and Output Valid	LOW
Converter Disabled	HIZ
Converter Enabled but in Fault, Hiccup or Light Load states	HIZ

6. Interrupt Output Pin (nIRQ)

The nIRQ output pin can be used to signal a fault or other system effects. The conditions below can active the nIRQ Pin and all of them can be masked individually using the IRQ Control Registers 0x1E and 0x1F. To clear the nIRQ and de-assert the nIRQ pin, the nIRQ_CLEAR must be written to a 1. The nIRQ_CLEAR is a self-clearing register bit. If the nIRQ_CLEAR is read, it will always be a 0, even if it has been written to 1.

1. **Watchdog Expired** - If the watchdog timer expires at any time, it will active the nIRQ Pin. This is level sensitive function. The watchdog timer must be reset or disabled and *nIRQ_CLEAR* must be written to 1 for the nIRQ to be de-asserted. – No watchdog in HIZ so cannot be triggered HIZ mode.
2. **VREG LDO Overcurrent or Under-voltage Lockout**- Any time the VREG LDO is in overcurrent or under-voltage lockout, the nIRQ will be asserted. This is a level sensitive function. The VREG LDO must be in regulation AND *nIRQ_CLEAR* must be written to a 1 for nIRQ to be de-asserted. If the VREG LDO is in the 100msec shutdown wait period, it will not clear the nIRQ output. This fault WILL be valid in all modes, including HIZ Mode.
3. **Die Over Temperature Shut Down** - Any time the die temperature exceeds the T_{SHUT} (160°C) threshold, the nIRQ will be asserted. This is a level sensitive function. The die temperature must be below the T_{SHUT_HYST} AND *nIRQ_CLEAR* must be written to 1 for nIRQ to be de-asserted.
4. **FET Overcurrent Fault** – If the device is disabled from switching because of FET overcurrent fault, the nIRQ will be asserted. This is a level sensitive function. This fault is latched, so the latch must cleared AND *nIRQ_CLEAR* must be written to 1 for nIRQ to be de-asserted.
5. **A2D Data Ready** – If the A2D is enabled, and a conversion is completed the nIRQ pin will be asserted. This is an edge triggered event and only a write to1 of *nIRQ_CLEAR* is needed to de-assert the nIRQ pin. This can be active in all modes, when the A2D is enabled.
6. **HIZ Enter** – If the devices enters HIZ mode the nIRQ pin will be asserted. This is an edge triggered event and only a write to 1 of the *nIRQ_CLEAR* is needed to de-assert the nIRQ pin. This is used to signal a fault or other condition that might have caused the device to jump out of operation mode un-expectantly.
7. **I2C Fault** – If the I2C command requires more than 100msec to complete, then a fault is latched on the rising edge of the error. This fault will get reset when another I2C command completes correctly, but is latched with the Reg 0x06 Bit 1.
8. **VOUT OV (30V) –** If the VOUT is above V_{OUT_OVP} (30V), the nIRQ will be asserted. This is a level sensitive function.
9. **VIN above V_{IN_OV} (23.5V) -** If the VIN is above V_{VIN_OV} (23.5V), the nIRQ will be asserted. This is a level sensitive function.
10. **VIN UV** - Any time the VIN is below VIN_UV threshold, the nIRQ will be asserted. This is a level sensitive function. VIN must be in the valid range AND nIRQ_CLEAR must be written to 1 for nIRQ to be de-asserted.
11. **Light Load Disable State** - Any time the device enters the LL_DIS state, the nIRQ will be asserted until the nIRQ_CLEAR Register is written to 1. The nIRQ is triggered with a “rising edge” of the LL_DIS state and does not require exiting the state to de-assert the nIRQ pin.
12. **Hiccup Mode / Vout Fault State** - Any time the device enters the HICCUP state, the nIRQ will be asserted until the nIRQ_CLEAR Register is written to 1. The nIRQ is triggered with a “rising edge” of the HICCUP state and does not require exiting the state to de-assert the nIRQ pin.

7. Protections

7.1. Thermal Shutdown

The device has thermal shutdown to disable the converter when IC junction temperature exceeds T_{SHUT} (160°C). The fault register *TSD* is set and latched when TSD fault is detected. The converter will restart automatically once the temperature of the DIE falls below the T_{SHUT_HYST} value. During this time, however, the TSD indicator register may still be latched until it is read.

7.2. FET Over Current Protection

The ACT510x closely monitors the HSFETs and LSFETs current for safe operation. If any FET exceeds the FET_ILIMIT value (8.5A or 10A), the FET will immediately be turned off for that cycle. If a FET detects the current limit for 8 continuous cycles, then the converter is latched off. This latch can be disabled by setting the *DIS_OCP_SHUTDOWN* Register. Once FET Overcurrent protection is latched, device must go back to the HIZ state to clear the Fault or set DIS_OCP_SHUTDOWN bit to 1. For example, EN pin must be toggled.

7.3. Watchdog Timer

To ensure there is not system failure, a watchdog timer is included. The timeout is controlled by *WATCHDOG[1:0]* Register 0x01 [1:0[. The settings from 40sec to 160sec allow a wide range of timeout. It can also be disabled, such as for stand-alone operation with the *WATCHDOG[1:0]*=00.

If the watchdog timer is enabled, the *WATCHDOG_RESET* needs to be written to a 1 before the timer times out. Note the WATCHDOG_RESET is an auto-clearing register. If it is written to 1, it will automatically reset back to 0.

WATCHDOG is always disabled in HIZ Mode and cannot be enabled in HIZ. In addition, the reset counter is reset to 0 when entering HIZ mode and automatically restarted when exiting HIZ mode into regulation mode.

8. System ADC Monitor

The ACT510x includes an A2D Converter to provide various system parameters during the modes of operation.

The A2D Inputs are the following:

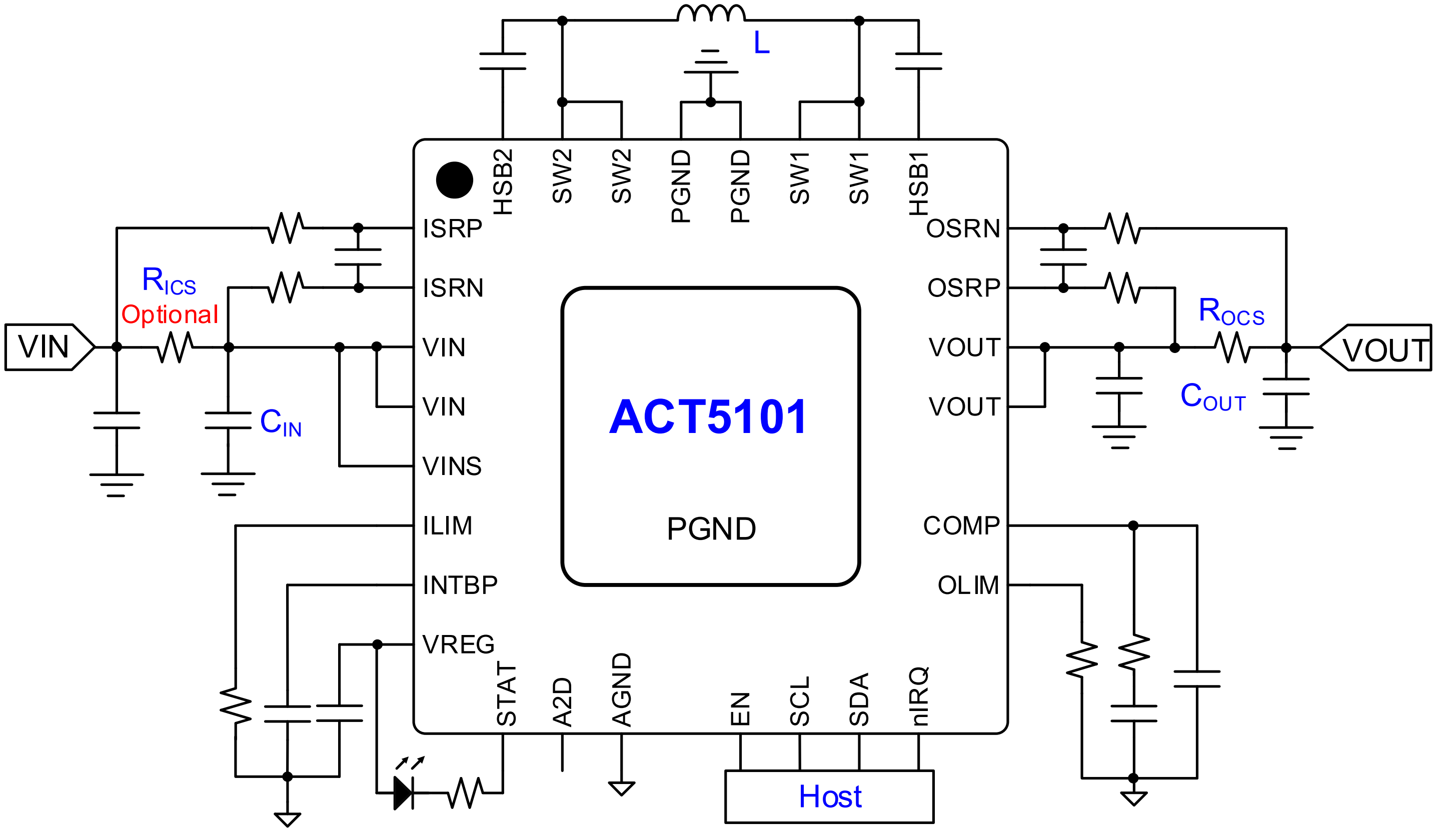
Channel	Channel Description	ADC_CH_CONV[2:0]	ADC_CH_READ[2:0]	Value
CH0	Output Current (OLIM)	000	000	I_{IN} = (DOUT-2048)/(65000*R_{CS_IN})
CH1	Output Voltage (VOUT)	001	001	V_{IN} = 0.02035*(DOUT-2048)
CH2	Input Current (ILIM)	010	010	I_{OUT} = (DOUT-2048)/(65000*R_{CS_OUT})
CH3	Input Voltage (VIN)	011	011	V_{OUT} = 0.02035*(DOUT-2048)
CH4	TH	100	100	V_{TH} = 0.003053*(DOUT-2048)
CH5	Die Temperature	101	101	T_J = 0.2707*DOUT - 809.49
CH6	ADC Input	110	110	V_{ADC} = 0.001527*(DOUT-2048)

9. PFM/PWM Operation

At light load, ACT510x operates in the PFM (pulse skipping) mode to save the switching power loss. The PFM can be disabled by the register bit.

APPLICATION

Application Schematics



I2C REGISTER

Basic I²C Registers Summary

Reg	Register Name	Type	R/W	Description	Default
0x00	Master Control 1	VM	R/W	Configure various device options	00
0x01	Master Control 2	NVM	R/W		00
0x02	General Status 1	VM	R	Device status	00
0x03	Charger Status 2	VM	R	Charger status	00
0x04	RFU	VM	R		00
0x05	Fault 1	VM	R	Device Faults	00
0x06	Fault 2	VM	R		00
0x07	ADC Output 1	VM	R	ADC Output	00
0x08	ADC Output 2	VM	R		00
0x09	ADC Configuration 1	VM	R/W	ADC configuration bits	00
0x0A	ADC Configuration 2	VM	R/W		00
0x0B	VREG Input	NVM	R/W	Configure VREG Input Source	
0x0C	RFU	NVM	R/W		
0x0D	RFU	NVM	R/W		
0x0E	Converter Control 1	NVM	R/W	Configure Converter Operation	
0x0F	Converter Control 2	NVM	R/W		
0x10	Converter Control 3	NVM	R/W		
0x11	VREG Voltage	NVM	R/W	5bit, 2.0 ~ 5.1V, LSB = 100mV, Default = 5V	
0x12	RFU	NVM	R/W		
0x13	Output Voltage 1	NVM	R/W	11-bit, 3.6 ~ 24.07V, LSB = 10mV, Default = 5V	
0x14	Output Voltage 2	NVM	R/W		
0x15	RFU	NVM	R/W		
0x16	RFU	NVM	R/W		
0x17	Output Current Limit	NVM	R/W	7-bit, 0 ~ 100%, LSB = 1%, Default = 100%	
0x18	RFU	NVM	R/W		
0x19	RFU	NVM	R/W		
0x1A	VIN UV OFFSET	NVM	R/W		

0x1B	RFU	NVM	R/W		
0x1C	RFU	NVM	R/W		
0x1D	Frequency	NVM			
0x1E	IRQ Control 1	VM	R/W	IRQ Mask Control	
0x1F	IRQ Control 2	VM	R/W		
0x20	IRQ Control/ Converter Status	VM	R	IRQ Mask Control / Converter Status	
0x21	Device ID	NVM	R	Device ID and CMI numbers	

REG 0x00: Main Control 1 (R/W) (VM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*HIZ*	0	Y	**0: Not in HIZ mode** 1: In HIZ mode	Bit to control if IC is in HIZ mode.
6	*RFU*	0	Y		
5	*RFU*	0	Y		
4	*RFU*	0	Y		
3	*RFU*	0	Y		
2	*WATCHDOG_RESET*	0	Y	**0: Normal** 1: Reset	I2C Watchdog Timer Reset This must be written to 1 before Watchdog timer expires, if Watchdog timer is enabled. This is auto clearing when writing to a 1.
1	*Audio Frequency Limit*	0	Y	**0: No limit** 1: Minimum 40kHz	0: No limit of switching frequency 1: Set minimum switching frequency to 40kHz to avoid audio noise
0	*REGISTER_RESET*	0	NA	1: Reset Registers to Default	Register is self-clearing. Write to 1 resets registers and set reset register back to 0.

REG 0x01: Main Control 2 (R/W) (NVM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*RFU*	1	Y		
6	*DIS_OCP_SHUTDOWN*	1	Y	0: Enable 1: Disable	If set to 0, the device will be disabled if FET cycle by cycle current limit is detected for 8 (or 16) continuous cycles. Uses the *FET_LIMIT* register setting for the FET ILIM.
5	*DIS_VIN_OVP*	0	Y	0: Enable 1: Disable	When set to 1, a VIN_OVP fault does not latch off the charger in a fault mode. Charger will restart automatically when the OVP condition is removed.
4	*FET_ILIMIT*	1	Y	0: 8.5A 1: 10A	This is the cycle by cycle current limit setting for ALL FETS in any operating mode:

3	*VOUT_OV_RESTART _DELAY*	0	Y	0: 40ms 1: 100usec	Delay time to restart in charger mode after Output OV fault has been removed
2	*VREG_DIS*	1	Y	0: Turn on VREG 1: Turn off VREG	Control VREG on/off Default is on.
1	*WATCHDOG[1]*	0	Y	00: Disable timer 01: 40s 10: 80s 11: 160s	I2C Watchdog Timer Setting Watchdog timer is always disabled and reset to 0 in HIZ Mode. When Disabled, Watchdog timer is also reset to 0.
0	*WATCHDOG[0]*	0	Y		

REG 0x02: General Status 1 (Read Only) (VM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*RFU*	NA	NA		
6	*nIRQ_PIN_Status*	NA	NA	0: Our device output drive HIZ 1: Our device output asserted Low	Device status of IRQ output Not actual status of the IRQ pin – Open drain output so other devices could be driving the pin low in a wired OR configuration
5	*EN_PIN_STATUS*	NA	NA	0: EN Pin Low 1: EN Pin High	Real time status of the EN pin
4	*RFU*	NA	NA		
3	*RFU*	NA	NA		
2	*RFU*	NA	NA		
1	*OPERATION_MODE[1]*	NA	NA	00: HIZ Mode 01: not valid 10: Operation Mode 11: not valid	Current state machine status for overall system.
0	*OPERATION_MODE[0]*	NA	NA		

REG 0x03: General Status 2 (Read only) (VM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment

7	*RFU*	NA	NA		
6	*THERMAL_ACTIVE*	NA	NA	0: Not in thermal regulation 1: Thermal regulation Active	Thermal Regulation Active
5	*RFU*	NA	NA		
4	*RFU*	NA	NA		
3	*RFU*	NA	NA		
2	*RFU*	NA	NA		
1	*RFU*	NA	NA		
0	*RFU*	NA	NA		

REG 0x04: RFU (Read Only) (VM)

REG 0x05: Faults 1 (Read only) (VM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*nIRQ_Clear*	0	NA	0: Normal Status 1: Clear IRQ output	Write this bit to 1 to clear the IRQ output. The bit will self-clear to a 0 once the write occurs. If a fault still occurs, then nIRQ pin may stay asserted low. Register 0x02 Bit 6 provides a real time status of the nIRQ output.
6	*RFU*	NA	NA		
5	*RFU*	NA	NA		
4	*VREG_OC_UVLO*	NA	NA	0: No Fault 1: VREG OC	VREG_LDO Overcurrent. Read to clear this latching fault bit. The fault mask bits *DIS_VREG_FLT* registers do not affect this fault bit. It will always get indicated here to notify the user. Note: There is a 100msec restart delay for OC faults on the VREG LDO, so the delay must expire before this bit can be reset with a read to clear.

3	*TSD*	NA	NA	0: No Fault 1: Over Temperature	Die Thermal Shutdown. Read to Clear latch Bit.
2	*FET_OC*	NA	NA	0: No Fault 1: Input OC	FET Overcurrent. Read to Clear latching Bit.
1	*RFU*	NA	NA		
0	*RFU*	NA	NA		

REG 0x06: Faults 2 (Read only) (VM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*WATCHDOG_FAULT*	NA	NA	0: No Fault 1: Watchdog Fault	Watchdog Timeout Fault Read to clear latching bit If Watchdog is enabled, and watchdog timer times out, then this bit is set high. This does not clear the watchdog timer. The watchdog timer needs to be cleared with a watchdog read or disable the watchdog timer. If this bit is read and the watchdog timer has not been reset, then this bit will immediately go high again after the read.
6	*VOUT_FAULT*	NA	NA	0: No Fault 1: VOUT Fault	Output Hiccup Mode Fault, read to clear latching bit. If the VOUT enters hiccup state because current exceeds the Constant Current Mode, then this bit gets set. This register will always be set during hiccup mode when VOUT is off during the 3sec restart time and converter is in the HICCUP state. After it exits this state, this bit can be cleared with a read.
5	*VIN_UV_FLT*	NA	NA	0: Not Fault 1: VIN UV Fault	VIN UV Fault. Read to Clear latching bit If VIN falls below the V_{IN_UV} Voltage specified in the VIN_UV Register (Reg 0x0F, Bits 7:5) The input voltage must be above the VIN_UV voltage and then a read will clear this fault bit.
4	*VOUT_OV*	NA	NA	0: Not Fault 1: VOUT OV Fault	Vout Overvoltage Fault, Read to Clear latching bit This bit will be set any time the Vout exceeds the OV threshold for external or internal feedback. The VOUT must be below the OV voltage and then a read will clear this fault bit.
3	*LIGHT_LOAD*	NA	NA	0: Not Fault 1: Converter Off	Output Light Load State Latch, read to clear latching bit Converter has been disabled because of light load condition on output and it entered the LL_DIS state. The

					device must exit the LL_DIS state, and then a read will clear this bit.
2	*VIN_OV*	NA	NA	0: Not Fault 1: VIN OV	VIN Overvoltage fault, Read to clear latching bit. This bit will be set any time the VIN exceeds the OV threshold. The VIN must be below the OV voltage and then a read will clear this fault bit.
1	*I2C_FAULT*	NA	NA	0: Not Fault 1: I2C Fault	If set to 1, I2C command did not finish correctly or errors on I2C data
0	*RFU*	NA	NA		

REG 0x07: ADC Output 1 (Read only) (VM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*ADC_OUT[13]/[7]*	0	Y		Selected data output from *ADC_READ* Register ADC output Upper 8 Bits of ADC output. If only 8 Bits are used, then [7:0] If all 14 Bits are used, then [13:6]
6	*ADC_OUT[12]/[6]*	0	Y		
5	*ADC_OUT[11]/[5]*	0	Y		
4	*ADC_OUT[10]/[4]*	0	Y		
3	*ADC_OUT[9]/[3]*	0	Y		
2	*ADC_OUT[8]/[2]*	0	Y		
1	*ADC_OUT[7]/[1]*	0	Y		
0	*ADC_OUT[6]/[0]*	0	Y		

REG 0x08: ADC Output 2 (Read only) (VM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*RFU*	0	Y		Selected data output from *ADC_READ* Register Lower 6 LSB Bits of ADC Output
6	*RFU*	0	Y		
5	*ADC_OUT[5]*	0	Y		
4	*ADC_OUT[4]*	0	Y		

3	*ADC_OUT[3]*	0	Y		
2	*ADC_OUT[2]*	0	Y		
1	*ADC_OUT[1]*	0	Y		
0	*ADC_OUT[0]*	0	Y		

REG 0x09: ADC Configuration 1 (R/W) (VM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*EN_ADC*	0	Y	0: ADC disabled 1: ADC enabled	
6	*ADC_ONE_SHOT*	0	Y	0: ADC continually converts data when EN_ADC=1 1: ADC performs a one-time conversion when EN_ADC=1	[ADC ONE SHOT][ADC_ CH_SCAN] = XX operation is described as below. 00 = Scan channel specified by ADC CHANNEL CONVERSION [2:0] register bits repeatedly in a loop. 01 = Scan and convert channels 0 – 7 repeatedly in a loop. 10 = Convert channel specified by ADC CHANNEL CONVERSION [2:0] once (one shot) 11 = Scan and convert channels 0 – 7 once and stop – one loop
5	*ADC_CH_SCAN*	0	Y	0: Scan single channel specified by ADC_CH_CONV 1: Scan all channels	
4	*DIS_ADC_BUFFER*	0	Y	0: ADC Buffer is enabled 1: ADC Buffer is disabled	This should always be set to 0.
3	*ADC_SWAP*	0	Y	0: ADC Buffer is normal inputs 1: ADC Buffer swaps inputs	If very accurate measurements are required, the ADC input pair can be swapped to negate input offset errors in the Buffer AMP. This requires one read with *ADC_SWAP*=0 and one read with *ADC_SWAP*=1, then average the results.
2	*HW_DIE_REV[2]*	0	Y		
1	*HW_DIE_REV[1]*	0	Y		
0	*HW_DIE_REV[0]*	0	Y		

REG 0x0A: ADC Configuration 2 (R/W) (VM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*ADC_DATA_READY*	0	Y	0: Data not ready 1: Data is ready	Read Only - Conversion occurred and data is ready to read
6	*RFU*				
5	*ADC_CH_I2C_READ[2]*	0	Y	000 = OLIM Pin 001 = VOUT voltage Divide by 13.33 010 = VIN voltage Divide by 10 011 = ILIM Pin 100 = not valid 101 = Die temperature 110 = EXT Pin voltage 111 = AGND voltage	This controls the current A2D register to output on the I2C register. The A2D can provide an I2C read on a different register while processing / converting another channel.
4	*ADC_CH_I2C_READ[1]*	0	Y		
3	*ADC_CH_I2C_READ[0]*	0	Y		
2	*ADC_CH_CONV [2]*	0	Y	000 = OLIM Pin 001 = VOUT voltage Divide by 13.33 010 = VIN voltage Divide by 10 011 = ILIM Pin 100 = not valid 101 = Die temperature 110 = EXT Pin voltage 111 = AGND voltage	This controls the current A2D conversion processing channel. The A2D can provide an I2C read on a different register while processing /converting another channel.
1	*ADC_CH_CONV [1]*	0	Y		
0	*ADC_CH_CONV [0]*	0	Y		

REG 0x0B: VREG Input (R/W) (NVM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*RFU*	1	Y		
6	*RFU*	0	Y		
5	*RFU*	0	Y		

4	*RFU*	0	Y		
3	*RFU*	0	Y		
2	*RFU*	0	Y		
1	*VREG_OVERRIDE*	0	Y	0: Automatic Control 1: Manual Control	0: Device automatically selects the correct supply to use 1: VREG uses the *VREG_SELECT* register to select the power input
0	*VREG_SELECT*	0	Y	0: VOUT Supply 1: VIN Supply	VREG powered from VIN or VOUT PIN

REG 0x0C: RFU (R/W) (NVM)

REG 0x0D: RFU (R/W) (NVM)

REG 0x0E: Converter Control 1 (R/W) (NVM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*EN*	1	Y	0: Disable 1: Enable	If this bit is low, converter is always disabled. If this bit is High, then either the EN pin or the EN_ OVERRIDE bit will enable the converter. In addition, the HIZ mode bit (Reg 0x00, bit 0) must be low.
6	*EN_OVERRIDE*	1	Y	0: Disable 1: Enable	If this bit is high, EN is over written and converter is enabled, if EN bit is high. This allows user to enable converter from I2C without using the PIN.
5	*SOFT START[1]*	1	Y	00: 0.2 ms 01: 1 ms 10: 3 ms 11: 10 ms	Soft start time for output voltage.
4	*SOFT START [0]*	1	Y		
3	*OFF_DLY[1]*	1	Y	00: Disable 01: 10 s 10: 20 s 11: 30 s	When light load is detected for the setting time, the converter is disabled and latched off. The converter must be disabled and re-enabled to turn back on. This can be done with the EN Pin, or through the EN register bit.
2	*OFF_DLY[0]*	1	Y		
1	*OFF_LOAD*	1	Y	0: 1 mA	This threshold is used to enable the timer for the OFF Delay during light load conditions in BUCK Mode Only,

				1: 5 mA	when $V_{IN} > V_{OUT} + 0.5V$
0	*OFF_LOAD_EN*	0	Y	0: Disable 1: Enable	Enable the disable with light load function. When not in BUCK mode, feature is always disabled.

REG 0x0F: Converter Control 2 (R/W) (NVM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*VIN_UV[2]*	1	Y	000: $V_{IN\_UV\_OFFSET}$ 001: $V_{IN\_UV\_OFFSET}$ -0.2V 010: $V_{IN\_UV\_OFFSET}$ -0.4V 011: $V_{IN\_UV\_OFFSET}$ -0.6V 100: $V_{IN\_UV\_OFFSET}$ -0.8V 101: $V_{IN\_UV\_OFFSET}$ -1.0V 110: $V_{IN\_UV\_OFFSET}$ -1.2V 111: $V_{IN\_UV\_OFFSET}$ -1.4V	VIN UV threshold for converter to operate. Referenced from $V_{IN\_UV\_OFFSET}$ level.
6	*VIN_UV [1]*	1	Y		
5	*VIN_UV [0]*	1	Y		
4	*EN_ STAT*	0	Y	0: Disable 1: Enable	If EN_STAT bit is 1, device will pull STAT pin low to indicate the converter is running. If converter is disabled for any reason, such as VOUT fault or VIN UV, etc, STAT will go high. If set to 0, STAT will always be HI-Z.
3	*CORD_COMP[1]*	1	Y	00: Disable 01: 100mV 10: 200mV 11: 300mV	Cord Compensation at 2.4A Load with 10mOhm Resistor (20mOhm resistor as option)
2	*CORD_COMP[0]*	0	Y		
1	*EN_DLY[1]*	0	Y	00: 0 ms 01: 200 ms 10: 500 ms 11: 1 s	The delay before enabling the converter from the EN pin or EN register bit.
0	*EN_DLY[0]*	1	Y		

REG 0x10: Converter Control 3 (R/W) (NVM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*OUTPUT_SLEW[1]*	1	Y	00: 1V/ms	If converter is set to internal feedback and output voltage is changed using the VOUT register for QC2.0/3.0 or

6	*OUTPUT_SLEW[0]*	1	Y	01: 0.5V/ms 10: 0.33V/ms 11: 0.1V/ms	USB PD voltage ramp, this register controls the rate at which the output voltage will change.
5	*PULLDOWN_RAMP*	1	Y	0: Disable 1: Enable	If RAMP_PULLDOWN is set to 1 and OUTPUT_I2C is set to 0 for internal feedback, an internal current source will pulldown on the output during a ramp down of the output voltage. This will allow the output to meet the QC 2.0/3.0 and USB PD ramp timing requirements.
4	*PULLDOWN_OV*	1	Y	0: Disable 1: Enable	If PULLDOWN_OV is set to 1, the pulldown current source will pulldown on the output during any OV condition on the output.
3	*INPUT_ILIM[1]*	1	Y	00: Disable 01: 150% of ILIM 10: 200% of ILIM 11: 300% of ILIM	Input current limit proportional to the ILIM current setting. Measured on the ISRP and ISRN pins and set by the ILIM Resistor
2	*INPUT_ILIM[0]*	0	Y		
1	*DIS_ VREG_FLT*	0	Y	0: Enable 1: Disable	If set to 0, an overcurrent or UVLO fault on the VREG will stop converter. If set to 1, converter will continue with fault on VREG.
0	*DIS_PFM*	0	Y	0: Enable 1: Disable	Disable PFM mode to reduce switching noise and follow a force PMW Mode

REG 0x11: VREG Voltage (R/W) (NVM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*VREG[4]*	1	Y	1600mV	VREG LDO Output Voltage Offset: 2V Range: 2V (00000) - 5.1V (11111)
6	*VREG[3]*	1	Y	800mV	
5	*VREG[2]*	1	Y	400mV	
4	*VREG[1]*	1	Y	200mV	
3	*VREG[0]*	0	Y	100mV	
2	*RFU*	1	Y		
1	*RFU*	1	Y		

0	*RFU*	0	Y		

REG 0x12: RFU (R/W) (NVM)

REG 0x13: Output Voltage 1 (R/W) (NVM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*RFU*	1	Y		
6	*RFU*	0	Y		
5	*RFU*	1	Y		
4	*RFU*	1	Y		
3	*VOUT_I2C*	0	Y	0: I2C Register 1: External Resister Divider using FB	When set to 0, internal resistor divider network is used and controlled by VOUT registers. When set 1, external resistor divider connected to FB is used to control the output.
2	*RFU*	0	Y		
1	*VOUT[9]*	0	Y	10240 mV	Internal divider network Offset: 2.96V Range: 2.96V (000_0000_0000) to 23.42V (111_1111_1111)
0	*VOUT[8]*	0	Y	5120 mV	

REG 0x14: Output Voltage 2 (R/W) (NVM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*VOUT[7]*	1	Y	2560 mV	Internal divider network Offset: 2.96V Range: 2.96V (000_0000_0000) to 23.42V (111_1111_1111)
6	*VOUT[6]*	0	Y	1280 mV	
5	*VOUT[5]*	1	Y	640 mV	
4	*VOUT[4]*	1	Y	320 mV	
3	*VOUT[3]*	0	Y	160 mV	

2	*VOUT[2]*	1	Y	80 mV	
1	*VOUT[1]*	0	Y	40 mV	
0	*VOUT[0]*	0	Y	20 mV	

REG 0x15: RFU (R/W) (NVM)

REG 0x16: RFU (R/W) (NVM)

REG 0x17: Output Current Limit (R/W) (NVM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*DIS_CC*	0	Y	0: Enable 1: Disable	Set 1 to disable the output constant current limit function.
6	*CC[6]*	1	Y	64%	Output Current Percentage of OLIM Resistor Setting. Range: 1% (000_0001) to 100% (110_0100) Setting 110_0100 to 111_1111 = 100% Setting 000_0000 to 000_0001 = 1%
5	*CC[5]*	1	Y	32%	
4	*CC[4]*	0	Y	16%	
3	*CC[3]*	0	Y	8%	
2	*CC[2]*	1	Y	4%	
1	*CC[1]*	0	Y	2%	
0	*CC[0]*	0	Y	1%	

REG 0x18: RFU (R/W) (NVM)

REG 0x19: RFU (R/W) (NVM)

REG 0x1A: VIN UV OFFSET (R/W) (NVM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment

7	*RFU*	0			
6	*VIN_UV_OFFSET[6]*	0	Y	6400 mV	Input UV offset voltage Offset: 5V Range: 5V (0000000) ~ 15.2V (1111111)
5	*VIN_UV_OFFSET [5]*	0	Y	3200 mV	
4	*VIN_UV_OFFSET [4]*	0	Y	1600 mV	
3	*VIN_UV_OFFSET [3]*	0	Y	800 mV	
2	*VIN_UV_OFFSET [2]*	0	Y	400 mV	
1	*VIN_UV_OFFSET [1]*	0	Y	200 mV	
0	*VIN_UV_OFFSET [0]*	0	Y	100 mV	

REG 0x1B: RFU (R/W) (NVM)

REG 0x1C: RFU (R/W) (NVM)

REG 0x1D: FREQUENCY (R/W) (NVM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*FREQ_SEL[1]*	1	Y	Frequency Selection Settings for SMPS 00: 125kHz 01: 250kHz 10: 500kHz 11: 1MHz	Operation Frequency Settings **Note:** These can NOT be changed "on the fly" and each setting requires a different inductor value and capacitors and compensation components. **CARE SHOULD BE TAKEN WHEN WRITING TO THIS REGISTER TO AVOID CHANGING THE FREQUENCY WHILE OPERATING**
6	*FREQ_SEL[0]*	0	Y		
5	*RFU*				
4	*RFU*	0	Y		
3	*RFU*	1	Y		
2	*RFU*	0	Y		
1	*TREG[1]*	1	Y	00: Disable 01: 80°C 10: 100°C	Die temperature regulation threshold
0	*TREG[0]*	1	Y		

				11: 120°C	

REG 0x1E: IRQ Control 1 R/W (NVM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*RFU*	1	Y		
6	*RFU*	1	Y		
5	*RFU*	1	Y		
4	*nIRQ_VIN_UVOV*	0	Y	0: VIN UV or OV on nIRQ 1: Masks nIRQ	If set to 0, a VIN below UV or VIN OV will active the nIRQ Pin Setting to 1, masks the fault to nIRQ
3	*RFU*	1	Y		
2	*RFU*	1	Y		
1	*nIRQ_VREG_FLT*	0	Y	0: VREG LDO Overcurrent or Undervoltage indicated on nIRQ 1: Masks nIRQ	If set to 0, a VREG LDO Overcurrent or Undervoltage will active the nIRQ pin Setting to 1, masks the fault to nIRQ
0	*nIRQ_TSD*	0	Y	0: Device Thermal Shutdown indicated on nIRQ 1: Masks nIRQ	If set to 0, a device Thermal Shutdown will active the nIRQ pin Setting to 1, masks the fault to nIRQ

REG 0x1F: IRQ Control 2 R/W (NVM)

Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*nIRQ_FET_OC*	0	Y	0: FET Overcurrent triggers nIRQ pin 1: Masks nIRQ	If set to 0, a FET Overcurrent condition will active the nIRQ pin Setting to 1, masks FET Overcurrent states to nIRQ
6	*nIRQ_Watchdog*	0	Y	0: Watchdog timer expired triggers nIRQ	If set to 0, a watchdog timeout will active the nIRQ pin

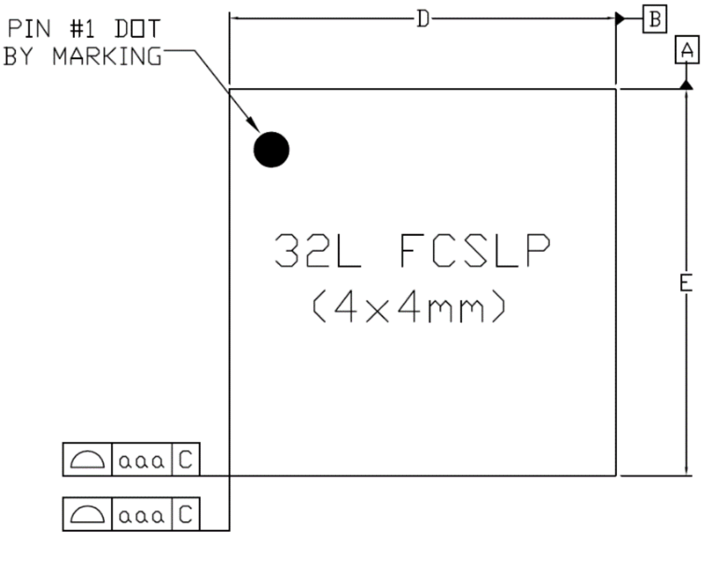
				1: Masks nIRQ	Setting to 1, masks the fault nIRQ
5	*nIRQ_HICCUP*	0	Y	0: Converter enter Hiccup state nIRQ 1: Masks nIRQ	If set to 0, converter entering hiccup state will active the nIRQ pin Setting to 1, masks hiccup mode to nIRQ
4	*nIRQ_LL*	0	Y	0: Converter enter Light Load state on nIRQ 1: Masks nIRQ	If set to 0, converter entering Light Load Disable state will active the nIRQ pin Setting to 1, masks light load disable state to nIRQ
3	*nIRQ_A2D_DATA*	0	Y	0: A2D Data Ready 1: Masks A2D Data Ready nIRQ	If set to 0, a rising edge on A2D Data Ready will active the nIRQ pin Setting to 1, masks the A2D Data Ready to nIRQ
2	*nIRQ_HIZ*	0	Y	0: Enter HIZ Mode 1: Masks Enter HIZ Mode nIRQ	If set to 0, a rising edge when entering HIZ State will active the nIRQ pin Setting to 1, masks the HIZ Enter to nIRQ
1	RFU	1	Y		
0	*RFU*	1	Y		

REG 0x20: IRQ / Converter Status (R/W) (VM)

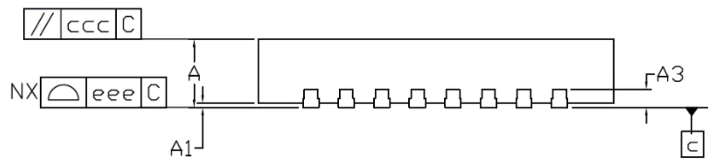
Bit	Name	Default Value	Reset by REG_RST	Description	Comment
7	*nIRQ_I2C_ERROR*	0	Y	0: I2C Fault 1: Masks I2C Fault nIRQ	If set to 0, a fault on the I2C command / I2C bus will active the nIRQ Pin Setting to 1, masks the nIRQ
6	*INPUT_CC*	NA	NA	0: Input not in current limit 1: Input is regulating in Constant Current Mode	Real Time status This is the current measured on the VIN side using ISRP and ISRN controlled by the *VIN_ILIM* Register
5	*OUTPUT_CC*	NA	NA	0: Output regulating using voltage loop 1: Output is regulating in Constant Current Mode	Real Time status This is the current measured on the VOUT side using OSRP and OSRN controlled by the *CC* Register
4	*VIN_UV*	NA	NA	0: VIN above VIN_UV 1: VIN below VIN_UV	Real time status – For latched fault, see the Fault Registers
3	*VIN_OV*	NA	NA	0: VIN below OV 1: VIN above OV	Real time status – For latched fault, see the Fault Registers

2	*STATUS[2]*	NA	NA	000: RST 001: SS 010: REG 011: HICCUP 100: LL_DIS	State machine for converter status 101 – 111: Not Valid
1	*STATUS[1]*	NA	NA		
0	*STATUS[0]*	NA	NA		

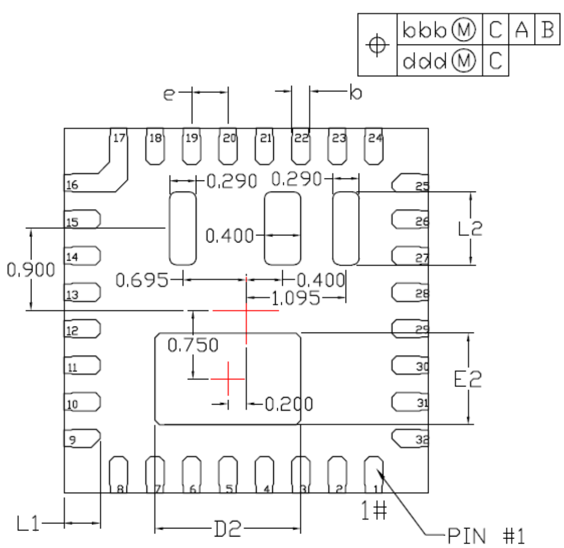
PACKAGE OUTLINE AND DIMENSIONS QFN4X4-32



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	---	---	0.050
A3	0.203 Ref.		
D	3.950	4.000	4.050
E	3.950	4.000	4.050
D2	1.550	1.600	1.650
E2	0.950	1.000	1.050
	--		
b	0.150	0.200	0.250
e	0.400 BSC		
L1	0.350	0.400	0.450
L2	0.750	0.800	0.850
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

All dimensions are in millimeters
Dimensioning and tolerancing per JEDED MO-232
See Active Semi Application note AN-104, QFN PCB Layout Guidelines for more information on generating the ACT510x land pattern.