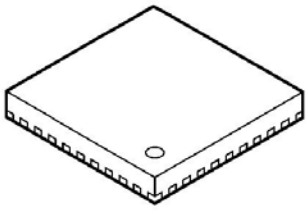
TOSHIBA Bi-CD Integrated Circuit Silicon Monolithic

TB67Z800FTG

3-channel Half Bridge Driver

The TB67Z800FTG incorporates 3-channel half bridge driver. It can control all channels independently.



P-VQFN36-0505-0.50-001

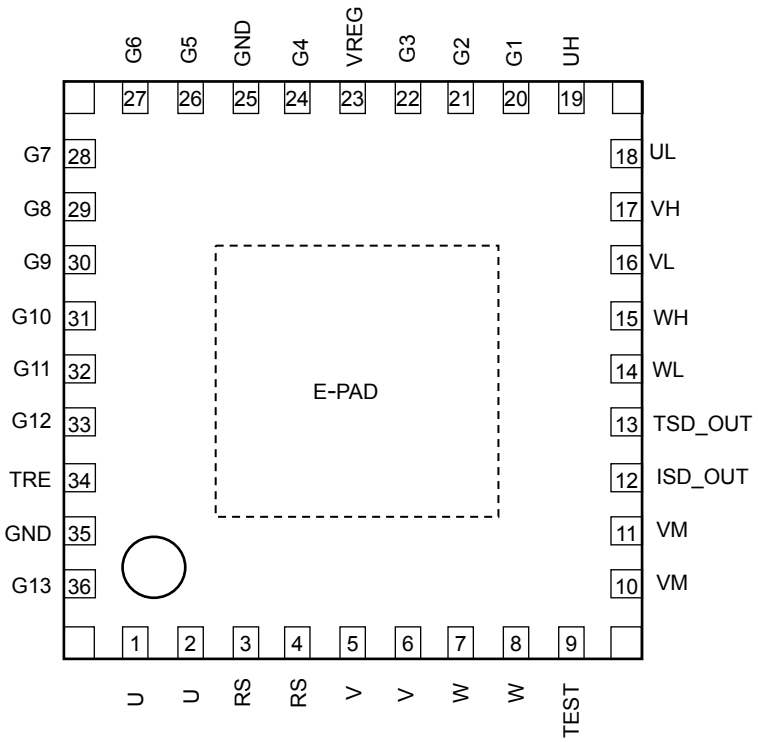
Weight: 0.05 g (typ.)

Features

- Output current: Absolute maximum rating: 3A
- Power supply: VM = 4.0 V to 22 V (Absolute maximum rating: 25 V)
- Over current protection (ISD)
- Thermal shutdown (TSD)
- Under voltage lockout (UVLO)
- Dead time for preventing shoot-through current

Pin Assignment

Top view



Note 1: Design the pattern in consideration of the heat design because the back side (E-PAD (3.4mm × 3.4mm)) and the four corners of the PAD have the role of heat radiation. (The back side (E-PAD) and the four corners of the PAD should be connected to GND because they are connected to the back of the chip electrically.)

Note 2: Because each U, V, W, RS, and VM has two pins, short out these two pins at the external pattern respectively.

Pin Description

Pin No.	Symbol	I/O	Description
1	U	O	U-phase output
2	U	O	U-phase output
3	RS	—	Connection pin for output current detecting resistance
4	RS	—	Connection pin for output current detecting resistance
5	V	O	V-phase output
6	V	O	V-phase output
7	W	O	W-phase output
8	W	O	W-phase output
9	TEST	—	Connect to GND pin
10	VM	—	Motor power supply pin
11	VM	—	Motor power supply pin
12	ISD_OUT	O	ISD detecting signal output pin (open-drain)
13	TSD_OUT	O	TSD detecting signal output pin (open-drain)
14	WL	I	W-phase low side control pin
15	WH	I	W-phase high side control pin
16	VL	I	V-phase low side control pin
17	VH	I	V-phase high side control pin
18	UL	I	U-phase low side control pin
19	UH	I	U-phase high side control pin
20	G1	—	Connect to GND pin
21	G2	—	Connect to GND pin
22	G3	—	Connect to GND pin
23	VREG	—	Reference voltage output
24	G4	—	Connect to GND pin
25	GND	—	Ground connection pin
26	G5	—	Connect to GND pin
27	G6	—	Connect to GND pin
28	G7	—	Connect to GND pin
29	G8	—	Connect to GND pin
30	G9	—	Connect to GND pin
31	G10	—	Connect to GND pin
32	G11	—	Connect to GND pin
33	G12	—	Connect to GND pin
34	TRE	—	Connection pin for a capacitor to set the ISD recovery time
35	GND	—	Ground connection pin
36	G13	—	Connect to GND pin

Functional Description

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes. Timing charts may be simplified for explanatory purposes.

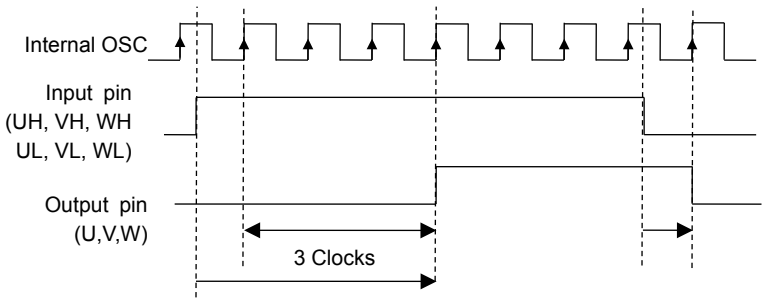
1. Function table

Mode	UH	UL	U
Normal	L	L	Hi-Z
	L	H	L
	H	L	H
	H	H	Hi-Z
ISD ON	X	X	Hi-Z
TSD ON	X	X	Hi-Z
UVLO ON	X	X	Hi-Z

Mode	VH	VL	V
Normal	L	L	Hi-Z
	L	H	L
	H	L	H
	H	H	Hi-Z
ISD ON	X	X	Hi-Z
TSD ON	X	X	Hi-Z
UVLO ON	X	X	Hi-Z

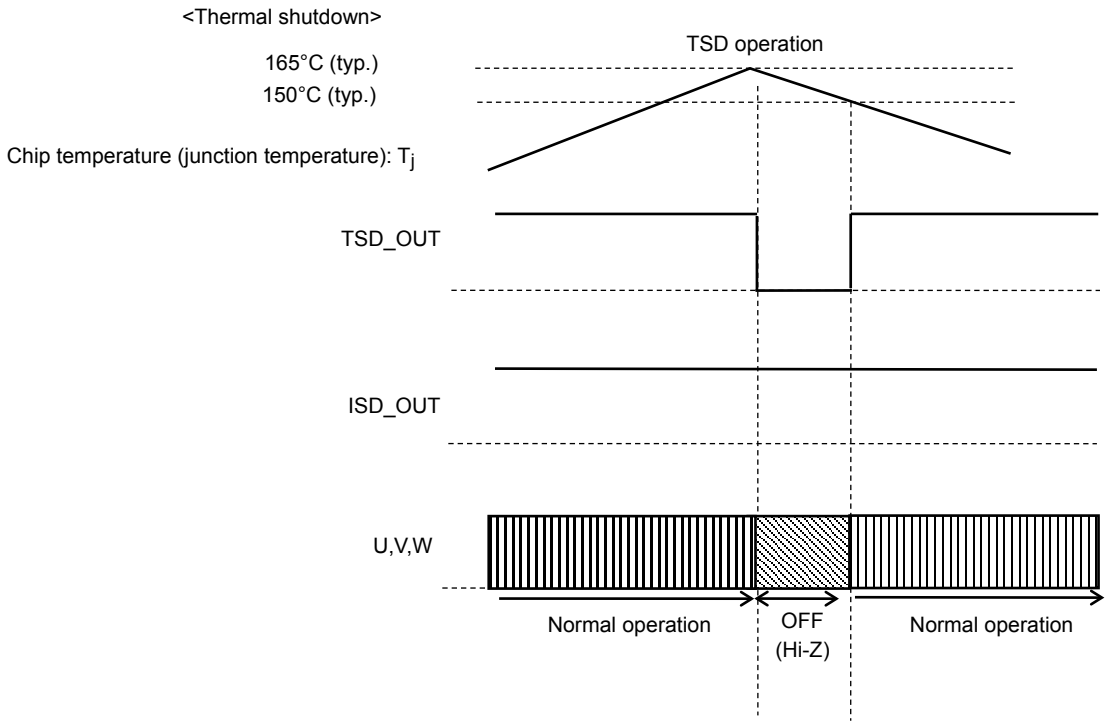
Mode	WH	WL	W
Normal	L	L	Hi-Z
	L	H	L
	H	L	H
	H	H	Hi-Z
ISD ON	X	X	Hi-Z
TSD ON	X	X	Hi-Z
UVLO ON	X	X	Hi-Z

The output logic change synchronizes with the OSC clocks. When the voltage of the input logic changes from low level to high level, the voltage of the output pin changes after 3 clocks of the OSC to avoid cross conduction. OSC frequency: 9 MHz±30%



2. Thermal Shutdown (TSD) Circuit

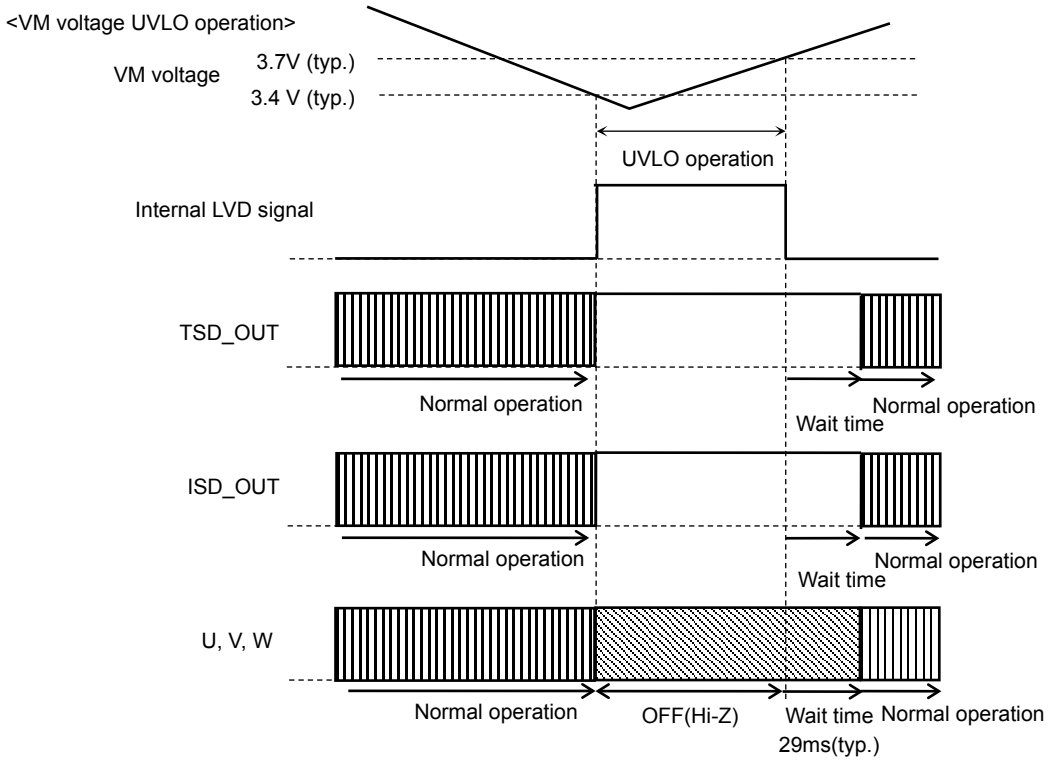
The TB67Z800FTG incorporates a thermal shutdown circuit. When the junction temperature (T_j) exceeds 165°C (typ.), the output transistors are turned off (Hi-Z).
The IC has 15°C of temperature hysteresis.

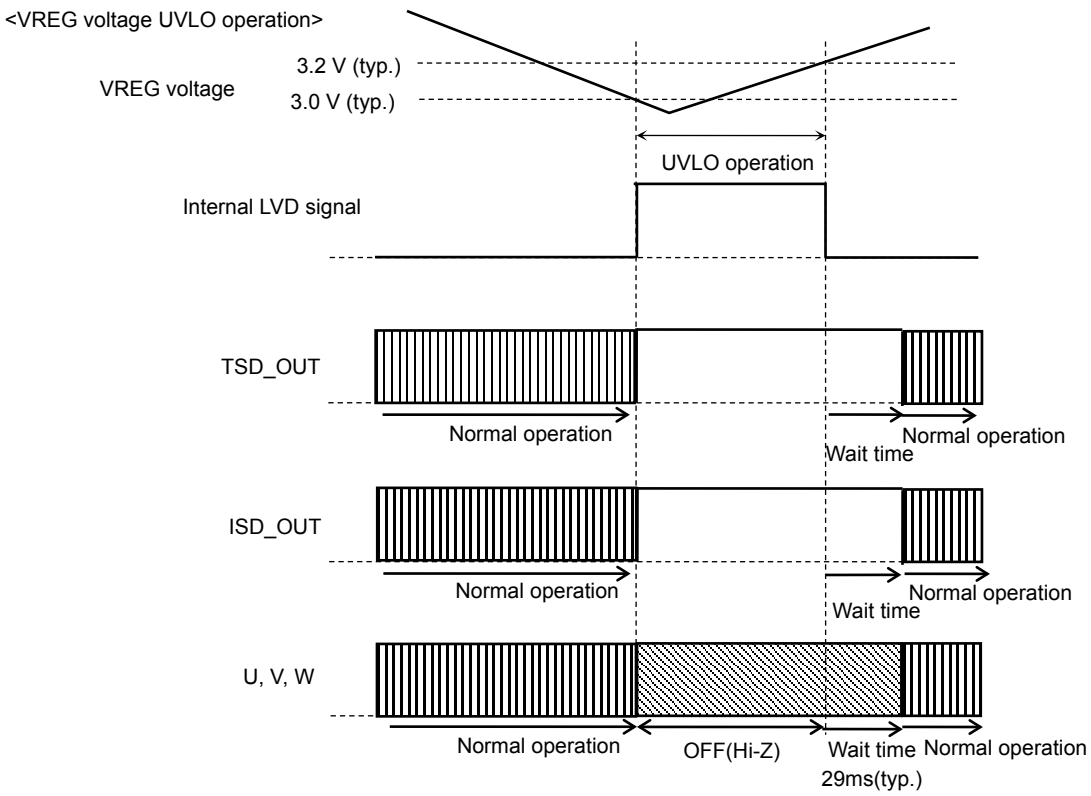


Note: The TSD circuit is activated if the absolute maximum junction temperature rating (T_j) of 150°C is violated. Note that the circuit is provided as an auxiliary only and does not necessarily provide the IC with a perfect protection from any kind of damages.

3. Under Voltage Lockout Circuit (UVLO)

The TB67Z800FTG includes an under voltage lockout circuit, which turns the control logic off to put the output transistors in the high-impedance state when VM decreases to 3.4 V (typ.) or less.
The output transistors are automatically turned on when VM increases past the lockout threshold, which is raised to 3.7 V (typ.) by a hysteresis of 0.3 V (typ.). The TB67Z800FTG turns the control logic off to put the output transistors in the high-impedance state when VREG decreases to 3.0 V (typ.) or less.
The output transistors are automatically turned on when VM increases past the lockout threshold, which is raised to 3.2 V (typ.) by a hysteresis of 0.2 V (typ.).

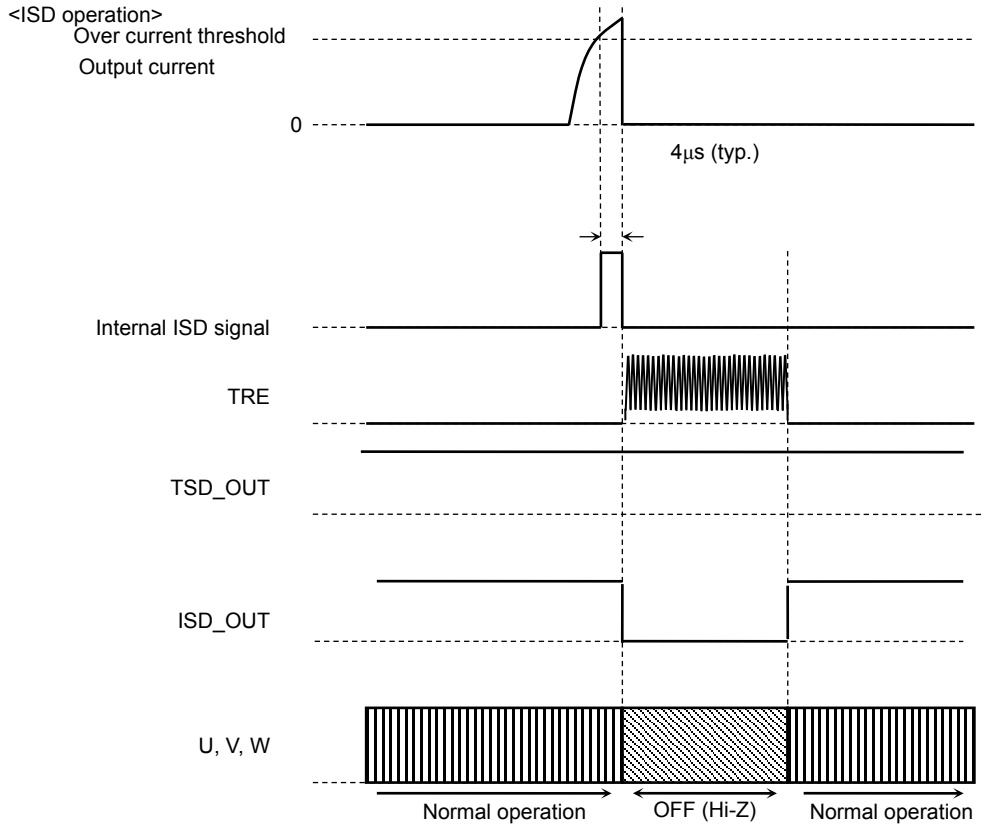



<VREG voltage UVLO operation>
VREG voltage
3.2 V (typ.)
3.0 V (typ.)
UVLO operation
Internal LVD signal
TSD_OUT
Normal operation
Normal operation
Wait time
ISD_OUT
Normal operation
Normal operation
Wait time
U, V, W
Normal operation
OFF(Hi-Z)
Wait time
29ms(typ.)
Normal operation

4. Over Current Protection (ISD) Circuit

The TB67Z800FTG incorporates the overcurrent protection circuit that monitors the current flowing through six output power transistors respectively.
If a current of between 3 A and 6 A is sensed for configured time or longer at any one of six transistors, all output transistors are turned off (Hi-Z).

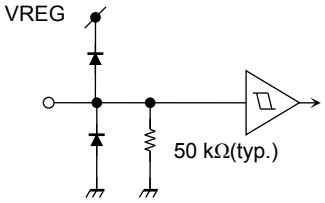
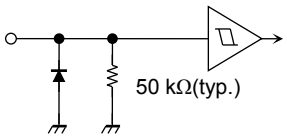
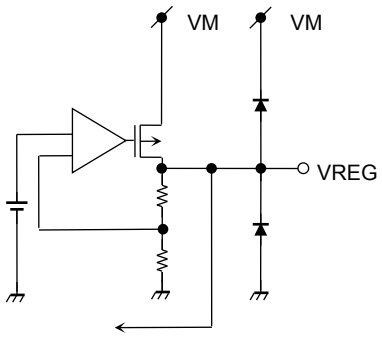
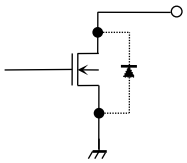
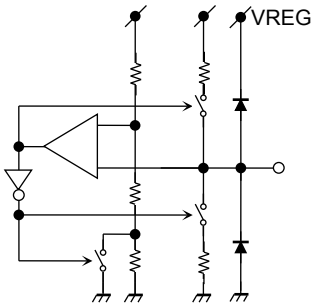
Restart term is configured by the capacitor of TRE pin as follows;
Restart term: $T = 0.313 \times 31.5 \text{ times} \times C \times 10^6$
When C = 1 μF, T ≈ 9.9 s

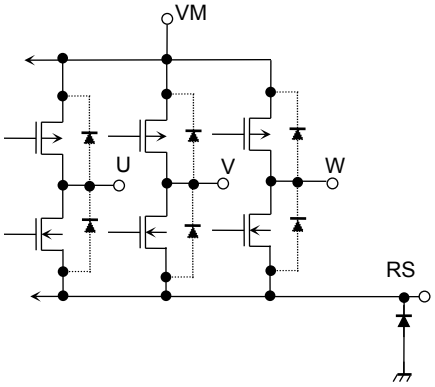


Note: The ISD circuit is activated if the absolute maximum current rating is violated. Note that the circuit is provided as an auxiliary only and does not necessarily provide the IC with a perfect protection from damages due to overcurrent caused by power fault, ground fault, load-short and the like.

I/O Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

Symbol	I/O Signal	I/O Internal Circuit
UH VL WH WL	Input H: 2 V (min) L: 0.8 V (max) When VM power supply turns off, input OFF (Low) signal. Though VM power supply turns off, when High signal is inputted, the voltage is supplied to the VM supply from VREG through the diode. It causes malfunction.	
UL VH	Input H: 2 V (min) L: 0.8 V (max)	
VREG	Reference voltage output VREG = 5 V(typ.)	
ISD_OUT TSD_OUT	Open-drain output An externally attached pull-up resistor enables the High output.	
TRE	Connection pin for a capacitor to set the ISD recovery time	

Symbol	I/O Signal	I/O Internal Circuit
VM U V W RS	U,V,W-phase output VM: Motor power supply pin RS: Connection pin for an output shunt resistor	

Absolute Maximum Ratings (Note) (Ta = 25 °C)

Characteristics	Symbol	Rating	Unit
Power supply voltage	VM	25	V
Input voltage	V_{IN1} (Note 1)	5.5	V
Output voltage	V_{OUT1} (Note 2)	25	V
	V_{OUT2} (Note 3)	25	V
Output current	I_{OUT1} (Note 4)	3 (Note 7)	A
	I_{OUT2} (Note 5)	10	mA
	I_{OUT3} (Note 6)	5	mA
Power dissipation	P_D	2.8 (Note 8)	W
Operating temperature	T_{opr}	-40 to 105	°C
Storage temperature	T_{stg}	-55 to 150	°C

Note: The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating (s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
Please use the TB67Z800FTG within the specified operating ranges.

Note 1: V_{IN1} is applicable to the voltage at the following pins: UH, UL, VH, VL, WH, and WL

Note 2: V_{OUT1} is applicable to the voltage at the following pins: U, V, and W

Note 3: V_{OUT2} is applicable to the voltage at the following pins: TSD_OUT and ISD_OUT

Note 4: I_{OUT1} is applicable to the voltage at the following pins: U, V, and W

Note 5: I_{OUT2} is applicable to the voltage at the following pins: TSD_OUT and ISD_OUT

Note 6: I_{OUT3} is applicable to the voltage at the following pin: VREG

Note 7: Output current may be limited by the ambient temperature or the device implementation.
The maximum junction temperature should not exceed T_{jmax} = 150°C

Note 8: When mounted on the board (4 layers:FR4:76.2mm x 114.3mm x 1.6mm)

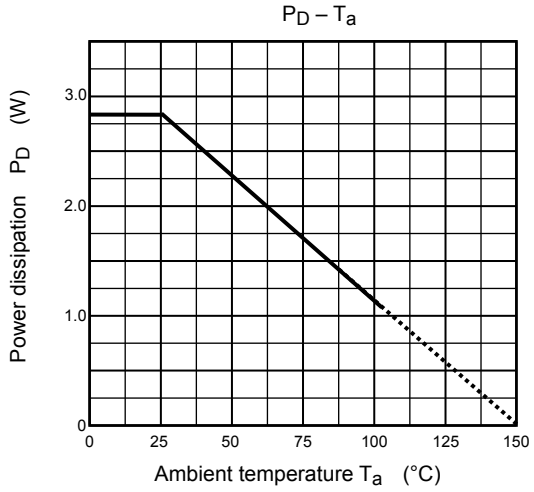
Operating Ranges

Characteristics	Symbol	Min	Typ.	Max	Unit
Power supply voltage 1	VM_{opr1}	5.5	12	22	V
Power supply voltage 2 (Note 9)	VM_{opr2}	4	5	5.5	V

Note 9: When voltage of VM is 5.5 V or less, pay attention to use the IC because the characteristics of the output ON resistance and VREG output voltage change.
High voltage that exceeds VM supply voltage should not be applied to the input signals of UH, UL, VH, VL, WH, and WL.

Package Power Dissipation (Reference data)

Mounted on the board (4-layer board: FR4:76.2mm × 114.3mm × 1.6mm)



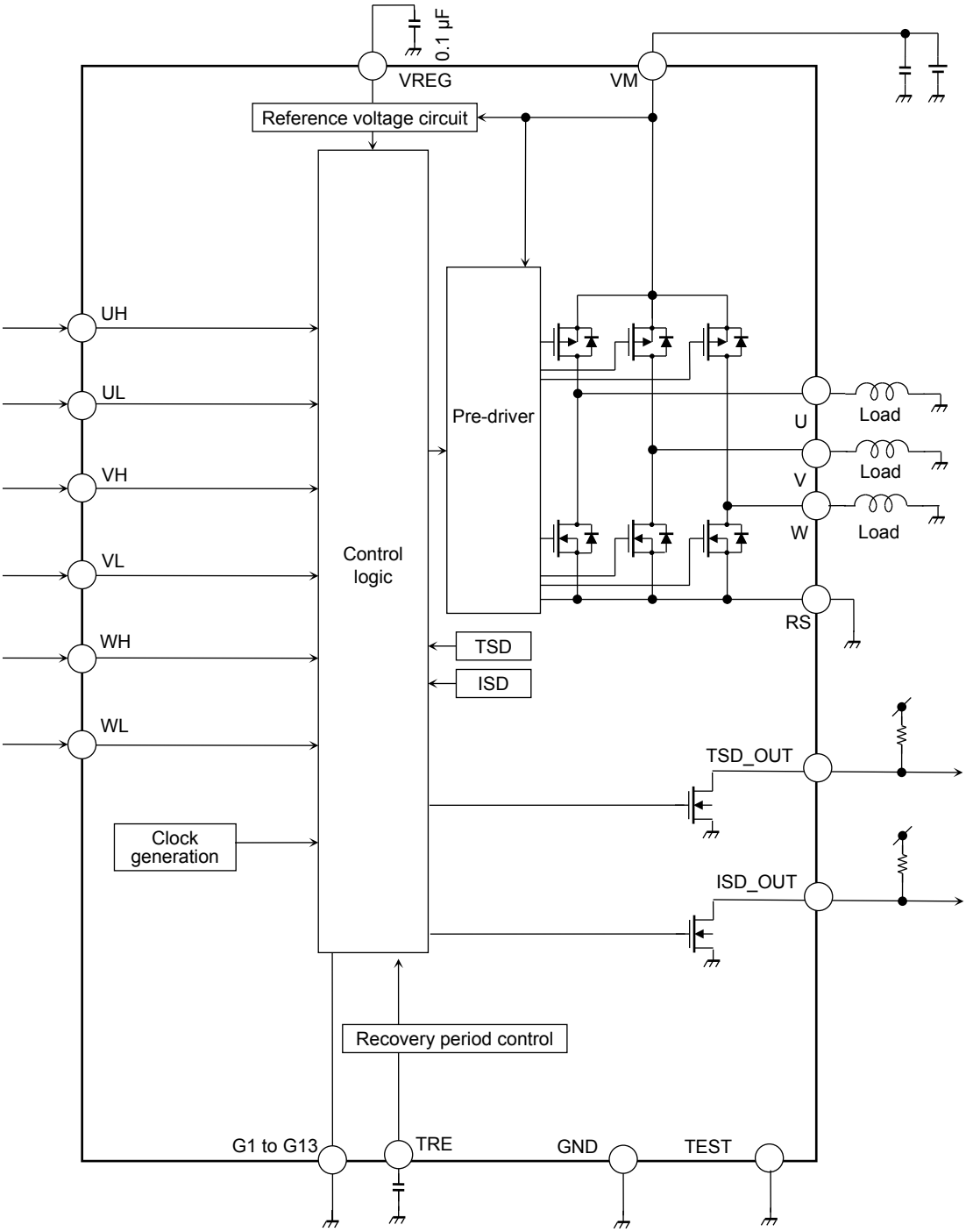
Electrical Characteristics (Ta = 25 °C, VM = 12 V, unless otherwise specified)

Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
Dynamic power supply current at VM	$I_{M\ (opr)}$	—	—	6.0	8.5	mA
Input current	IIN1(H)	V_{IN} = 5 V, UH,UL,VH,VL,WH,WL	—	100	150	μA
	IIN1 (L)	V_{IN} = 0 V, UH,UL,VH,VL,WH,WL	-1	—	1	
Input voltage	V_{IN1} (H)	UH,UL,VH,VL,WH,WL	2.0	—	—	V
	V_{IN1} (L)		GND	—	0.8	
Input voltage hysteresis	V1hys	UH,UL,VH,VL,WH,WL (Reference data)	—	0.12	—	V
TRE pin setting time	Tre	TRE = 1 μF(Reference data)	—	9.9	—	s
High-level TRE voltage	VH	—	2.25	2.5	2.75	V
Low-level TRE voltage	VL	—	0.45	0.5	0.55	V
Low-level TSD_OUT/ISD_OUT output voltage	V_{FG_OUT}	I_{OUT} = 5 mA	GND	—	0.5	V
TSD_OUT/ISD_OUT leakage current	I_{LFG_OUT}	V_{OUT} = 25 V	—	0	2	μA
Output ON-resistance at the U, V, and W pins	R_{ON1} (H)	I_{OUT} = 0.1A	—	0.3	0.6	Ω
	R_{ON1}(L)	I_{OUT} = -0.1A	—	0.3	0.6	
	R_{ON2} (H)	I_{OUT} = 0.1A, VM = 4.0 V	—	0.33	0.6	
	R_{ON2} (L)	I_{OUT} = -0.1A, VM = 4.0 V	—	0.33	0.6	
Output leakage current at the U, V, and W pins	I_L (H)	V_{OUT} = 0 V	-10	0	—	μA
	I_L (L)	V_{OUT} = 25 V	—	0	10	
Output diodes forward voltage at the U, V, and W pins	V_F (H)	I_{OUT} = 1.5 A (Reference data)	—	1.0	1.4	V
	V_F (L)	I_{OUT} = -1.5 A (Reference data)	—	1.0	1.4	
OSC frequency	OSC	(Reference data)	—	9	—	MHz
Masking time of over current detection	TISD	(Reference data)	—	4	—	μs
Current for over current detection	IISD	(Reference data)	—	4.5	—	A
Thermal shutdown	TSD	(Reference data)	—	165	—	°C
	TSDhys	Hysteresis from thermal shutdown to normal operation. (Reference data)	—	15	—	
UVLO trip threshold voltage at the VM pin	VMUVLO	—	—	3.4	—	V
UVLO recovery voltage at the VM pin	VMUVLOR	—	—	3.7	—	V
UVLO trip threshold voltage at the VREG pin	VREGUVLO	—	—	3.0	—	V
UVLO recovery voltage at the VREG pin	VREGUVLOR	—	—	3.2	—	V
Recovery time of UVLO detection	TUVLO	(Reference data)	—	29	—	ms
VREG output voltage	VREG1	IVREG = -5 mA	4.5	5	5.5	V
	VREG2	IVREG = -5 mA, VM = 4.0 V	3.6	3.9	4.0	V

*Reference data: No shipping inspection.

Application Circuit Example

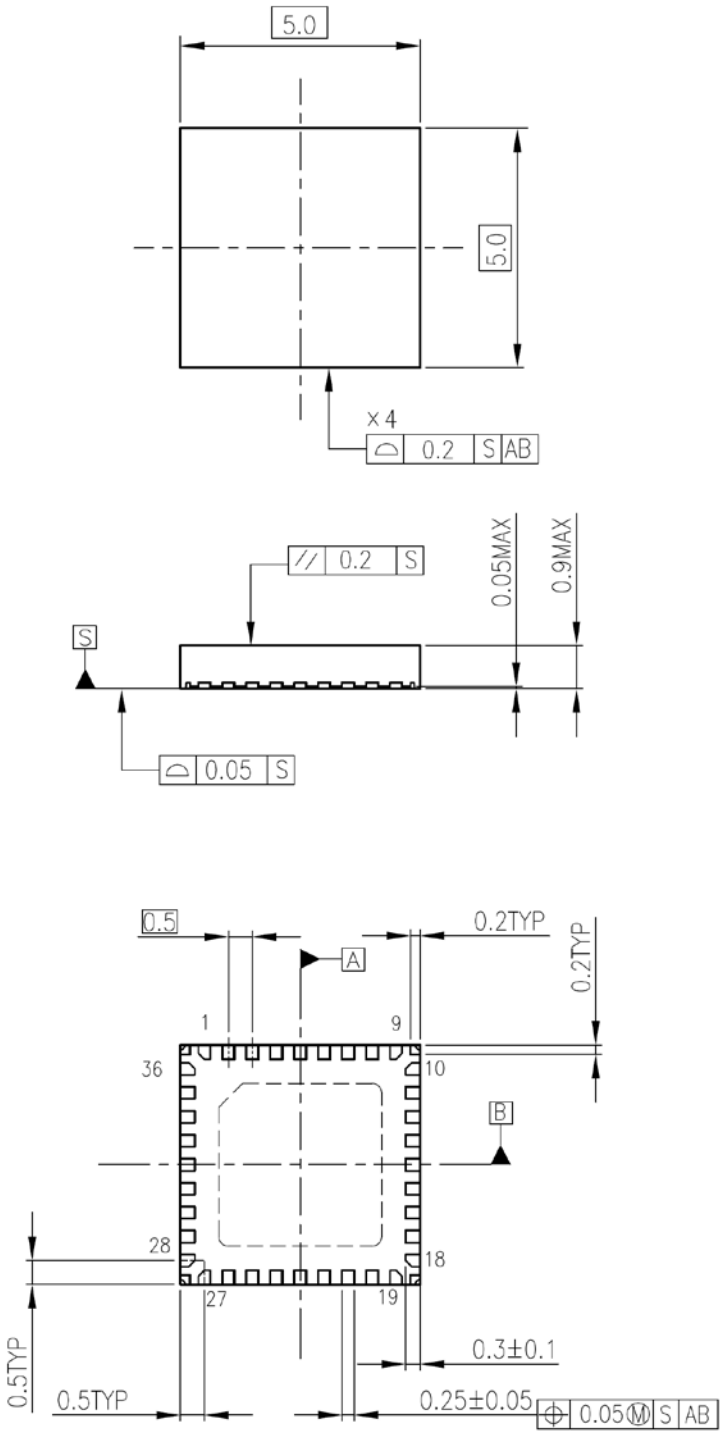
Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.
The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
Providing these application circuit examples does not grant a license for industrial property rights.



Package Dimensions

P-VQFN36-0505-0.50-001

Unit: mm



Weight: 0.05g (typ.)

Notes on Contents

1. Block Diagrams

Some of the functional blocks, circuits, or constants in the block diagram may be omitted or simplified for explanatory purposes.

2. Equivalent Circuits

The equivalent circuit diagrams may be simplified or some parts of them may be omitted for explanatory purposes.

3. Timing Charts

Timing charts may be simplified for explanatory purposes.

4. Application Circuits

The application circuits shown in this document are provided for reference purposes only. Thorough evaluation is required, especially at the mass production design stage.
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5. Test Circuits

Components in the test circuits are used only to obtain and confirm the device characteristics. These components and circuits are not guaranteed to prevent malfunction or failure from occurring in the application equipment.

IC Usage Considerations

Notes on handling of ICs

(1) The absolute maximum ratings of a semiconductor device are a set of ratings that must not be exceeded, even for a moment. Do not exceed any of these ratings.
Exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.

(2) Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

(3) If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. IC breakdown may cause injury, smoke or ignition.
Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

(4) Do not insert devices in the wrong orientation or incorrectly.
Make sure that the positive and negative terminals of power supplies are connected properly. Otherwise, the current or power consumption may exceed the absolute maximum rating, and exceeding the rating(s) may cause the device breakdown, damage or deterioration, and may result injury by explosion or combustion.
In addition, do not use any device that is applied the current with inserting in the wrong orientation or incorrectly even just one time.

Points to remember on handling of ICs

(1) Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

(2) Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately. Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

(3) Heat Radiation Design

In using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_j) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into considerate the effect of IC heat radiation with peripheral components.

(4) Back-EMF

When a motor rotates in the reverse direction, stops or slows down abruptly, a current flow back to the motor's power supply due to the effect of back-EMF. If the current sink capability of the power supply is small, the device's motor power supply and output pins might be exposed to conditions beyond absolute maximum ratings. To avoid this problem, take the effect of back-EMF into consideration in system design.

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