CY7C09349AV
CY7C09359AV

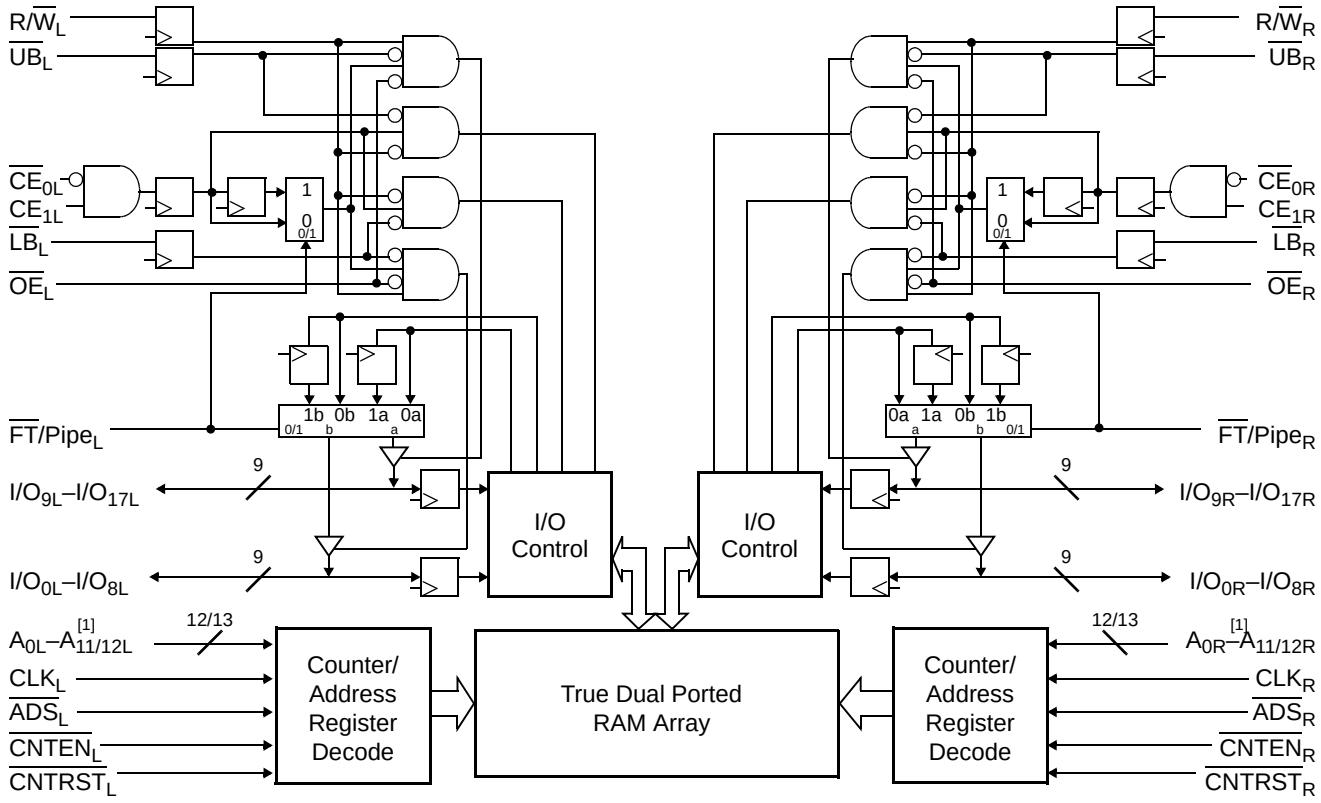
3.3 V 4 K/8 K × 18 Synchronous Dual Port Static RAM

Features

- True dual ported memory cells which allow simultaneous access of the same memory location
- Two flow-through/pipelined devices
  - 4 K × 18 organization (CY7C09349AV)
  - 8 K × 18 organization (CY7C09359AV)
- Three modes
  - Flow-through
  - Pipelined
  - Burst
- Pipelined output mode on both ports allows fast 67-MHz operation
- 0.35-micron complementary metal oxide semiconductor (CMOS) for optimum speed/power
- High-speed clock to data access 9 and 12 ns (max)
- 3.3 V low operating power
  - Active = 135 mA (typical)
  - Standby = 10 µA (typical)
- Fully synchronous interface for easier operation
- Burst counters increment addresses internally
  - Shorten cycle times
  - Minimize bus noise
  - Supported in flow-through and pipelined modes
- Dual chip enables for easy depth expansion
- Upper and lower byte controls for bus matching
- Automatic power-down
- Available in 100-pin thin quad flat pack (TQFP)

For a complete list of related documentation, click here.

Logic Block Diagram



Note
1. A_0–A_{11} for 4 K; A_0–A_{12} for 8 K devices.

Functional Description

The CY7C09349AV and CY7C09359AV are high-speed 3.3 V synchronous CMOS 4 K and 8 K × 18 dual-port static RAMs. Two ports are provided, permitting independent, simultaneous access for reads and writes to any location in memory.[2] Registers on control, address, and data lines allow for minimal set-up and hold times. In pipelined output mode, data is registered for decreased cycle time. Clock to data valid t_{CD2} = 9 ns (pipelined). Flow-through mode can also be used to bypass the pipelined output register to eliminate access latency. In flow-through mode data will be available t_{CD1} = 20 ns after the address is clocked into the device. Pipelined output or flow-through mode is selected via the FT/Pipe pin.

Each port contains a burst counter on the input address register. The internal write pulse width is independent of the LOW-to-HIGH transition of the clock signal. The internal write pulse is self-timed to allow the shortest possible cycle times.

A HIGH on $\overline{CE}_0$ or LOW on CE_1 for one clock cycle will power down the internal circuitry to reduce the static power consumption. The use of multiple chip enables allows easier banking of multiple chips for depth expansion configurations. In the pipelined mode, one cycle is required with $\overline{CE}_0$ LOW and CE_1 HIGH to reactivate the outputs.

Counter enable inputs are provided to stall the operation of the address input and utilize the internal address generated by the internal counter for fast interleaved memory applications. A port's burst counter is loaded with the port's address strobe (ADS). When the port's count enable (CNTEN) is asserted, the address counter will increment on each LOW-to-HIGH transition of that port's clock signal. This will read/write one word from/into each successive address location until CNTEN is deasserted. The counter can address the entire memory array and will loop back to the start. Counter reset (CNTRST) is used to reset the burst counter.

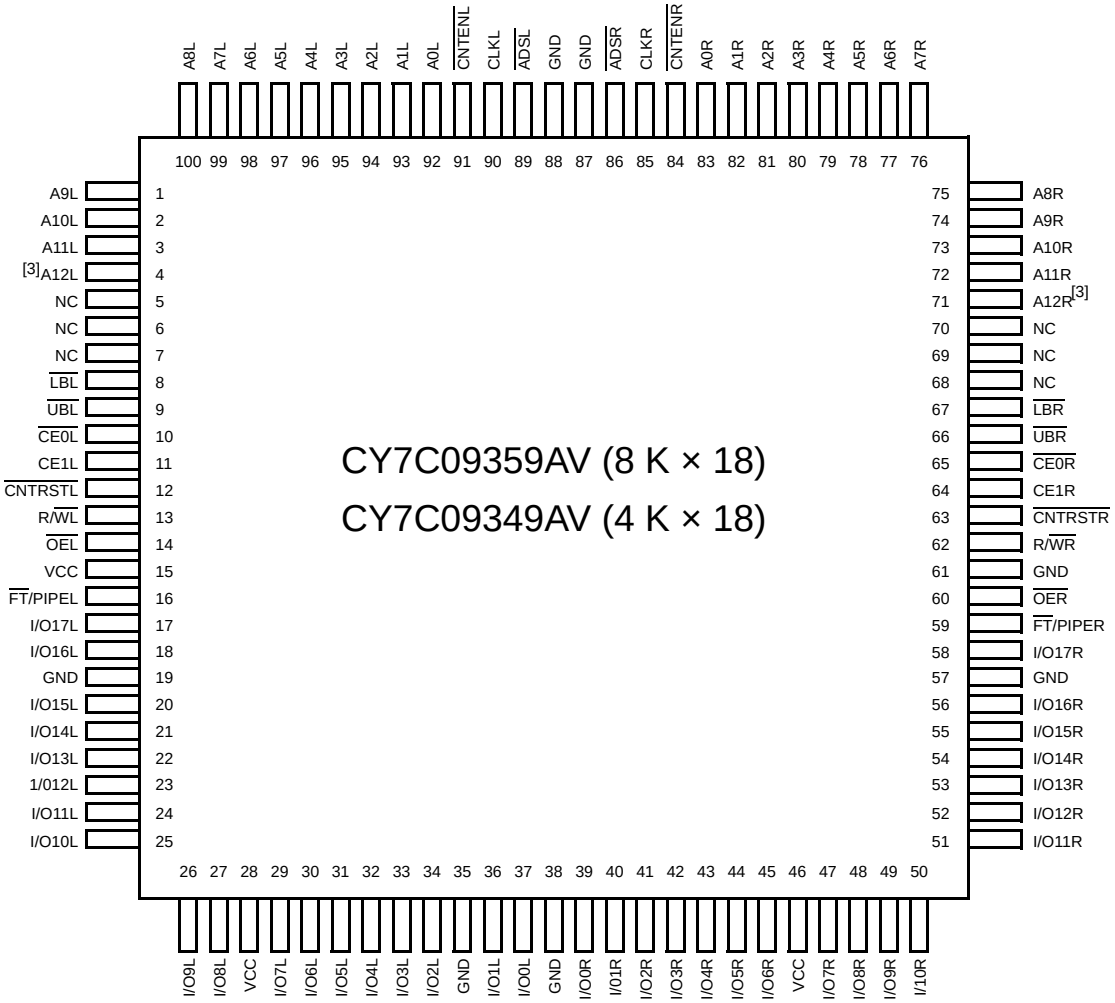
All parts are available in 100-pin thin quad plastic flatpack (TQFP) packages.

Note
2. When simultaneously writing to the same location, final value cannot be guaranteed.

Contents

Pin Configuration

Figure 1. 100-pin TQFP (Top View)



Selection Guide

	CY7C09349AV CY7C09359AV –9	CY7C09349AV –12
f_{MAX2} (MHz) (pipelined)	67	50
Max access time (ns) (clock to data, pipelined)	9	12
Typical operating current I_{CC} (mA)	135	115
Typical standby current for I_{SB1} (mA) (both ports TTL level)	20	20
Typical standby current for I_{SB3} (µA) (both ports CMOS level)	10	10

Note
3. This pin is NC for CY7C09349AV.

Pin Definitions

Left Port	Right Port	Description
A_{0L}–A_{12L}	A_{0R}–A_{12R}	Address inputs (A_0–A_{11} for 4 K, A_0–A_{12} for 8 K devices).
$\overline{ADS}_L$	$\overline{ADS}_R$	Address strobe input. Used as an address qualifier. This signal should be asserted LOW during normal read or write transactions. Asserting this signal LOW also loads the burst address counter with data present on the I/O pins.
$\overline{CE}_{0L}$, CE_{1L}	$\overline{CE}_{0R}$, CE_{1R}	Chip enable input. To select either the left or right port, both $\overline{CE}_0$ and CE_1 must be asserted to their active states ($\overline{CE}_0 \le V_{IL}$ and $CE_1 \ge V_{IH}$).
CLK_L	CLK_R	Clock signal. This input can be free running or strobed. Maximum clock input rate is f_{MAX}.
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter enable input. Asserting this signal LOW increments the burst address counter of its respective port on each rising edge of CLK. $\overline{CNTEN}$ is disabled if $\overline{ADS}$ or $\overline{CNTRST}$ are asserted LOW.
$\overline{CNTRST}_L$	$\overline{CNTRST}_R$	Counter reset input. Asserting this signal LOW resets the burst address counter of its respective port to zero. $\overline{CNTRST}$ is not disabled by asserting $\overline{ADS}$ or $\overline{CNTEN}$.
I/O_{0L}–I/O_{17L}	I/O_{0R}–I/O_{17R}	Data bus input/output (I/O_0–I/O_{15} for ×16 devices).
$\overline{LB}_L$	$\overline{LB}_R$	Lower byte select input. Asserting this signal LOW enables read and write operations to the lower byte (I/O_0–I/O_8 for ×18, I/O_0–I/O_7 for ×16) of the memory array. For read operations both the $\overline{LB}$ and $\overline{OE}$ signals must be asserted to drive output data on the lower byte of the data pins.
$\overline{UB}_L$	$\overline{UB}_R$	Upper byte select input. Same function as $\overline{LB}$, but to the upper byte ($I/O_{8/9L}$–$I/O_{15/17L}$).
$\overline{OE}_L$	$\overline{OE}_R$	Output enable input. This signal must be asserted LOW to enable the I/O data pins during read operations.
$R/\overline{W}_L$	$R/\overline{W}_R$	Read/write enable input. This signal is asserted LOW to write to the dual port memory array. For read operations, assert this pin HIGH.
$\overline{FT}/PIPE_L$	$\overline{FT}/PIPE_R$	Flow-through/pipelined select input. For flow-through mode operation, assert this pin LOW. For pipelined mode operation, assert this pin HIGH.
GND		Ground input.
NC		No connect.
V_{CC}		Power input.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied . –55 °C to +125 °C

Supply voltage to ground potential .....–0.5 V to +4.6 V

DC voltage applied to outputs in high Z state .....–0.5 V to V_{CC} + 0.5 V

DC input voltage .....–0.5 V to V_{CC} + 0.5 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	3.3 V ± 300 mV
Industrial	–40 °C to +85 °C	3.3 V ± 300 mV

Electrical Characteristics

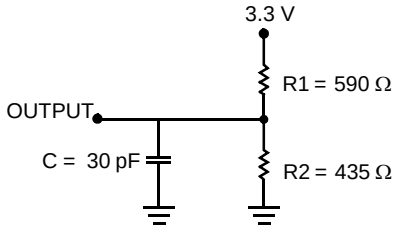
Over the Operating Range

Parameter	Description		CY7C09349AV CY7C09359AV						Unit
			–9			–12			
			Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH voltage (V_{CC} = Min, I_{OH} = –4.0 mA)		2.4	–	–	2.4	–	–	V
V_{OL}	Output LOW voltage (V_{CC} = Min, I_{OH} = +4.0 mA)		–		0.4	–		0.4	V
V_{IH}	Input HIGH voltage		2.0		–	2.0		–	V
V_{IL}	Input LOW voltage		–		0.8	–		0.8	V
I_{OZ}	Output leakage current		–10		10	–10		10	µA
I_{CC}	Operating current (V_{CC} = Max, I_{OUT} = 0 mA) outputs disabled	Commercial	–	135	230	–	115	180	mA
		Industrial		–			155	250	mA
I_{SB1}	Standby current (both ports TTL level)[4] $\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Commercial		20	75		20	70	mA
		Industrial		–			30	80	mA
I_{SB2}	Standby current (one port TTL level)[4] $\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Commercial		95	155		85	140	mA
		Industrial		–			95	150	mA
I_{SB3}	Standby current (both ports CMOS level)[4] $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ – 0.2 V, f = 0	Commercial		10	500		10	500	µA
		Industrial		–			10	500	µA
I_{SB4}	Standby current (one port CMOS level)[4] $\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$, f = f_{MAX}	Commercial		85	115		75	100	mA
		Industrial		–			85	110	mA

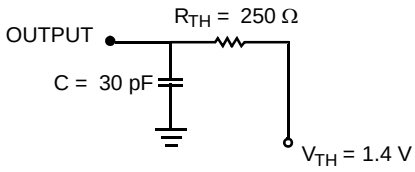
Capacitance

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 3.3 V	10	pF
C_{OUT}	Output capacitance		10	pF

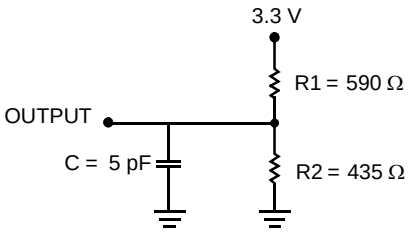
AC Test Loads



(a) Normal Load (Load 1)



(b) Thévenin Equivalent (Load 1)



(c) Three-State Delay (Load 2)
(Used for t_{CKLZ}, t_{OLZ}, & t_{OHZ} including scope and jig)

Note
4. $\overline{CE}_L$ and $\overline{CE}_R$ are internal signals. To select either the left or right port, both $\overline{CE}_0$ AND CE_1 must be asserted to their active states ($\overline{CE}_0 \leq V_{IL}$ and $CE_1 \geq V_{IH}$).

Switching Characteristics

Over the Operating Range

Parameter	Description	CY7C09349AV CY7C09359AV				Unit
		–9		–12		
		Min	Max	Min	Max	
f_{MAX1}	f_{Max} flow-through	–	40	–	33	MHz
f_{MAX2}	f_{Max} pipelined	–	67	–	50	MHz
t_{CYC1}	Clock cycle time – flow-through	25	–	30	–	ns
t_{CYC2}	Clock cycle time – pipelined	15	–	20	–	ns
t_{CH1}	Clock HIGH time – flow-through	12	–	12	–	ns
t_{CL1}	Clock LOW time – flow-through	12	–	12	–	ns
t_{CH2}	Clock HIGH time – pipelined	6	–	8	–	ns
t_{CL2}	Clock LOW time – pipelined	6	–	8	–	ns
t_R	Clock rise time	–	3	–	3	ns
t_F	Clock fall time	–	3	–	3	ns
t_{SA}	Address set-up time	4	–	4	–	ns
t_{HA}	Address hold time	1	–	1	–	ns
t_{SC}	Chip enable set-up time	4	–	4	–	ns
t_{HC}	Chip enable hold time	1	–	1	–	ns
t_{SW}	R/$\overline{W}$ set-up time	4	–	4	–	ns
t_{HW}	R/$\overline{W}$ hold time	1	–	1	–	ns
t_{SD}	Input data set-up time	4	–	4	–	ns
t_{HD}	Input data hold time	1	–	1	–	ns
t_{SAD}	$\overline{ADS}$ set-up time	4	–	4	–	ns
t_{HAD}	$\overline{ADS}$ hold time	1	–	1	–	ns
t_{SCN}	$\overline{CNTEN}$ set-up time	4	–	4	–	ns
t_{HCN}	$\overline{CNTEN}$ hold time	1	–	1	–	ns
t_{SRST}	$\overline{CNTRST}$ set-up time	4	–	4	–	ns
t_{HRST}	$\overline{CNTRST}$ hold time	1	–	1	–	ns
t_{OE}	Output enable to data valid	–	10	–	12	ns
t_{OLZ}	$\overline{OE}$ to low Z	2	–	2	–	ns
t_{OHZ}	$\overline{OE}$ to high Z	1	7	1	7	ns
t_{CD1}	Clock to data valid – flow-through	–	20	–	25	ns
t_{CD2}	Clock to data valid – pipelined	–	9	–	12	ns
t_{DC}	Data output hold after clock HIGH	2	–	2	–	ns
t_{CKHZ}	Clock HIGH to output high Z	2	9	2	9	ns
t_{CKLZ}	Clock HIGH to output low Z	2	–	2	–	ns
Port to port delays						
t_{CWDD}	Write port clock HIGH to read data delay	–	40	–	40	ns
t_{CCS}	Clock to clock set-up time	–	15	–	15	ns

Switching Waveforms

Figure 2. Read Cycle for Flow-through Output ($\overline{FT}$/PIPE = V_{IL})[5, 6, 7, 8]

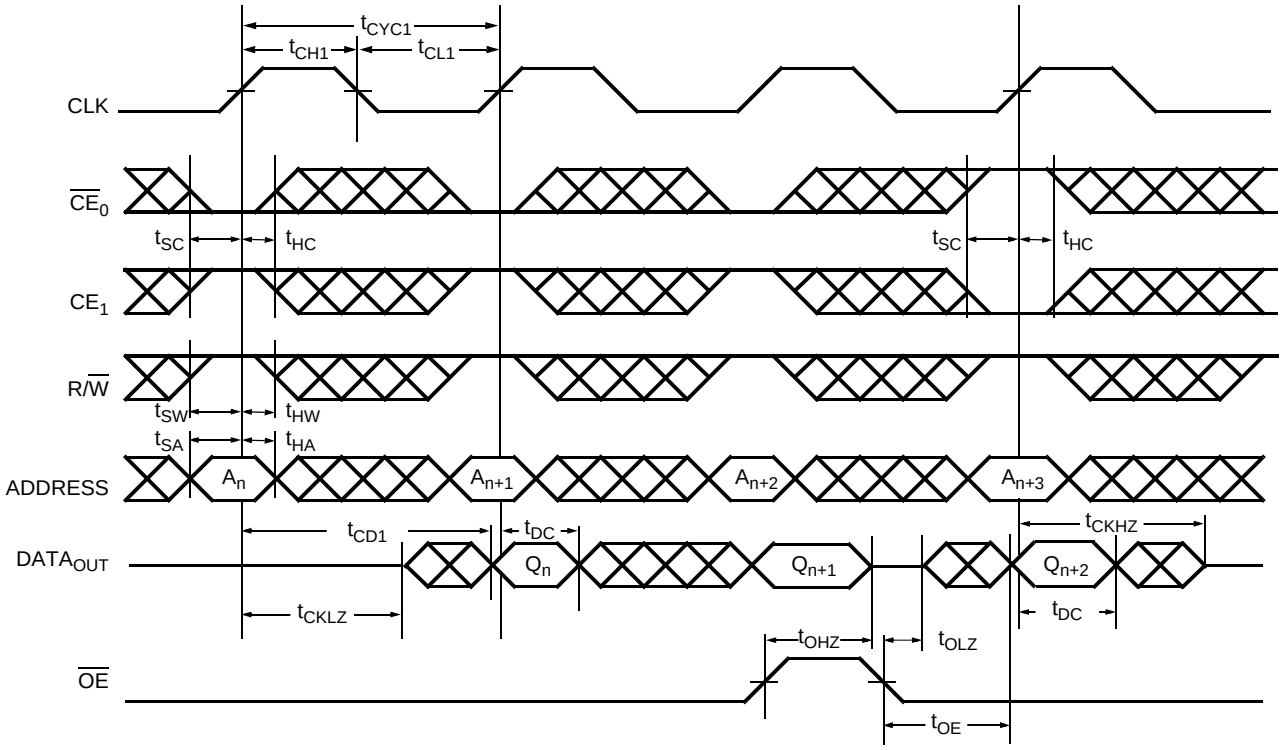
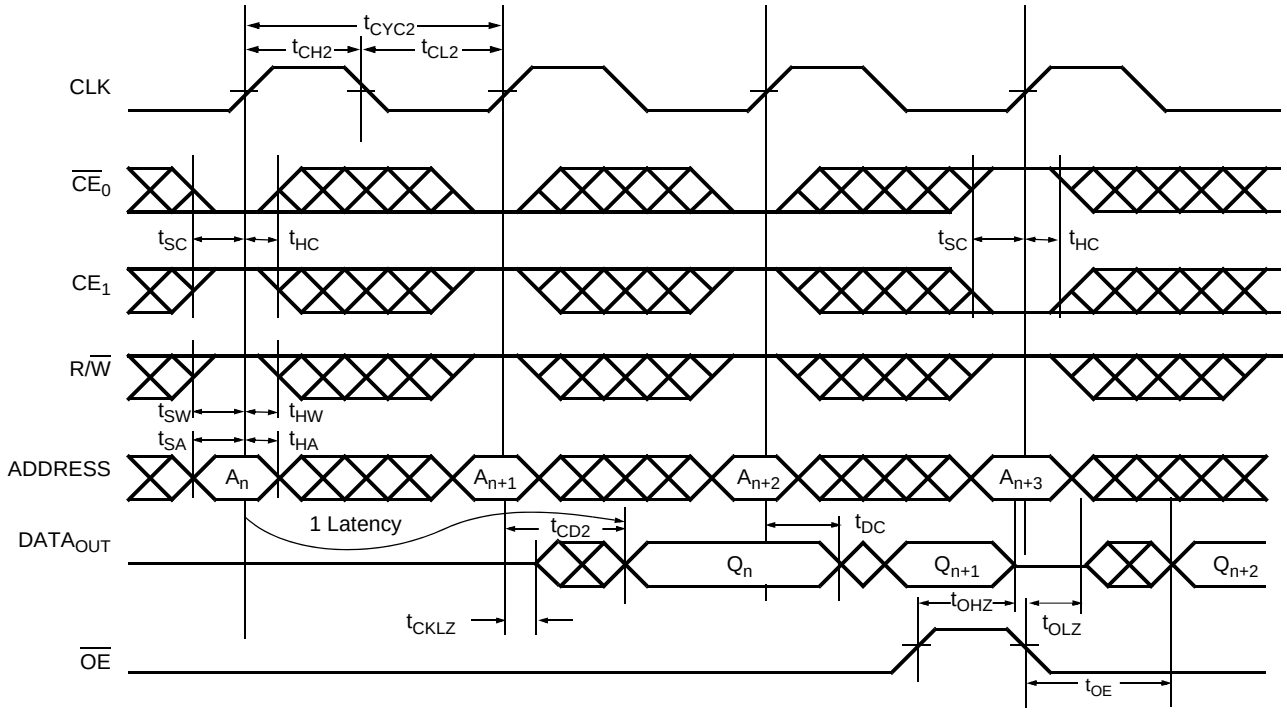


Figure 3. Read Cycle for Pipelined Operation ($\overline{FT}$/PIPE = V_{IH})[5, 6, 7, 8]



Notes

5. $\overline{OE}$ is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
6. $\overline{ADS}$ = V_{IL}, CNTEN and $\overline{CNTRST}$ = V_{IH}.
7. The output is disabled (high-impedance state) by $\overline{CE}_0$ = V_{IH} or CE_1 = V_{IL} following the next rising edge of the clock.
8. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK. Numbers are for reference only.

Switching Waveforms *(continued)*

Figure 4. Bank Select Pipelined Read[9, 10]

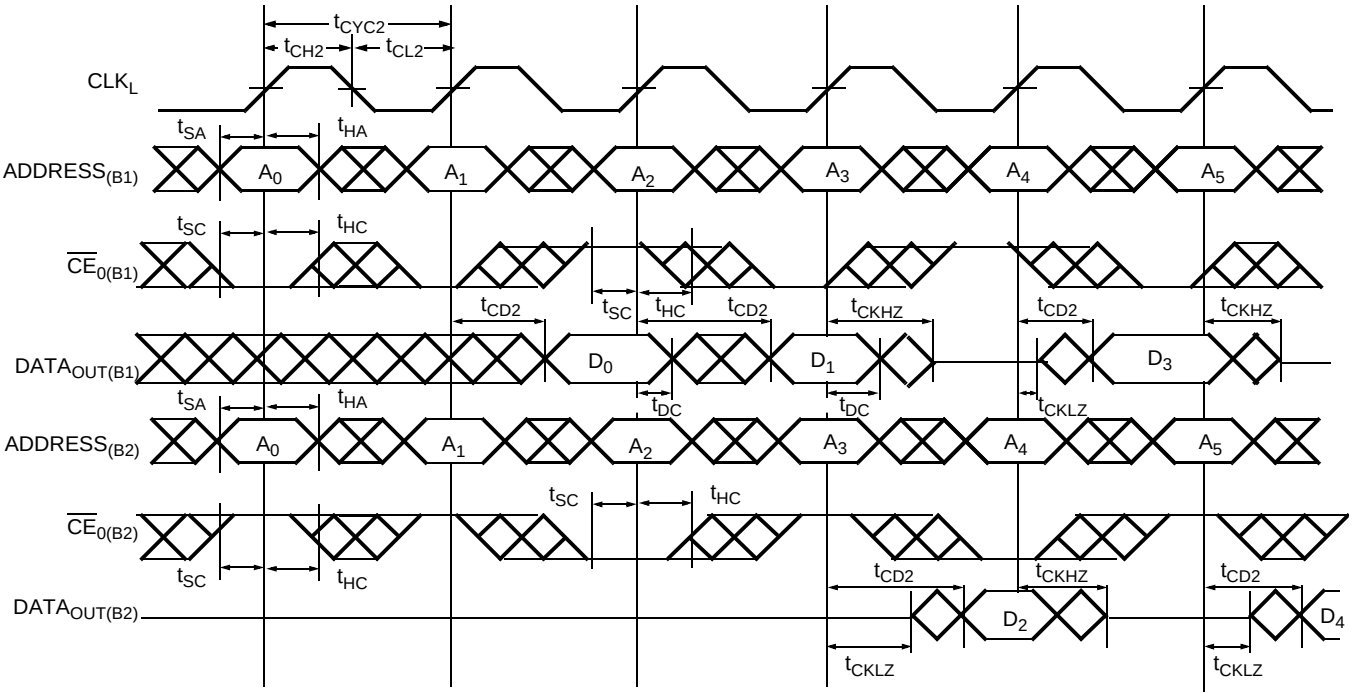
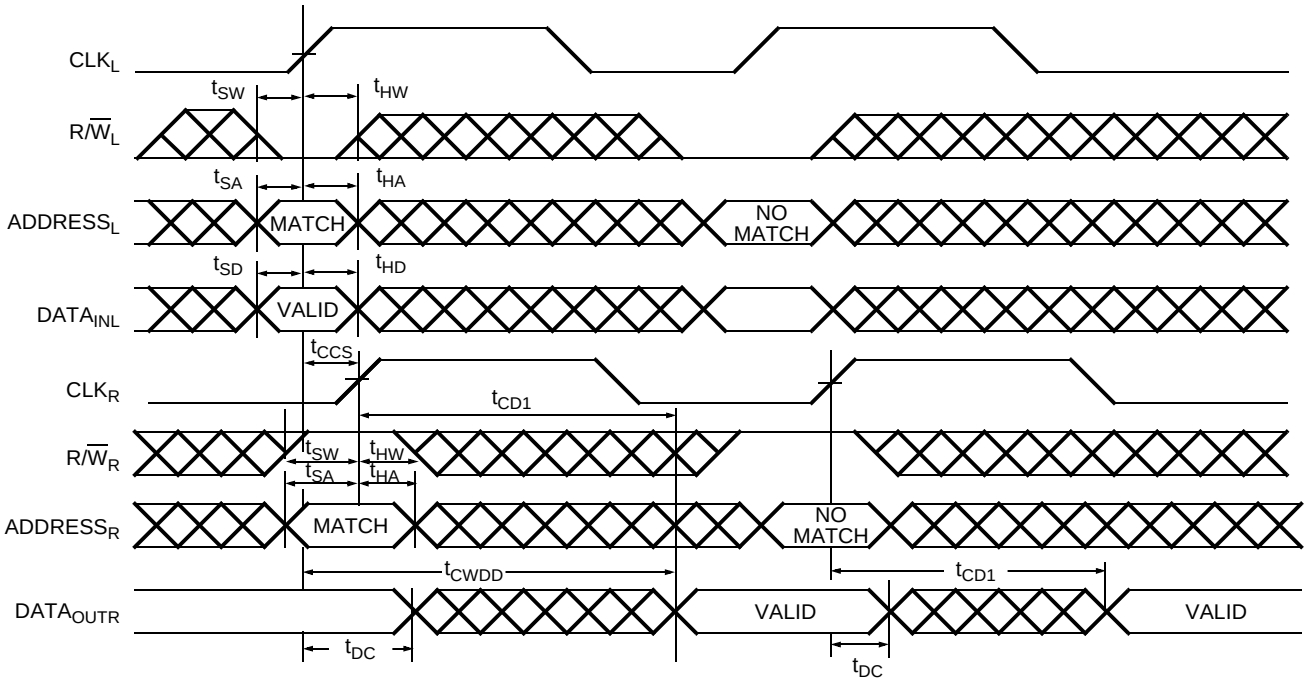


Figure 5. Left Port Write to Flow-through Right Port Read[11, 12, 13, 14]



Notes

9. In this depth expansion example, B1 represents Bank #1 and B2 is Bank #2; Each bank consists of one Cypress dual-port device from this data sheet. $ADDRESS_{(B1)} = ADDRESS_{(B2)}$.
10. $\overline{UB}$, $\overline{LB}$, $\overline{OE}$ and $\overline{ADS} = V_{IL}$; $\overline{CE}_{1(B1)}$, $CE_{1(B2)}$, R/$\overline{W}$, $\overline{CNTEN}$, and $\overline{CNTRST} = V_{IH}$.
11. The same waveforms apply for a right port write to flow-through left port read.
12. $\overline{CE}_0$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADS} = V_{IL}$; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST} = V_{IH}$.
13. $\overline{OE} = V_{IL}$ for the right port, which is being read from. $\overline{OE} = V_{IH}$ for the left port, which is being written to.
14. If $t_{CCS} \le$ maximum specified, then data from right port READ is not valid until the maximum specified for t_{CWDD}. If t_{CCS} > maximum specified, then data is not valid until $t_{CCS} + t_{CD1}$. t_{CWDD} does not apply in this case.

Switching Waveforms *(continued)*

Figure 6. Pipelined Read-to-Write-to-Read ($\overline{OE}$ = V_{IL})[15, 16, 17, 18]

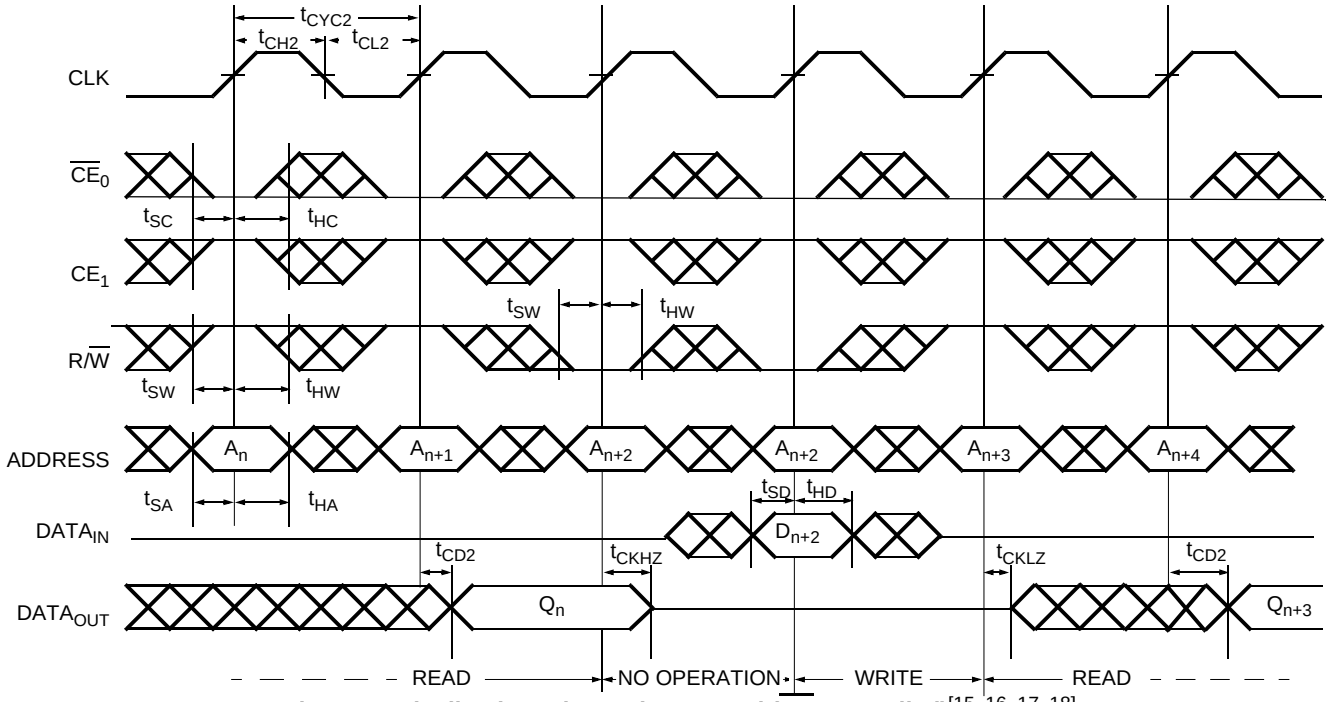
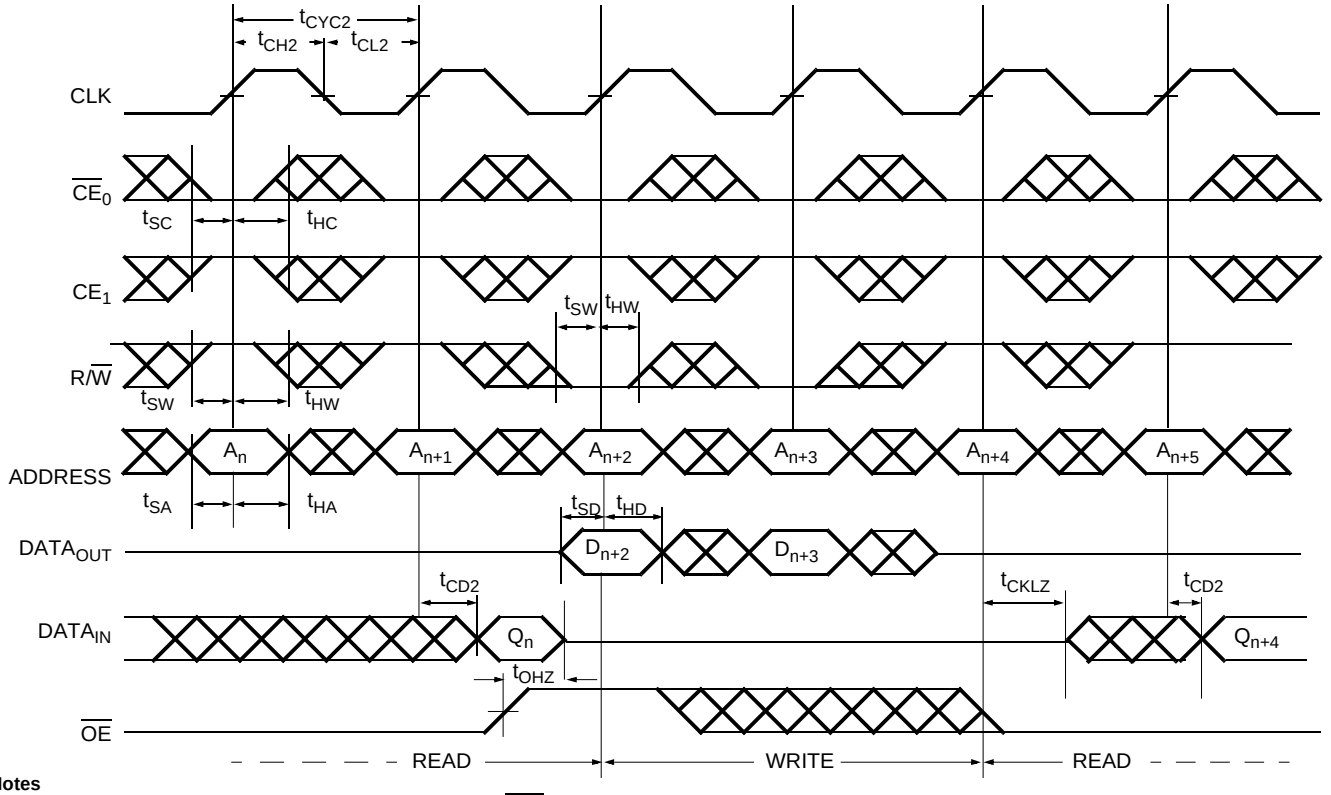


Figure 7. Pipelined Read-to-Write-to-Read ($\overline{OE}$ Controlled)[15, 16, 17, 18]



Notes

15. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK. Numbers are for reference only.
16. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
17. $\overline{CE_0}$ and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
18. During “No operation”, data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.

Switching Waveforms *(continued)*

Figure 8. Flow-through Read-to-Write-to-Read ($\overline{OE}$ = V_{IL})[19, 20, 22, 23]

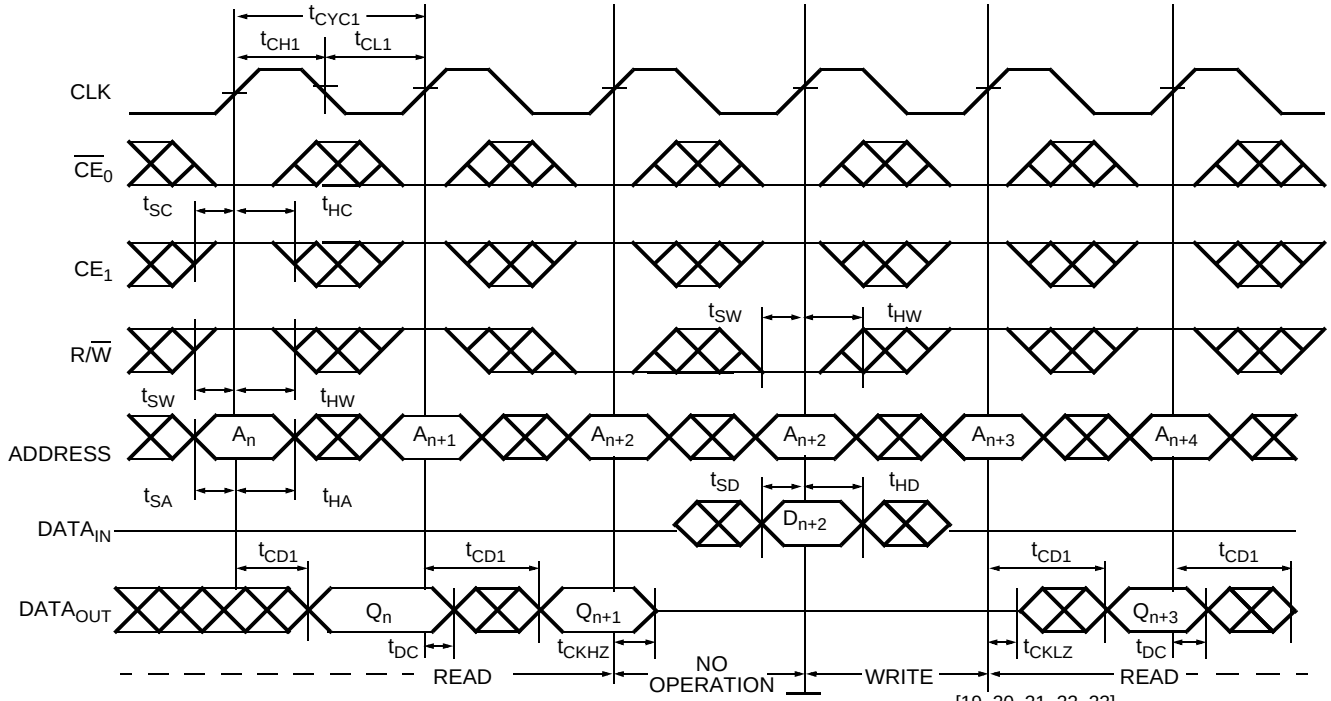
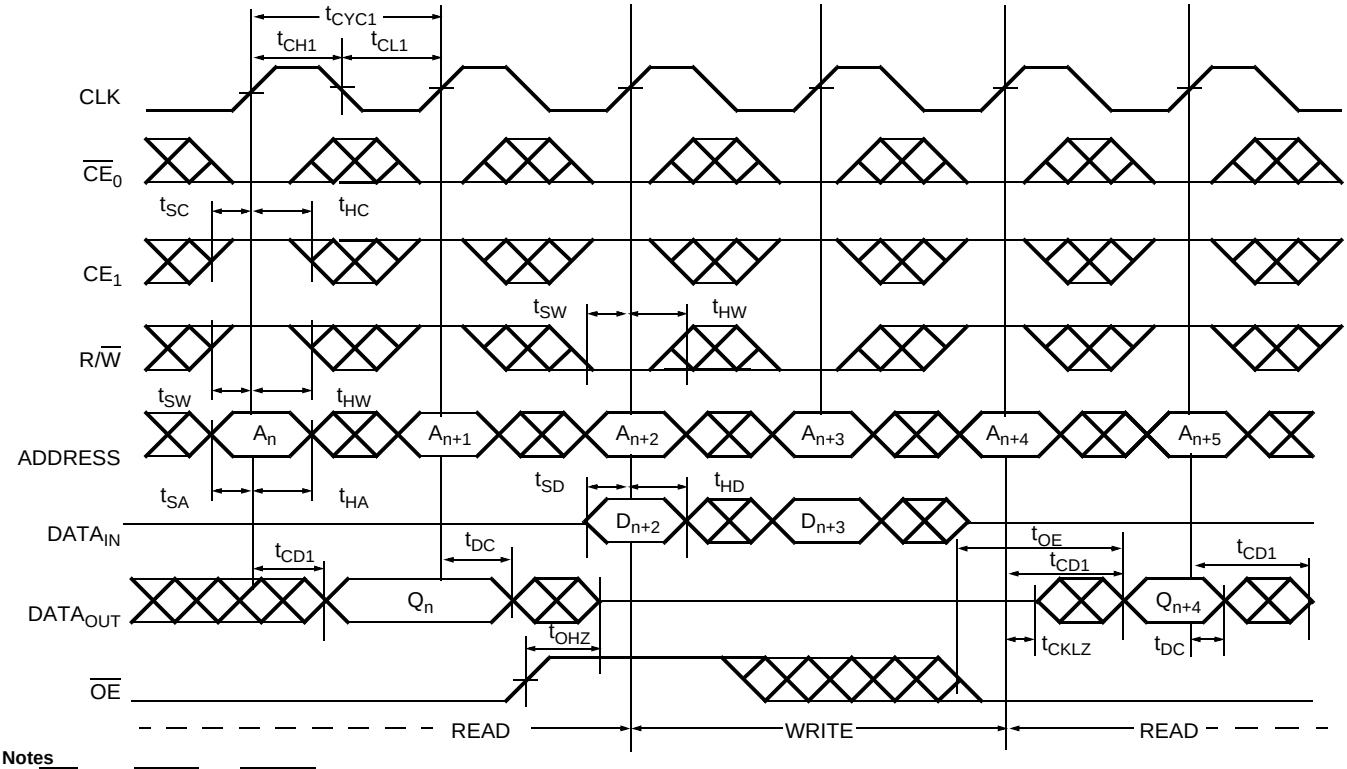


Figure 9. Flow-through Read-to-Write-to-Read ($\overline{OE}$ Controlled)[19, 20, 21, 22, 23]



Notes

19. $\overline{ADS}$ = V_{IL}, $\overline{CNTEN}$ and $\overline{CNTRST}$ = V_{IH}.
20. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK. Numbers are for reference only.
21. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
22. $\overline{CE_0}$ and $\overline{ADS}$ = V_{IL}; CE_1, $\overline{CNTEN}$, and $\overline{CNTRST}$ = V_{IH}.
23. During "No operation," data in memory at the selected address may be corrupted and should be rewritten to ensure data integrity.

Switching Waveforms *(continued)*

Figure 10. Pipelined Read with Address Counter Advance[24]

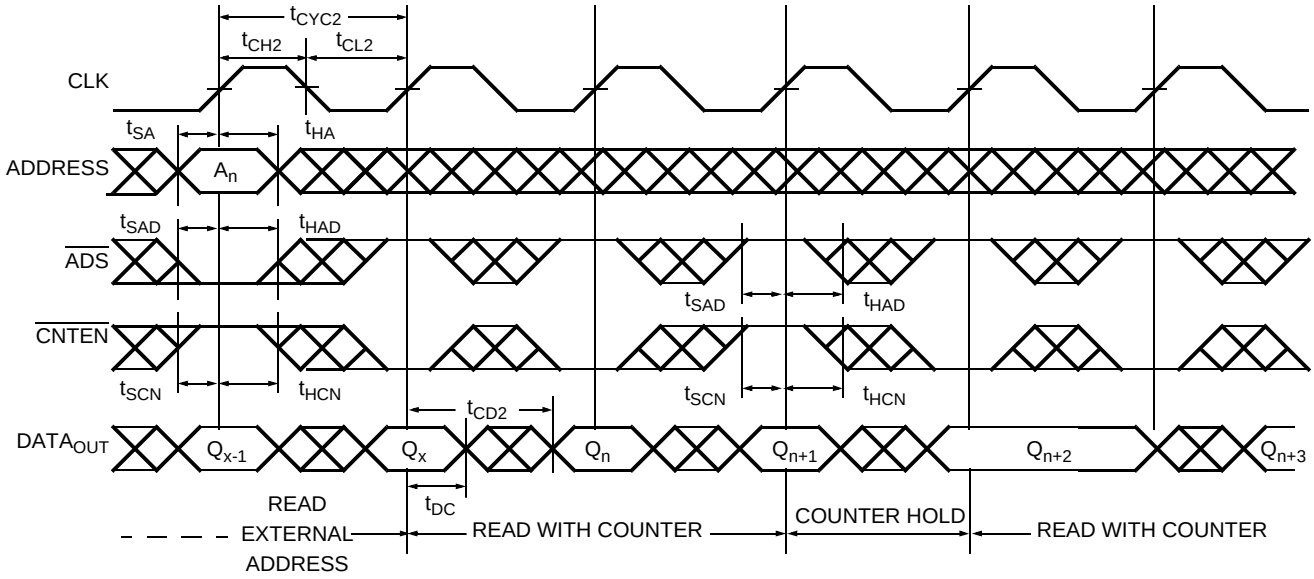
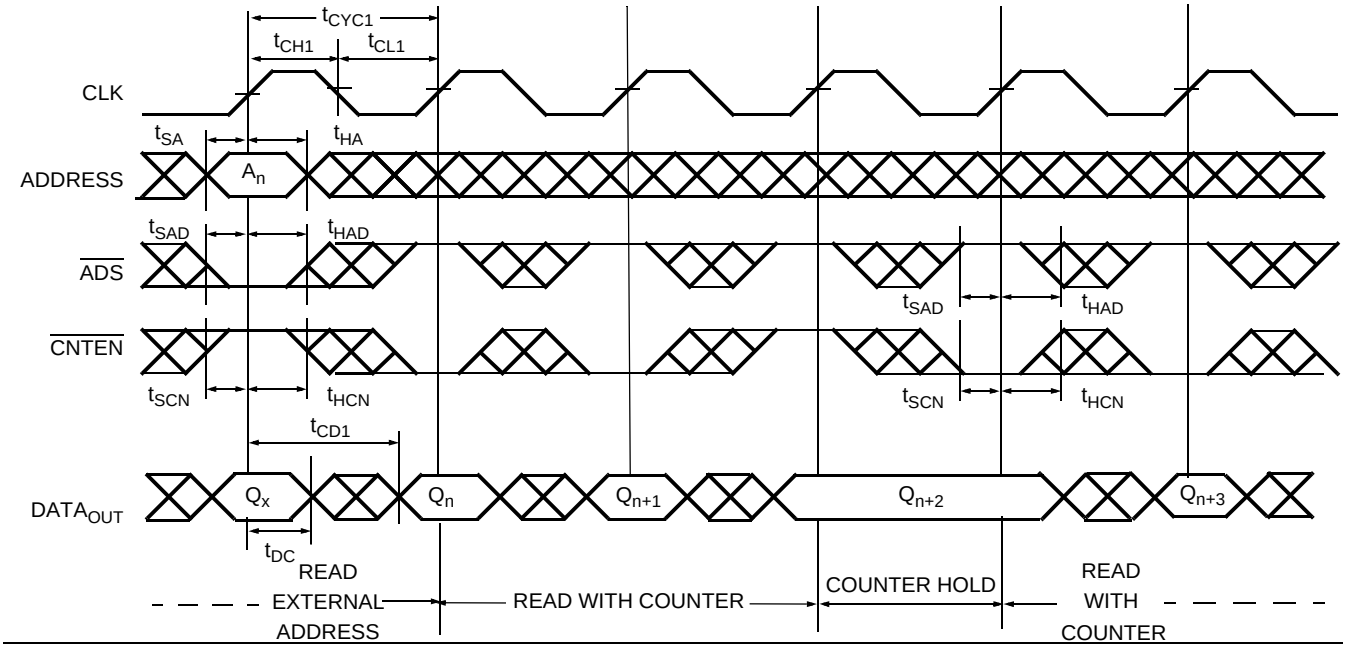


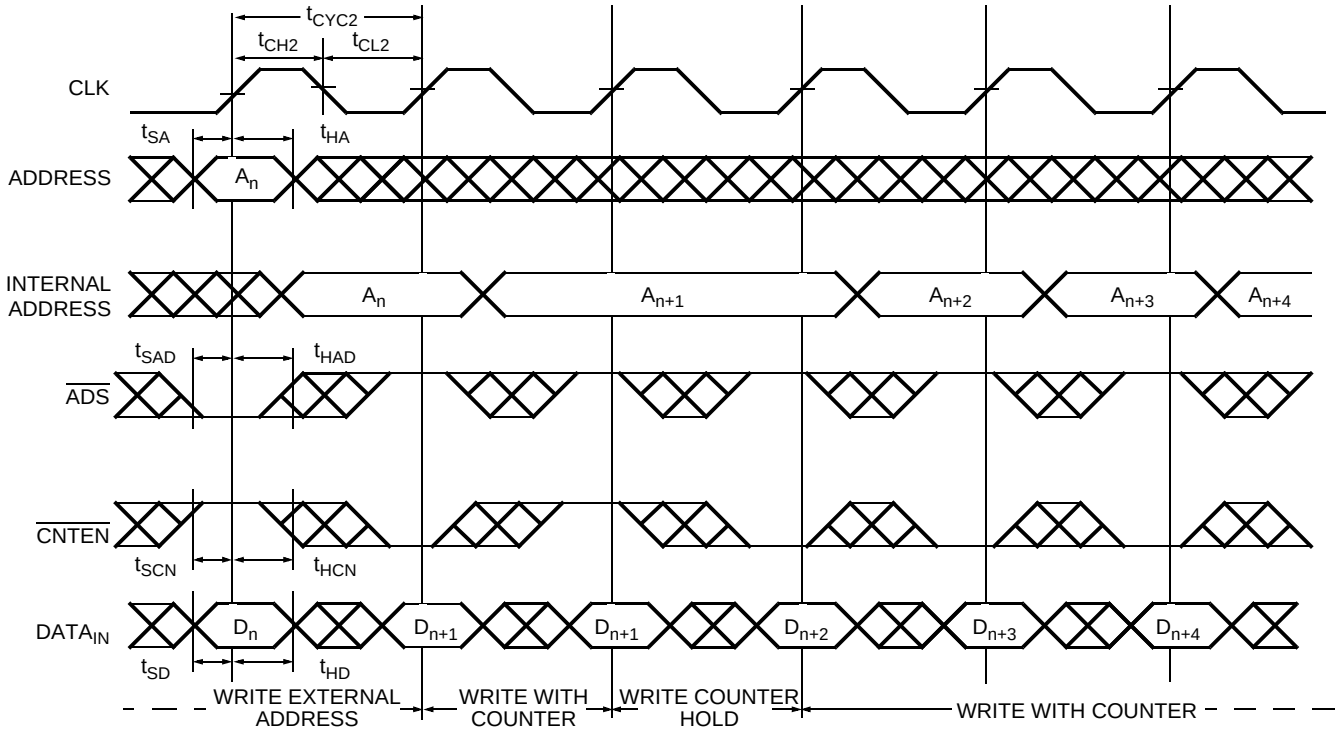
Figure 11. Flow-through Read with Address Counter Advance[24]



Note
24. $\overline{CE_0}$ and $\overline{OE}$ = V_{IL}; CE_1, R/$\overline{W}$ and $\overline{CNTRST}$ = V_{IH}.

Switching Waveforms *(continued)*

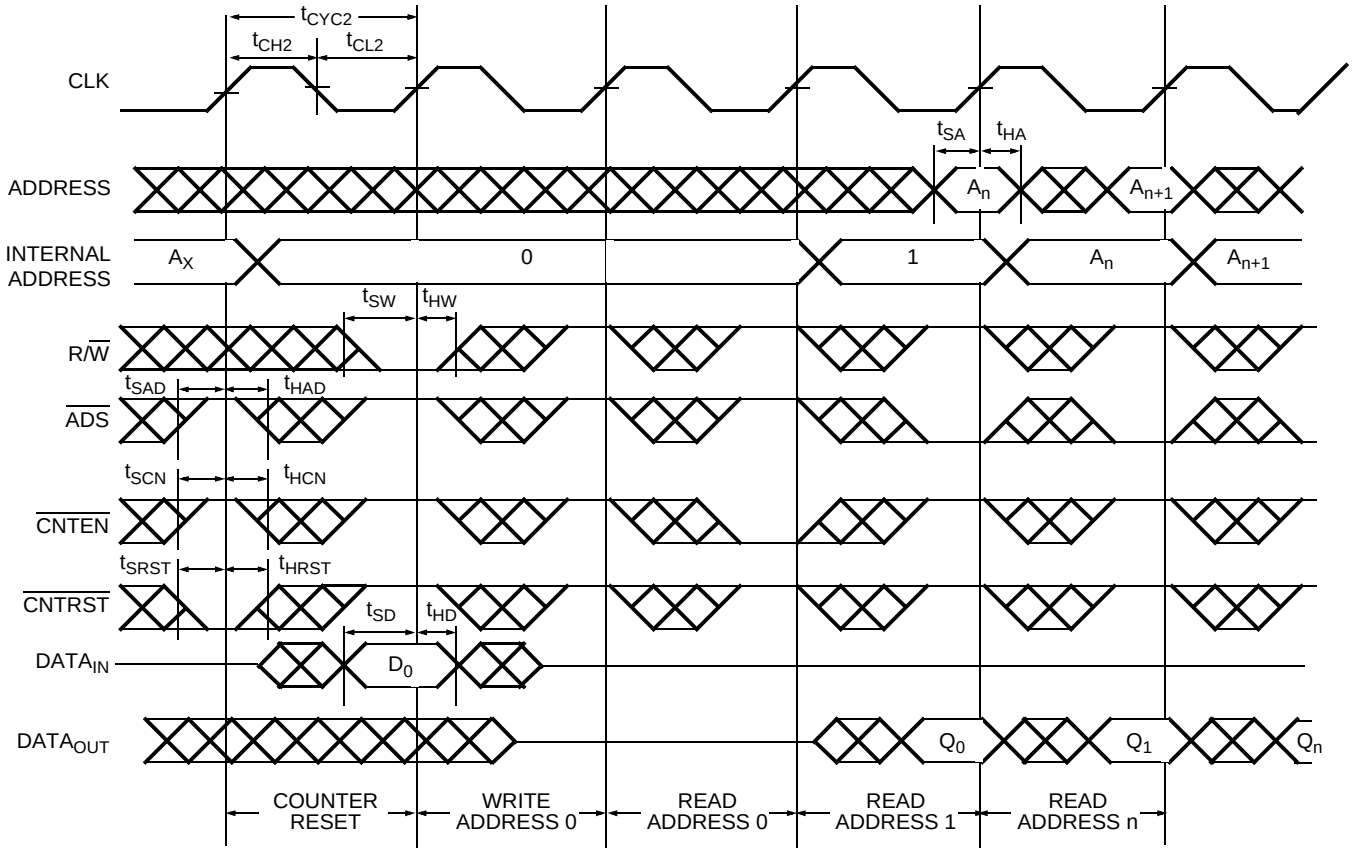
Figure 12. Write with Address Counter Advance (Flow-through or Pipelined Outputs)[25, 26]



Notes
25. $\overline{CE_0}$, $\overline{UB}$, $\overline{LB}$, and R/$\overline{W}$ = V_{IL}; CE_1 and $\overline{CNTRST}$ = V_{IH}.
26. The “Internal Address” is equal to the “External Address” when $\overline{ADS}$ = V_{IL} and equals the counter output when $\overline{ADS}$ = V_{IH}.

Switching Waveforms *(continued)*

Figure 13. Counter Reset (Pipelined Outputs)[27, 28, 29, 30]



Notes
27. Addresses do not have to be accessed sequentially since $\overline{ADS}$ = V_{IL} constantly loads the address on the rising edge of the CLK. Numbers are for reference only.
28. Output state (HIGH, LOW, or high-impedance) is determined by the previous cycle control signals.
29. CE_0, $\overline{UB}$, and $\overline{LB}$ = V_{IL}; CE_1 = V_{IH}.
30. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset.

Read/Write and Enable Operation[31, 32, 33]

Inputs					Outputs	Operation
$\overline{OE}$	CLK	$\overline{CE_0}$	CE_1	R/$\overline{W}$	I/O_0–I/O_{17}	
X	↑	H	X	X	High Z	Deselected[34]
X	↑	X	L	X	High Z	Deselected[34]
X	↑	L	H	L	D_{IN}	Write
L	↑	L	H	H	D_{OUT}	Read[34]
H	X	L	H	X	High Z	Outputs disabled

Address Counter Control Operation[31, 35, 36, 37]

Address	Previous Address	CLK	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{CNTRST}$	I/O	Mode	Operation
X	X	↑	X	X	L	$D_{out(0)}$	Reset	Counter reset to address 0
A_n	X	↑	L	X	H	$D_{out(n)}$	Load	Address load into counter
X	A_n	↑	H	H	H	$D_{out(n)}$	Hold	External address blocked—counter disabled
X	A_n	↑	H	L	H	$D_{out(n+1)}$	Increment	Counter enabled—internal address generation

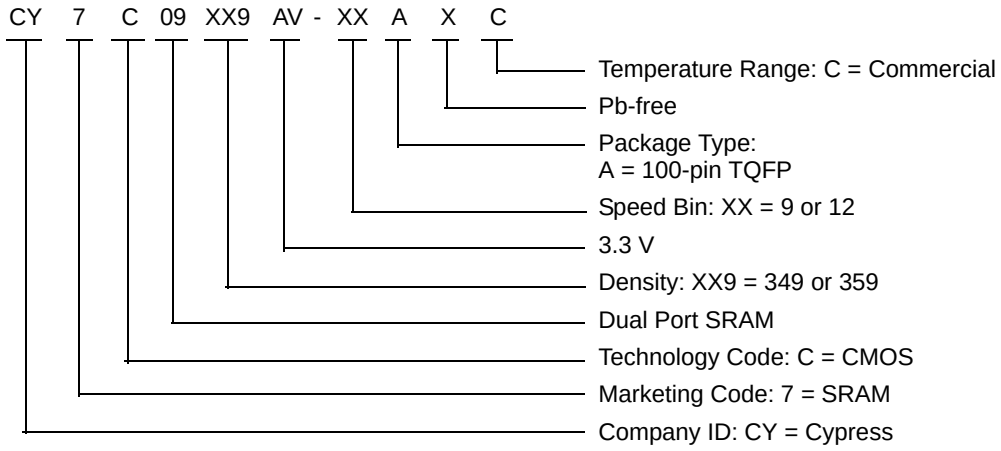
Notes
31. "X" = "Don't Care," "H" = V_{IH}, "L" = V_{IL}.
32. $\overline{ADS}$, $\overline{CNTEN}$, $\overline{CNTRST}$ = "Don't Care."
33. $\overline{OE}$ is an asynchronous input signal.
34. When $\overline{CE}$ changes state in the pipelined mode, deselection and read happen in the following clock cycle.
35. $\overline{CE_0}$ and $\overline{OE}$ = V_{IL}; CE_1 and R/$\overline{W}$ = V_{IH}.
36. Data shown for flow-through mode; pipelined mode output will be delayed by one cycle.
37. Counter operation is independent of $\overline{CE_0}$ and CE_1.

Ordering Information

4 K × 18 3.3 V Synchronous Dual-Port SRAM

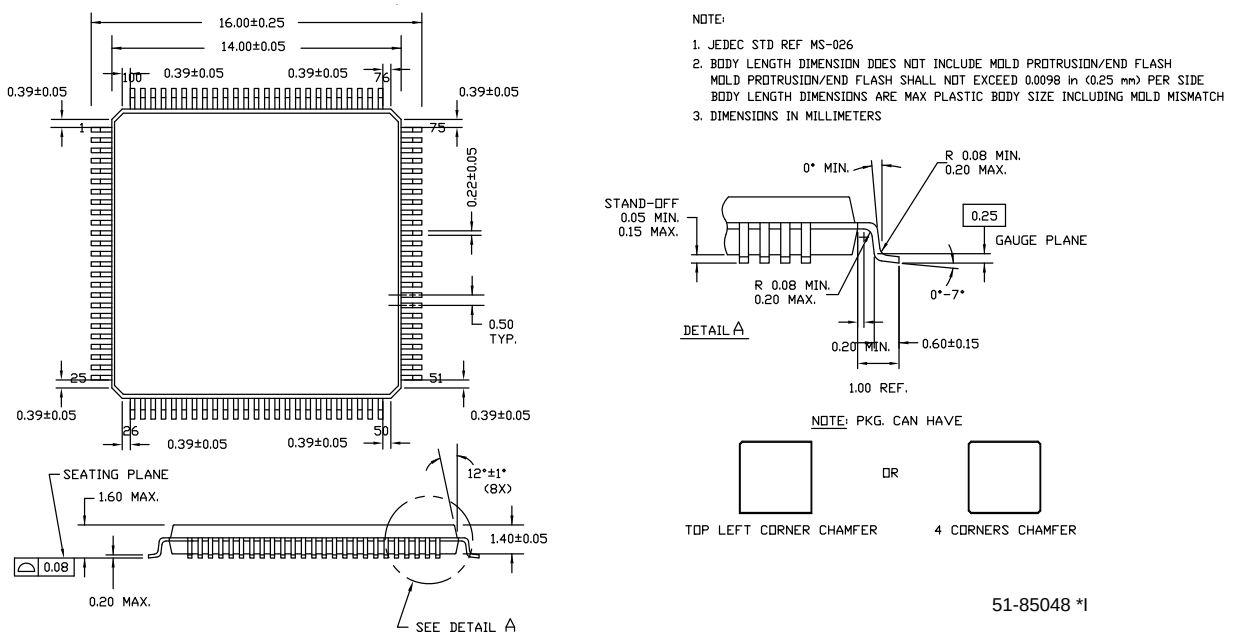
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
9	CY7C09349AV-9AXC	A100	100-pin Pb-free Thin Quad Flat Pack	Commercial
12	CY7C09349AV-12AXC	A100	100-pin Pb-free Thin Quad Flat Pack	Commercial

Ordering Code Definitions



Package Diagram

Figure 14. 100-pin TQFP (14 × 14 × 1.4 mm) A100SA Package Outline, 51-85048



Acronyms

Acronym	Description
CE	chip enable
CLK	clock
CMOS	complementary metal oxide semiconductor
I/O	Input/output
OE	output enable
SRAM	static random access memory
TQFP	thin quad flat pack

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microamperes
mA	milliamperes
mV	millivolts
mW	milliwatts
ns	nanoseconds
pF	picofarad
V	volts
W	watts

Document History Page

Document Title: CY7C09349AV/CY7C09359AV, 3.3 V 4 K/8 K × 18 Synchronous Dual Port Static RAM Document Number: 001-63888				
Rev.	**ECN No.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	2998931	09/16/2010	RAME	New data sheet.
*A	3386551	09/28/2011	ADMU	Updated footnotes. Updated Package Diagram.
*B	4547288	10/21/2014	ADMU	Updated Ordering Information: Updated part numbers. Updated Package Diagram: spec 51-85048 – Changed revision from *E to *I. Updated to new template.
*C	4580426	11/25/2014	ADMU	Added related documentation hyperlink in page 1.

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