RDA5807M

SINGLE-CHIP BROADCAST FM RADIO TUNER

Rev.1.1–July.2011

1 General Description

The RDA5807M series is the newest generation single-chip broadcast FM stereo radio tuner with fully integrated synthesizer, IF selectivity, RDS/RBDS and MPX decoder. The tuner uses the CMOS process, support multi-interface and require the least external component. All these make it very suitable for portable devices.

The RDA5807M series has a powerful low-IF digital audio processor, this make it have optimum sound quality with varying reception conditions.

The RDA5807M series support frequency range is from 50MHz to 115MHz.

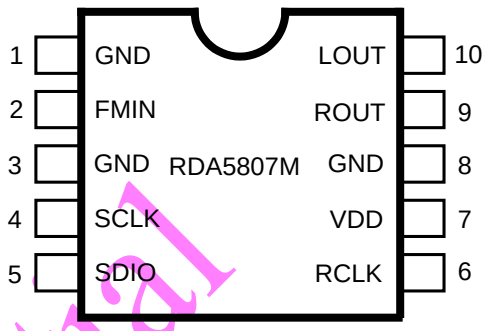


Figure1-1. RDA5807M Top View

1.1 Features

- CMOS single-chip fully-integrated FM tuner
- Low power consumption
  - Total current consumption lower than 20mA at 3.0V power supply when under normal situation
- Support worldwide frequency band
  - 50 -115 MHz
- Support flexible channel spacing mode
  - 100KHz, 200KHz, 50KHz and 25KHz
- Support RDS/RBDS
- Digital low-IF tuner
  - Image-reject down-converter
  - High performance A/D converter
  - IF selectivity performed internally
- Fully integrated digital frequency synthesizer
  - Fully integrated on-chip RF and IF VCO
  - Fully integrated on-chip loop filter
- Autonomous search tuning
- Support 32.768KHz crystal oscillator
- Digital auto gain control (AGC)
- Digital adaptive noise cancellation
  - Mono/stereo switch
  - Soft mute
  - High cut
- Programmable de-emphasis (50/75 μs)
- Receive signal strength indicator (RSSI) and SNR
- Bass boost
- Volume control and mute
- Line-level analog output voltage
- 32.768 KHz 12M,24M,13M,26M,19.2M,38.4MHz Reference clock
- Only support 2-wire bus interface
- Directly support 32Ω resistance loading
- Integrated LDO regulator
  - 2.7 to 3.3 V operation voltage
- MSOP－10pins

1.2 Applications

- Cellular handsets
- MP3, MP4 players
- Portable radios
- PDAs, Notebook

Table of Contents

2 Functional Description

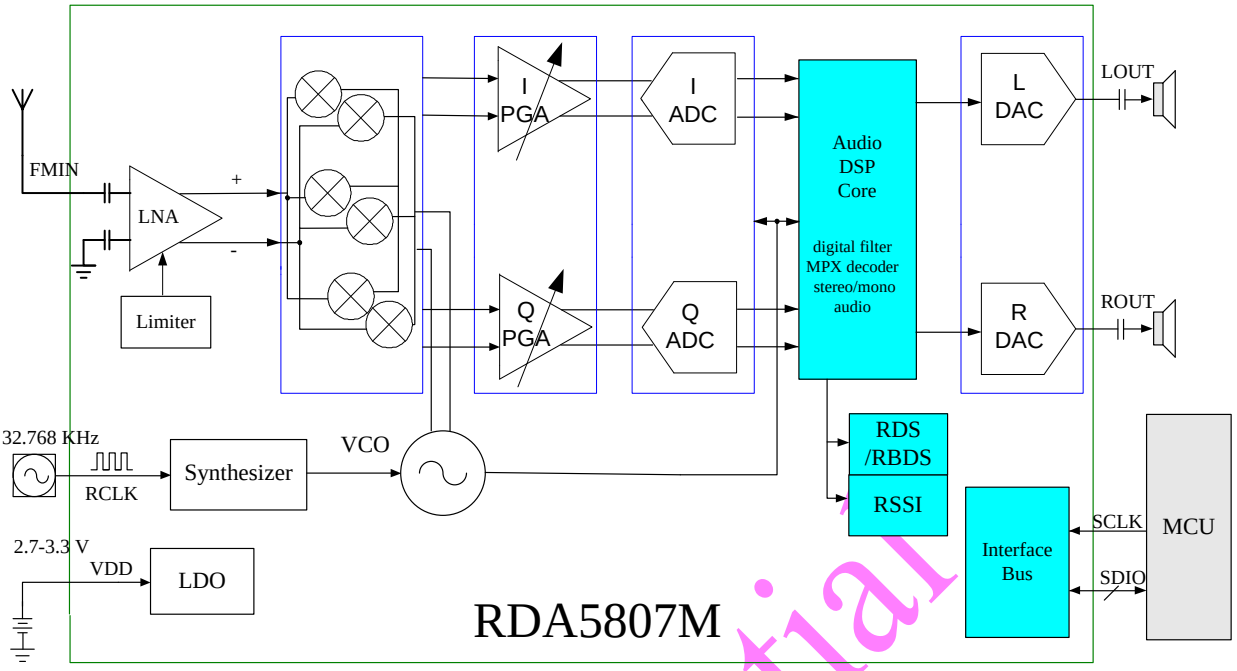


Figure 2-1. RDA5807M FM Tuner Block Diagram

2.1 FM Receiver

The receiver uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering lower solution cost and reduces complexity, and integrates a low noise amplifier (LNA) supporting the FM broadcast band (50 to 115MHz), a multi-phase image-reject mixer array, a programmable gain control (PGA), a high resolution analog-to-digital converters (ADCs), an audio DSP and a high-fidelity digital-to-analog converters (DACs).

The limiter prevents overloading and limits the amount of intermodulation products created by strong adjacent channels.

The multi-phase mixer array down converts the LNA output differential RF signal to low-IF, it also has image-reject function and harmonic tones rejection.

The PGA amplifies the mixer output IF signal and then digitized with ADCs.

The DSP core finishes the channel selection, FM demodulation, stereo MPX decoder and output audio signal. The MPX decoder can autonomous switch from stereo to mono to limit the output noise.

The DACs convert digital audio signal to analog and change the volume at same time. The DACs has low-pass feature and -3dB frequency is about 30 KHz.

2.2 Synthesizer

The frequency synthesizer generates the local oscillator signal which divide to multi-phase, then be used to downconvert the RF input to a constant low intermediate frequency (IF). The synthesizer reference clock is 32.768 KHz.

The synthesizer frequency is defined by bits CHAN[9:0] with the range from 50MHz to 115MHz.

2.3 Power Supply

The RDA5807M integrated one LDO which supplies power to the chip. The external supply voltage range is 2.7-3.3 V.

2.4 RESET and Control Interface select

The RDA5807M is RESET itself When VDD is Power up. And also support soft reset by trigger 02H BIT1 from 0 to 1. The RDA5807M only support **I²C** control interface bus mode.

2.5 Control Interface

The RDA5807M only supports I²C control interface.

The I²C interface is compliant to I²C Bus Specification 2.1. It includes two pins: SCLK and SDIO. A I²C interface transfer begins with START condition, a command byte and data bytes, each byte has a followed ACK (or NACK) bit, and ends with STOP condition. The command byte includes a 7-bit chip address (0010000b) and a R/W bit. The ACK (or NACK) is always sent out by receiver. When in write transfer, data bytes is written out from MCU, and when in read transfer, data bytes is read out from RDA5807M. There is no visible register address in I²C interface transfers. The I²C interface has a fixed start register address (0x02h for write transfer and 0x0Ah for read transfer), and an internal incremental address counter. If register address meets the end of register file, 0x3Ah, register address will wrap back to 0x00h. For write transfer, MCU programs registers from register 0x02h high byte, then register 0x02h low byte, then register 0x03h high byte, till the last register. RDA5807M always gives out ACK after every byte, and MCU gives out STOP condition when register programming is finished. For read transfer, after command byte from MCU, RDA5807M sends out register 0x0Ah high byte, then register 0x0Ah low byte, then register 0x0Bh high byte, till receives NACK from MCU. MCU gives out ACK for data bytes besides last data byte. MCU gives out NACK for last data byte, and then RDA5807M will return the bus to MCU, and MCU will give out STOP condition.

3 Electrical Characteristics

Table 3-1 DC Electrical Specification (Recommended Operation Conditions):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VDD	Supply Voltage	2.7	3.0	3.3	V
T_{amb}	Ambient Temperature	-20	27	+75	℃
V_{IL}	CMOS Low Level Input Voltage	0		0.3*VDD	V
V_{IH}	CMOS High Level Input Voltage	0.7*VDD		VDD	V
V_{TH}	CMOS Threshold Voltage		0.5*VDD		V

Table 3-2 DC Electrical Specification (Absolute Maximum Ratings):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{amb}	Ambient Temperature	-40		+90	°C
I_{IN}	Input Current (1)	-10		+10	mA
V_{IN}	Input Voltage(1)	-0.3		VDD+0.3	V
V_{Ina}	FM Input Level			+10	dBm

Notes:

1. For Pin: SCLK, SDIO

Table 3-3 Power Consumption Specification

(VDD = 3 V, T_A = 25℃, unless otherwise specified)

SYMBOL	DESCRIPTION	CONDITION	TYP	UNIT
I_{VDD}	Supply Current(1)	ENABLE=1	20	mA
I_{VDD}	Supply Current(2)	ENABLE=1	21	mA
I_{PD}	Powerdown Current	ENABLE=0	15	μA

Notes:

1. **For strong input signal condition**
2. **For weak input signal condition**

4 Receiver Characteristics

Table 4-1 Receiver Characteristics

(VDD = 3 V, T_A = 25 °C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
General specifications							
F_{in}	FM Input Frequency Range	Adjust BAND Register		50		115	MHz
V_{rf}	Sensitivity[1,2,3]	S/N=26dB	50MHz	-	1.4	1.8	μV EMF
			65MHz	-	1.2	1.5	
			88MHz	-	1.2	1.5	
			98MHz	-	1.3	1.5	
			108MHz	-	1.3	1.5	
			115MHz	-	1.3	1.8	
$IP3_{in}$	Input IP3[4]	AGCD=1		80	-	-	dBμV
α_{am}	AM Suppression[1,2]	m=0.3		60	-	-	dB
S_{200}	Adjacent Channel Selectivity	±200KHz		50	70	-	dB
S_{400}	400KHz Selectivity	±400KHz		60	85	-	dB
V_{AFL}; V_{AFR}	Audio L/R Output Voltage[1,2] (Pins LOUT and ROUT)	Volume [3:0] =1111		-	360	-	mV
S/N	Maximum Signal to Noise Ratio[1,2,3,5]		Mono[2]	55	57	-	dB
			Stereo[6]	53	55	-	
α_{SCS}	Stereo Channel Separation			35	-	-	dB
R_L	Audio Output Loading Resistance	Single-ended		32	-	-	Ω
THD	Audio Total Harmonic Distortion[1,3,6]	Volume[3:0] =1111	R_{load}=1KΩ	-	0.15	0.2	%
			R_{load}=32Ω	-	0.2	-	
α_{AOI}	Audio Output L/R Imbalance[1,6]			-	-	0.05	dB
R_{mute}	Mute Attenuation Ratio[1]	Volume[3:0]=0000		60	-	-	dB
BW_{audio}	Audio Response[1]	1KHz=0dB ±3dB point	Low Freq[9]	-	100	-	Hz
			High Freq	-	14	-	
Pins FMIN, LOUT, ROUT							
V_{com_rfin}	Pins FMIN Input Common Mode Voltage				0		V
V_{com}	Audio Output Common Mode Voltage[8]			1.0	1.05	1.1	V

Notes: 1. F_{in}=65 to 115MHz; F_{mod}=1KHz; de-emphasis=75μs; MONO=1; L=R unless noted otherwise;

2. Δf=22.5KHz; 3. B_{AF} = 300Hz to 15KHz, RBW <=10Hz; 4. $|f_2-f_1|>1$MHz, $f_0=2xf_1-f_2$, AGC disable, F_{in}=76 to 108MHz;
5. P_{RF}=60dB$_U$V; 6. Δf=75KHz,fpilot=10% 7. Measured at V_{EMF} = 1 m V, f_{RF} = 65 to 108MHz
8. At LOUT and ROUT pins 9. Adjustable

5 Serial Interface

5.1 I²C Interface Timing

Table 5-1 I²C Interface Timing Characteristics

(VDD = 3 V, T_A = 25 °C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SCLK Frequency	f_{scl}		0	-	400	KHz
SCLK High Time	t_{high}		0.6	-	-	µs
SCLK Low Time	t_{low}		1.3	-	-	µs
Setup Time for START Condition	$t_{su:sta}$		0.6	-	-	µs
Hold Time for START Condition	$t_{hd:sta}$		0.6	-	-	µs
Setup Time for STOP Condition	$t_{su:sto}$		0.6	-	-	µs
SDIO Input to SCLK↑ Setup	$t_{su:dat}$		100	-	-	ns
SDIO Input to SCLK↓ Hold	$t_{hd:dat}$		0	-	900	ns
STOP to START Time	t_{buf}		1.3	-	-	µs
SDIO Output Fall Time	$t_{f:out}$		20+0.1C_b	-	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{r:in}$ / $t_{f:in}$		20+0.1C_b	-	300	ns
Input Spike Suppression	t_{sp}		-	-	50	ns
SCLK, SDIO Capacitive Loading	C_b		-	-	50	pF
Digital Input Pin Capacitance					5	pF

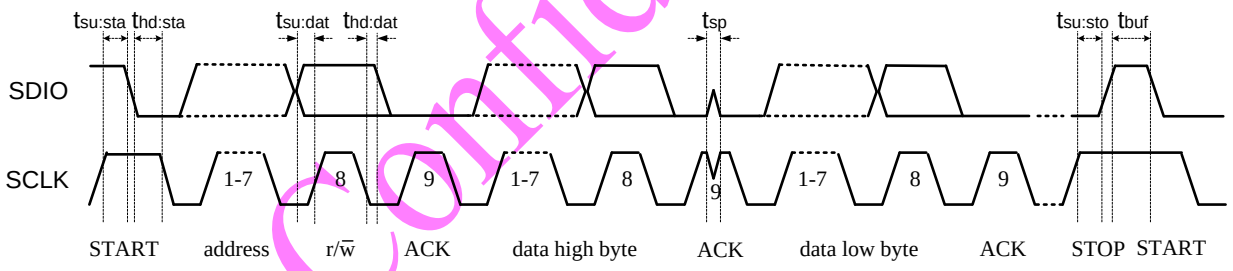


Figure 5-1. I²C Interface Write Timing Diagram

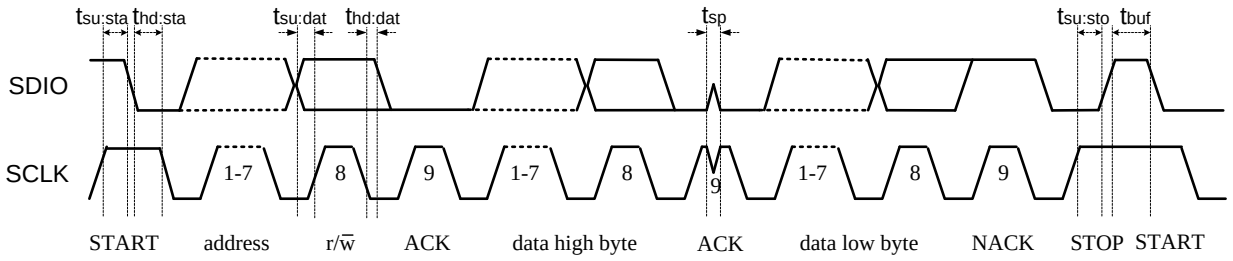


Figure 5-2. I²C Interface Read Timing Diagram

6 Register Definition

REG	BITS	NAME	FUNCTION	DEFAULT
00H	15:8	CHIPID[7:0]	Chip ID.	0x58
02H	15	DHIZ	Audio Output High-Z Disable. *0 = High impedance; 1 = Normal operation*	0
	14	DMUTE	Mute Disable. *0 = Mute; 1 = Normal operation*	0
	13	MONO	Mono Select. *0 = Stereo; 1 = Force mono*	0
	12	BASS	Bass Boost. *0 = Disabled; 1 = Bass boost enabled*	0
	11	RCLK NON-CALIBRATE MODE	0=RCLK clock is always supply 1=RCLK clock is not always supply when FM work (when 1, RDA5807M can't directly support -20℃~70℃ temperature. Only suppory ±20℃ temperature swing from tune point)	0
	10	RCLK DIRECT INPUT MODE	1=RCLK clock use the directly input mode	0
	9	SEEKUP	Seek Up. *0 = Seek down; 1 = Seek up*	0
	8	SEEK	Seek. *0 = Disable stop seek; 1 = Enable* *Seek begins in the direction specified by* SEEKUP *and ends when a channel is found, or the entire band has been searched.* *The* SEEK *bit is set low and the* STC *bit is set high when the seek operation completes.*	0
	7	SKMODE	Seek Mode 0 = wrap at the upper or lower band limit and continue seeking 1 = stop seeking at the upper or lower band limit	0
	6:4	CLK_MODE[2:0]	000=32.768kHz 001=12Mhz 101=24Mhz 010=13Mhz 110=26Mhz 011=19.2Mhz 111=38.4Mhz	000
	3	RDS_EN	RDS/RBDS enable If 1, rds/rbds enable	0
	2	NEW_METHOD	New Demodulate Method Enable, can improve the receive sensitivity about 1dB.	0
	1	SOFT_RESET	Soft reset. If 0, not reset; If 1, reset.	0

REG	BITS	NAME	FUNCTION	DEFAULT
	0	**ENABLE**	**Power Up Enable.** ***0 = Disabled; 1 = Enabled***	0
03H	**15:6**	**CHAN[9:0]**	**Channel Select.** **BAND =** ***0*** ***Frequency =*** ***Channel Spacing (kHz) x* CHAN+ *87.0 MHz*** **BAND =** ***1or 2*** ***Frequency =*** ***Channel Spacing (kHz) x* CHAN + *76.0 MHz*** **BAND =** ***3*** ***Frequency =*** ***Channel Spacing (kHz) x* CHAN + *65.0 MHz*** **CHAN** ***is updated after a seek operation.***	0x00
	5	**DIRECT MODE**	**Directly Control Mode, Only used when test.**	0
	4	**TUNE**	**Tune** **0 = Disable** **1 = Enable** **The tune operation begins when the TUNE bit is set high. The STC bit is set high when the tune operation completes.** **The tune bit is reset to low automatically when the tune operation completes..**	0
	3:2	**BAND[1:0]**	**Band Select.** **00 = 87–108 MHz (US/Europe)** **01 = 76–91 MHz (Japan)** **10 = 76–108 MHz (world wide)** **11[1] = 65 –76 MHz （East Europe） or 50-65MHz**	00
	1:0	**SPACE[1:0]**	**Channel Spacing.** **00 = 100 kHz** **01 = 200 kHz** **10 = 50kHz** **11 = 25KHz**	00
04H	**15**	**RSVD**	**Reserved**	0
	13:12	**RSVD**	**Reserved**	00
	11	**DE**	**De-emphasis.** ***0 = 75 μs; 1 = 50 μs***	0
	10	**RSVD**	**Reserved**	
	9	**SOFTMUTE_EN**	**If 1, softmute enable**	1
	8	**AFCD**	**AFC disable.** **If 0, afc work;** **If 1, afc disabled.**	0
05H	**15**	**INT _MODE**	**If 0, generate 5ms interrupt;** **If 1, interrupt last until read reg0CH action occurs.**	1

[1] If 0x07h_bit<9> (band)=1, 65-76MHz; =0, 50-76MHz

REG	BITS	NAME	FUNCTION	DEFAULT
	14:12	RSVD	Reserved	000
	11:8	SEEKTH[3:0][2]	Seek SNR threshold value	1000
	5:4	RSVD	Resvered	00
	3:0	VOLUME[3:0]	DAC Gain Control Bits (Volume). 0000=min; 1111=max Volume scale is logarithmic When 0000, output mute and output impedance is very large	1111
06H	15	RSVD	reserved	0
	14:13	OPEN_MODE[1:0]	Open reserved register mode. 11=open behind registers writing function others: only open behind registers reading function	00
07H	15	RSVD	Reserved	0
	14:10	TH_SOFRBLEND[5:0]	Threshold for noise soft blend setting, unit 2dB	10000
	9	65M_50M MODE	Valid when band[1:0] = 2'b11 (0x03H_bit<3:2>) 1 = 65~76 MHz; 0 = 50~76 MHz.	1
	8	RSVD	Reserved	0
	7:2	SEEK_TH_OLD[3]	Seek threshold for old seek mode, Valid when Seek_Mode=001	000000
	1	SOFTBLEND_EN	If 1, Softblend enable	1
	0	FREQ_MODE	If 1, then freq setting changed. Freq = 76000(or 87000) kHz + freq_direct (08H) kHz.	0
0AH	15	RDSR	RDS ready 0 = No RDS/RBDS group ready(default) 1 = New RDS/RBDS group ready	0
	14	STC	Seek/Tune Complete. 0 = Not complete 1 = Complete The seek/tune complete flag is set when the seek or tune operation completes.	0
	13	SF	Seek Fail. *0 = Seek successful; 1 = Seek failure* *The seek fail flag is set when the seek operation fails to find a channel with an* RSSI *level greater than* SEEKTH[5:0].	0
	12	RDSS	RDS Synchronization 0 = RDS decoder not synchronized(default) 1 = RDS decoder synchronized Available only in RDS Verbose mode	0
	11	BLK_E	When RDS enable:	0

[2] This value is SNR threshold for seeking, and the default value 1000 is about 32dB SNR.
[3] 0x20H_bit<14:12>, Seek_Mode register. Default value is 000; When = 001, will add the 5802E seek mode.

REG	BITS	NAME	FUNCTION	DEFAULT
			1 = Block E has been found **0 = no Block E has been found**	
	10	**ST**	**Stereo Indicator.** ***0 = Mono; 1 = Stereo***	1
	9:0	**READCHAN[9:0]**	**Read Channel.** **BAND = 0** **Frequency = Channel Spacing (kHz) x READCHAN[9:0]+ 87.0 MHz** **BAND = 1 or 2** **Frequency = Channel Spacing (kHz) x READCHAN[9:0]+ 76.0 MHz** **BAND = 3** **Frequency = Channel Spacing (kHz) x READCHAN[9:0]+ 65.0 MHz** **READCHAN[9:0] is updated after a tune or seek operation.**	8'h00
0BH	**15:9**	**RSSI[6:0]**	**RSSI.** **000000 = min** **111111 = max** **RSSI scale is logarithmic.**	0
	8	**FM TRUE**	**1 = the current channel is a station** **0 = the current channel is not a station**	0
	7	**FM_READY**	**1=ready** **0=not ready**	0
	<6:5>	**reserved**		0
	<4>	**ABCD_E**	**1= the block id of register 0cH,0dH,0eH,0fH is E** **0= the block id of register 0cH, 0dH, 0eH,0fH is A, B, C, D**	
	<3:2>	**BLERA[1:0]**	**Block Errors Level of RDS_DATA_0, and is always read as Errors Level of RDS BLOCK A (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1)** **00= 0 errors requiring correction** **01= 1~2 errors requiring correction** **10= 3~5 errors requiring correction** **11= 6+ errors or error in checkword, correction not possible.** **Available only in RDS Verbose mode**	
	<1:0>	**BLERB[1:0]**	**Block Errors Level of RDS_DATA_1, and is always read as Errors Level of RDS BLOCK B (in RDS mode) or E (in RBDS mode when ABCD_E flag is 1).** **00= 0 errors requiring correction** **01= 1~2 errors requiring correction** **10= 3~5 errors requiring correction**	

REG	BITS	NAME	FUNCTION	DEFAULT
			11= 6+ errors or error in checkword, correction not possible. **Available only in RDS Verbose mode**	
0CH	**<15:0>**	**RDSA[15:0]**	**BLOCK A (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1)**	16'h5803
0DH	**<15:0>**	**RDSB[15:0]**	**BLOCK B (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1)**	16'h5804
0EH	**<15:0>**	**RDSC[15:0]**	**BLOCK C (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1)**	16'h5808
0FH	**<15:0>**	**RDSD[15:0]**	**BLOCK D (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1)**	16'h5804

7 Pins Description

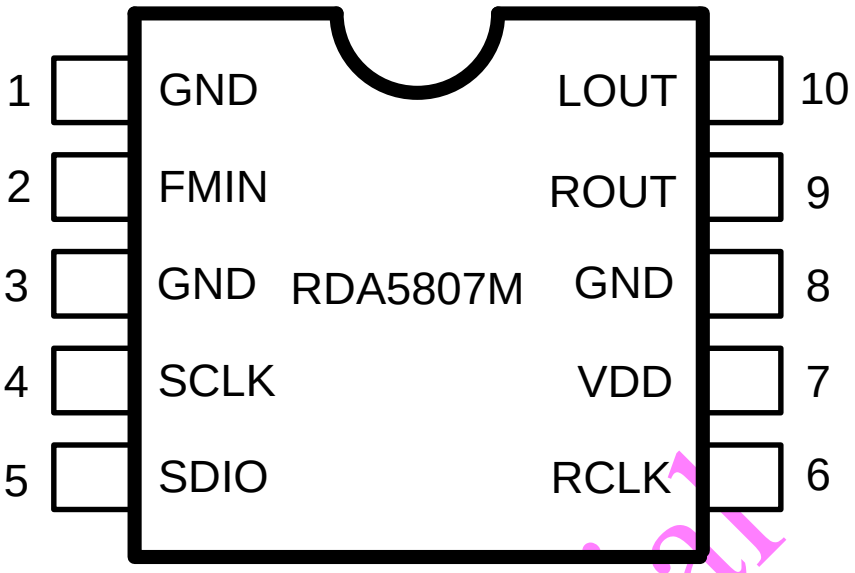
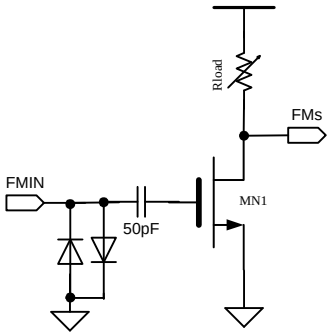
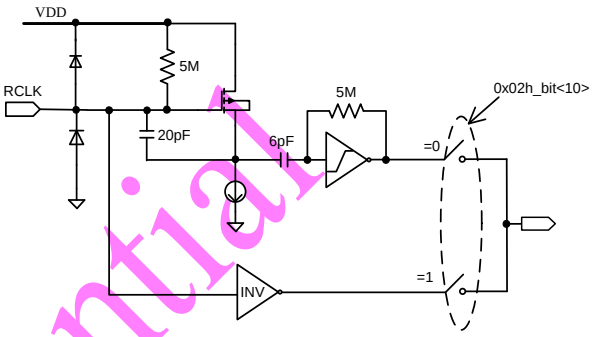
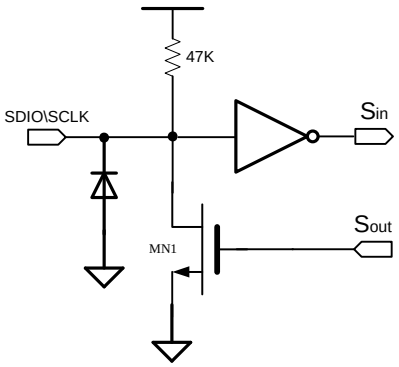


Figure 7-1. RDA5807M Top View

Table 7-1 RDA5807M Pins Description

SYMBOL	PIN	DESCRIPTION
GND	1,3,8	Ground. Connect to ground plane on PCB
FMIN	2	FM single input
RCLK	6	32.768KHz crystal oscillator and reference clock input
SDIO	5	Data input/output for serial control bus
SCLK	4	Clock input for serial control bus
VDD	7	Power supply
ROUT,LOUT	9,10	Right/Left audio output

Table 7-2 Internal Pin Configuration

SYMBOL	PIN	DESCRIPTION
FMIN	2	
RCLK	6	
SDIO /SCLK	5/4	

8 Application Diagram

8.1 Audio Loading Resistance Larger than 32Ω & Reference Clock Application:

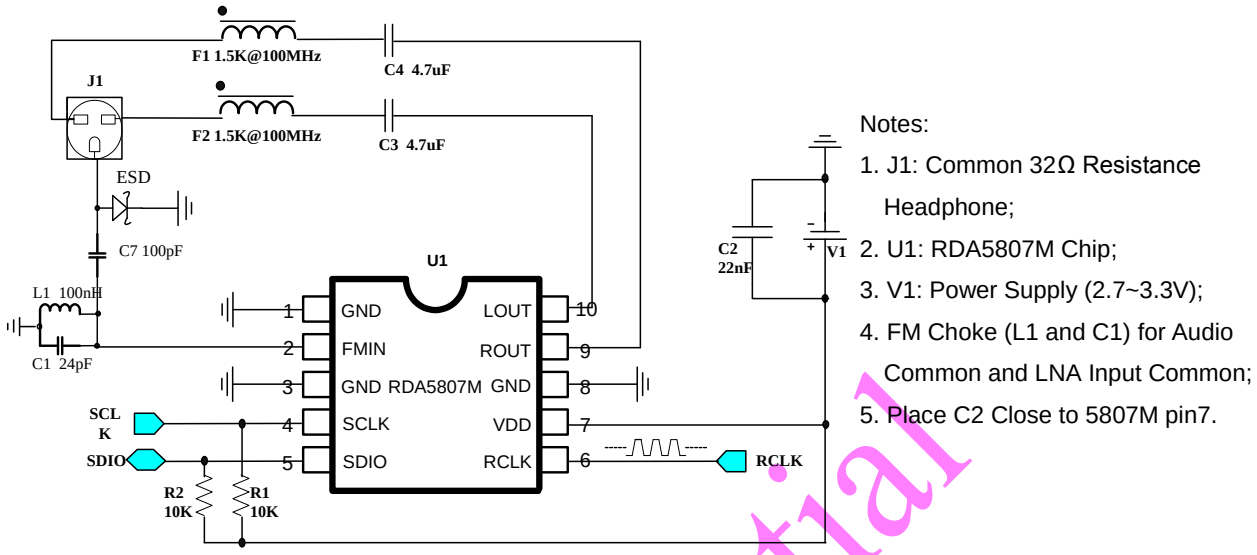
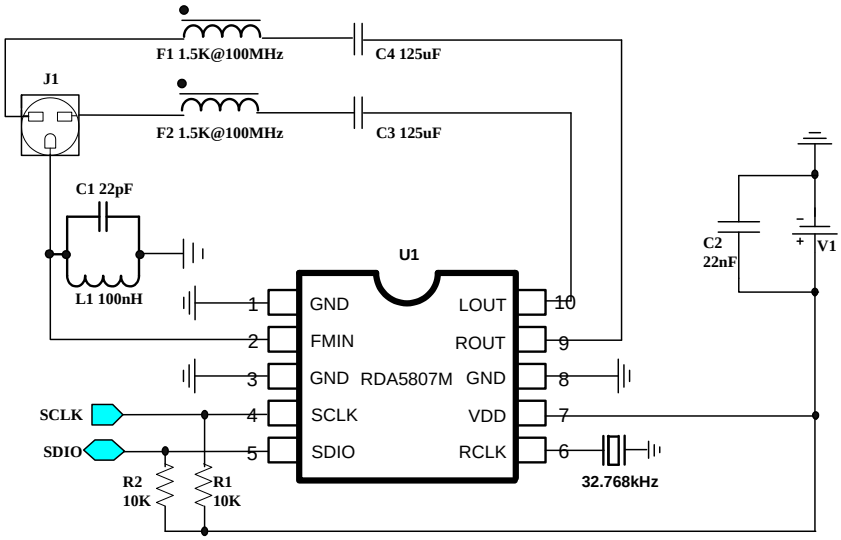


Figure 8-1. RDA5807M FM Tuner Application Diagram (Reference Clock Application)

8.1.1 Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5807M	Broadcast FM Radio Tuner	RDA
J1		Common 32Ω Resistance Headphone	
L1/C1	100nH/24pF	LC Chock for FMIN Input	Murata
C3,C4	4.7μF	Audio AC Couple Capacitors	Murata
C2	22nF	Power Supply Bypass Capacitor	Murata
C7	100pF	AC Couple Capacitors	Murata
ESD		TVS	
F1/F2	1.5K@100MHz	FM Band Ferrite	Murata
R1,R2	10KΩ	I^2C Bus Pull-up Resister	Murata

8.2 Audio Loading Resistance Larger than 32Ω & DCXO Application:



Notes:

1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5807M Chip;
3. V1: Power Supply (2.7~3.3V);
4. FM Choke (L1 and C1) for Audio Common and LNA Input Common;
5. Place C2 Close to 5807M pin7.

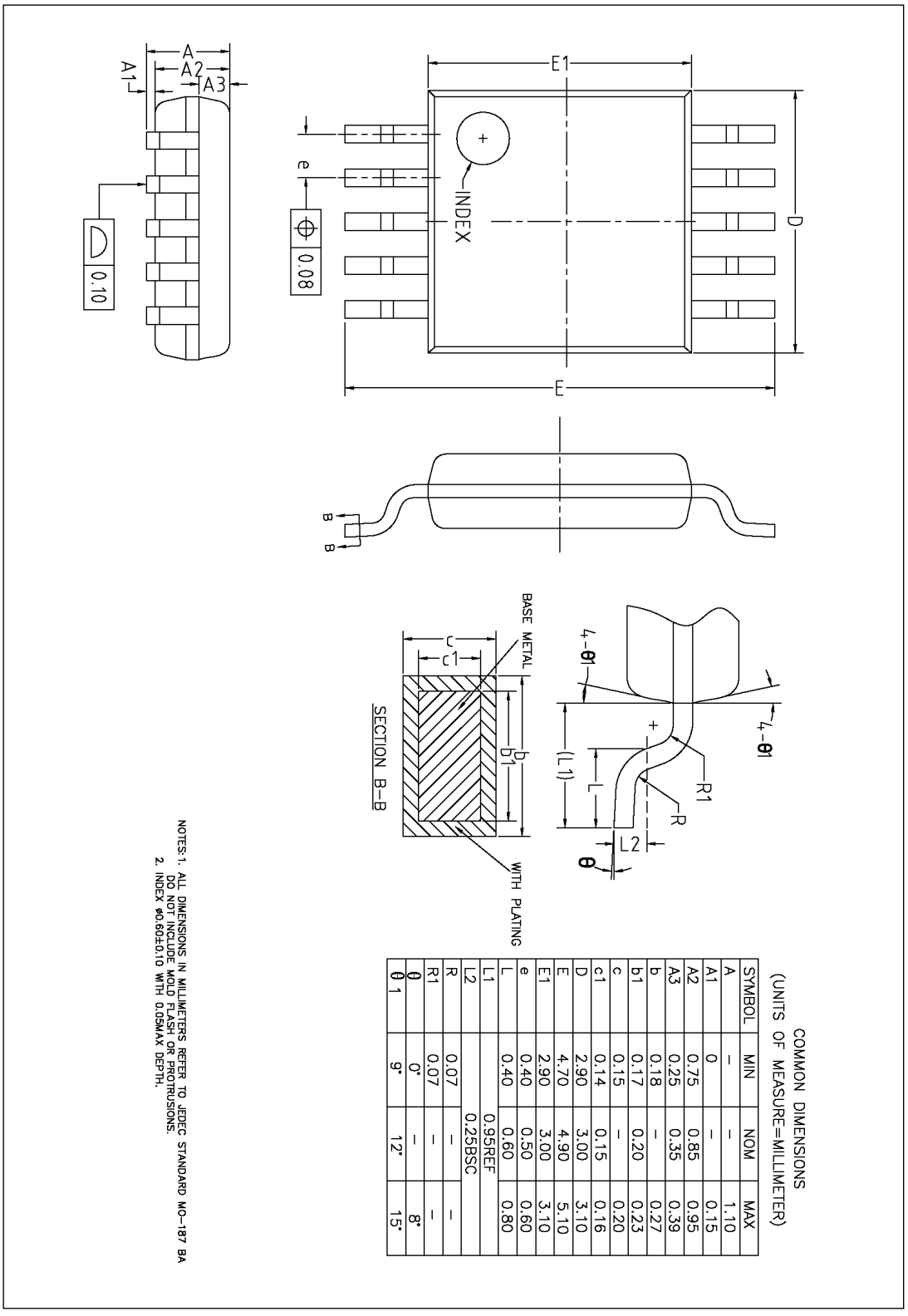
Figure 8-2. RDA5807M FM Tuner Application Diagram (32.768K crystal)

8.2.1 Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5807M	Broadcast FM Radio Tuner	RDA
J1		Common 32Ω Resistance Headphone	
L1/C1	100nH/22pF	LC Chock for FMIN Input	Murata
C3,C4	125μF	Audio AC Couple Capacitors	Murata
C2	22nF	Power Supply Bypass Capacitor	Murata
F1/F2	1.5K@100MHz	FM Band Ferrite	Murata
R1,R2	10KΩ	I^2C Bus Pull-up Resister	Murata

9 Physical Dimension

Figure 9-1 illustrates the package details for the RDA5807M. The package is lead-free and RoHS-compliant.



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.10
A1	0	–	0.15
A2	0.75	0.85	0.95
A3	0.25	0.35	0.39
b	0.18	–	0.27
b1	0.17	0.20	0.23
c	0.15	–	0.20
c1	0.14	0.15	0.16
D	2.90	3.00	3.10
E	4.70	4.90	5.10
E1	2.90	3.00	3.10
e	0.40	0.50	0.60
L	0.40	0.60	0.80
L1		0.95REF	
L2		0.25BSC	
R	0.07	–	–
R1	0.07	–	–
θ	0°	–	8°
θ1	9°	12°	15°

Figure 9-1. 10-Pin MSOP

10 PCB Land Pattern

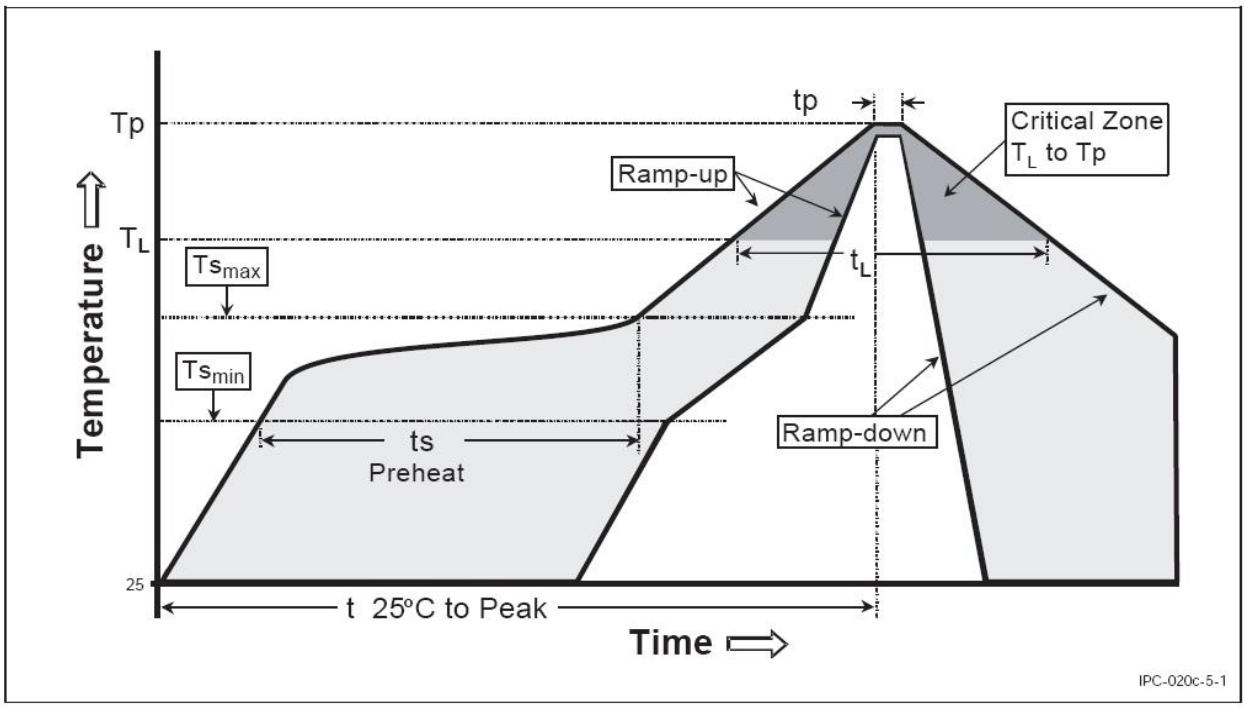


Figure 10-1.Classification Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (T_{Smax} to T_p)	3 °C/second max.	3 °C/second max.
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (t_{smin} to t_{smax})	 100 °C 100 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: -Temperature (T_L) -Time (t_L)	 183 °C 60-150seconds	 217°C 60-150 seconds
Peak /Classification Temperature(T_p)	See Table-II	See Table-III
Time within 5 °C of actual Peak Temperature (t_p)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Table-I Classification Reflow Profiles

Package Thickness	Volume mm^3 <350	Volume mm^3 ⩾350
＜2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
⩾2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

Table – II SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 ＜350	Volume mm^3 350-2000	Volume mm^3 ＞2000
＜1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
⩾2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *
*Tolerance : The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.			

Table – III Pb-free Process – Package Classification Reflow Temperatures

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever

is required to control the profile process but at no time will it exceed - 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table –III.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a “lead-free” assembly process **shall** be evaluated using the “lead free” classification temperatures and profiles defined in Table-I II III whether or not lead free.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

Change List

REV	DATE	AUTHER	CHANGE DESCRIPTION
V1.0	2011-05-23	Chun Zhao	Original Draft.

11 Notes：

12 Contact Information

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