

## 1. General description

AC Thyristor Triac power switch in a SOT404 (D2PAK) surface mountable plastic package with self-protective clamping capabilities against low and high energy transients. This "series CTN" triac will commute the full RMS current at the maximum rated junction temperature ( $T_{j(max)} = 150\text{ °C}$ ) without the aid of a snubber. It is used in applications where "high junction operating temperature capability" is required.

## 2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- High junction operating temperature capability ( $T_{j(max)} = 150\text{ °C}$ )
- High minimum  $I_{GT}$  for guaranteed immunity to gate noise
- Full cycle AC conduction
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Protective self turn-on capability for high energy transients
- Safe clamping capability for low energy over-voltage transients
- Less sensitive gate for high noise immunity
- Surface mountable package
- Triggering in three quadrants only
- Very high immunity to false turn-on by  $dV/dt$  and IEC 61000-4-4 fast transient
- Package meets UL94V0 flammability requirement
- Package is RoHS compliant

## 3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls
- Applications subject to high temperature ( $T_{j(max)} = 150\text{ °C}$ )

## 4. Quick reference data

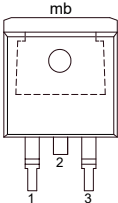
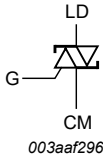
Table 1. Quick reference data

| Symbol       | Parameter                         | Conditions   | Min | Typ | Max | Unit |
|--------------|-----------------------------------|--|-----|-----|-----|------|
| $V_{DRM}$    | repetitive peak off-state voltage |  | -   | -   | 800 | V    |
| $I_{T(RMS)}$ | RMS on-state current              | full sine wave; $T_{mb} \leq 131\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a> | -   | -   | 8   | A    |

| Symbol                         | Parameter                             | Conditions  | Min  | Typ | Max | Unit |
|--------------------------------|---------------------------------------|---|------|-----|-----|------|
| I <sub>TSM</sub>               | non-repetitive peak on-state current  | full sine wave; T <sub>j(initial)</sub> = 25 °C; t <sub>p</sub> = 20 ms; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>                              | -    | -   | 80  | A    |
|                                |                                       | full sine wave; T <sub>j(initial)</sub> = 25 °C; t <sub>p</sub> = 16.7 ms   | -    | -   | 88  | A    |
| T <sub>j</sub>                 | junction temperature                  |   | -    | -   | 150 | °C   |
| V <sub>PP</sub>                | peak pulse voltage                    | T <sub>j</sub> = 25 °C; non-repetitive, off-state; <a href="#">Fig. 6</a>   | -    | -   | 2   | kV   |
| <b>Static characteristics</b>  |                                       |   |      |     |     |      |
| I <sub>GT</sub>                | gate trigger current                  | V <sub>D</sub> = 12 V; I <sub>T</sub> = 100 mA; LD+ G+; T <sub>j</sub> = 25 °C; <a href="#">Fig. 8</a>  | 5    | -   | 35  | mA   |
|                                |                                       | V <sub>D</sub> = 12 V; I <sub>T</sub> = 100 mA; LD+ G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 8</a>  | 5    | -   | 35  | mA   |
|                                |                                       | V <sub>D</sub> = 12 V; I <sub>T</sub> = 100 mA; LD- G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 8</a>  | 5    | -   | 35  | mA   |
| I <sub>H</sub>                 | holding current                       | V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>  | -    | -   | 40  | mA   |
| V <sub>T</sub>                 | on-state voltage                      | I <sub>T</sub> = 10 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a>  | -    | -   | 1.5 | V    |
| V <sub>CL</sub>                | clamping voltage                      | I <sub>CL</sub> = 0.1 mA; t <sub>p</sub> = 1 ms; T <sub>j</sub> = 25 °C   | 850  | -   | -   | V    |
| <b>Dynamic characteristics</b> |                                       |   |      |     |     |      |
| dV <sub>D</sub> /dt            | rate of rise of off-state voltage     | V <sub>DM</sub> = 536 V; T <sub>j</sub> = 125 °C; (V <sub>DM</sub> = 67% of V <sub>DRM</sub> ); exponential waveform; gate open circuit               | 4000 | -   | -   | V/μs |
|                                |                                       | V <sub>DM</sub> = 536 V; T <sub>j</sub> = 150 °C; exponential waveform; gate open circuit   | 2000 | -   | -   | V/μs |
| dI <sub>com</sub> /dt          | rate of change of commutating current | V <sub>D</sub> = 400 V; T <sub>j</sub> = 150 °C; I <sub>T(RMS)</sub> = 8 A; dV <sub>com</sub> /dt = 20 V/μs; gate open circuit; snubberless condition | 12   | -   | -   | A/ms |
|                                |                                       | V <sub>D</sub> = 400 V; T <sub>j</sub> = 150 °C; I <sub>T(RMS)</sub> = 8 A; dV <sub>com</sub> /dt = 10 V/μs; gate open circuit                        | 15   | -   | -   | A/ms |
|                                |                                       | V <sub>D</sub> = 400 V; T <sub>j</sub> = 150 °C; I <sub>T(RMS)</sub> = 8 A; dV <sub>com</sub> /dt = 1 V/μs; gate open circuit                         | 20   | -   | -   | A/ms |

## 5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description         | Simplified outline   | Graphic symbol   |
|-----|--------|---------------------|--|--|
| 1   | CM     | common              |  <p><b>D2PAK (SOT404)</b></p> |  <p>003aaf296</p> |
| 2   | LD     | load                |  |  |
| 3   | G      | gate                |  |  |
| mb  | LD     | mounting base; load |  |  |

## 6. Ordering information

Table 3. Ordering information

| Type number   | Package |  |         |
|---------------|---------|--|---------|
|               | Name    | Description  | Version |
| ACTT8B-800CTN | D2PAK   | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404  |

## 7. Marking

Table 4. Marking codes

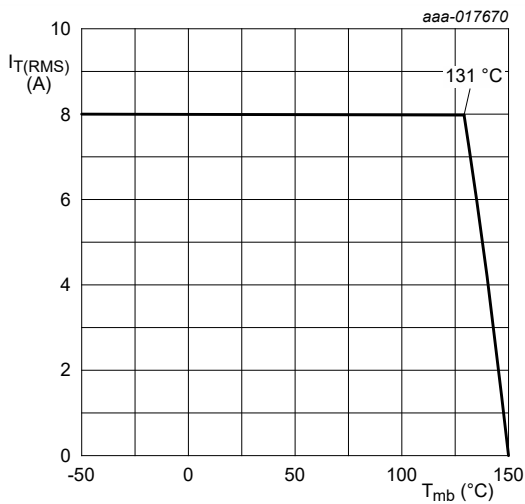
| Type number   | Marking code  |
|---------------|---------------|
| ACTT8B-800CTN | ACTT8B-800CTN |

### 8. Limiting values

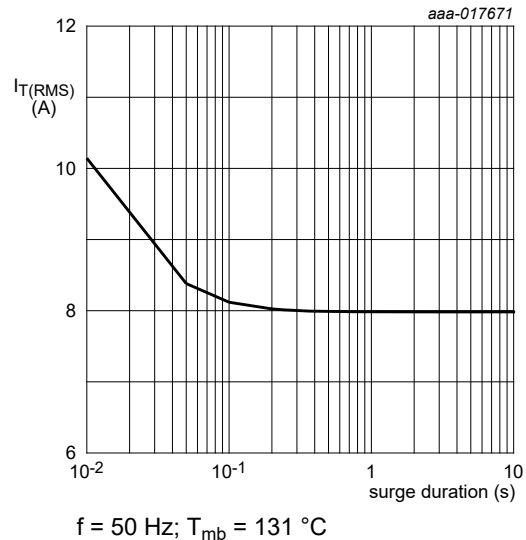
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol       | Parameter                            | Conditions   | Min | Max | Unit        |
|--------------|--------------------------------------|--|-----|-----|-------------|
| $V_{DRM}$    | repetitive peak off-state voltage    |  | -   | 800 | V           |
| $I_{T(RMS)}$ | RMS on-state current                 | full sine wave; $T_{mb} \leq 131\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>       | -   | 8   | A           |
| $I_{TSM}$    | non-repetitive peak on-state current | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a> | -   | 80  | A           |
|              |                                      | full sine wave; $T_{j(\text{init})} = 25\text{ °C}$ ; $t_p = 16.7\text{ ms}$   | -   | 88  | A           |
| $I^2t$       | $I^2t$ for fusing                    | $t_p = 10\text{ ms}$ ; sine-wave pulse   | -   | 32  | $A^2s$      |
| $di_T/dt$    | rate of rise of on-state current     | $I_G = 70\text{ mA}$   | -   | 100 | $A/\mu s$   |
| $I_{GM}$     | peak gate current                    | $t = 20\text{ }\mu s$  | -   | 2   | A           |
| $P_{GM}$     | peak gate power                      |  | -   | 5   | W           |
| $P_{G(AV)}$  | average gate power                   | over any 20 ms period  | -   | 0.5 | W           |
| $T_{stg}$    | storage temperature                  |  | -40 | 150 | $^{\circ}C$ |
| $T_j$        | junction temperature                 |  | -   | 150 | $^{\circ}C$ |
| $V_{PP}$     | peak pulse voltage                   | $T_j = 25\text{ °C}$ ; non-repetitive, off-state; <a href="#">Fig. 6</a>   | -   | 2   | kV          |



**Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values**



**Fig. 2. RMS on-state current as a function of surge duration; maximum values**

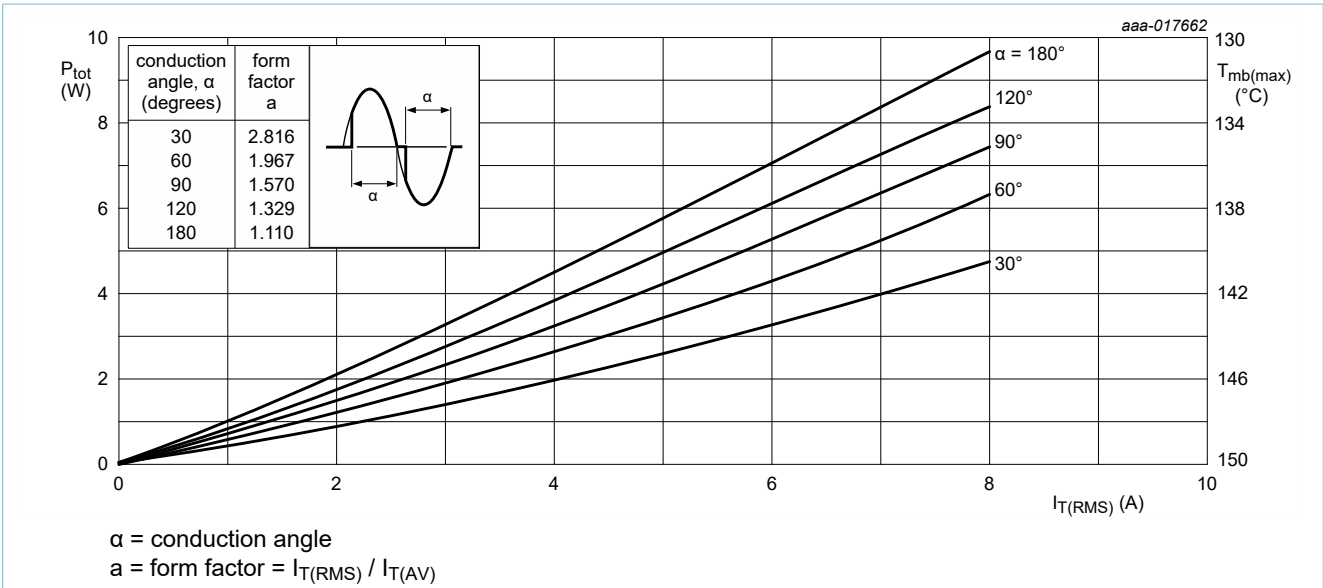


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

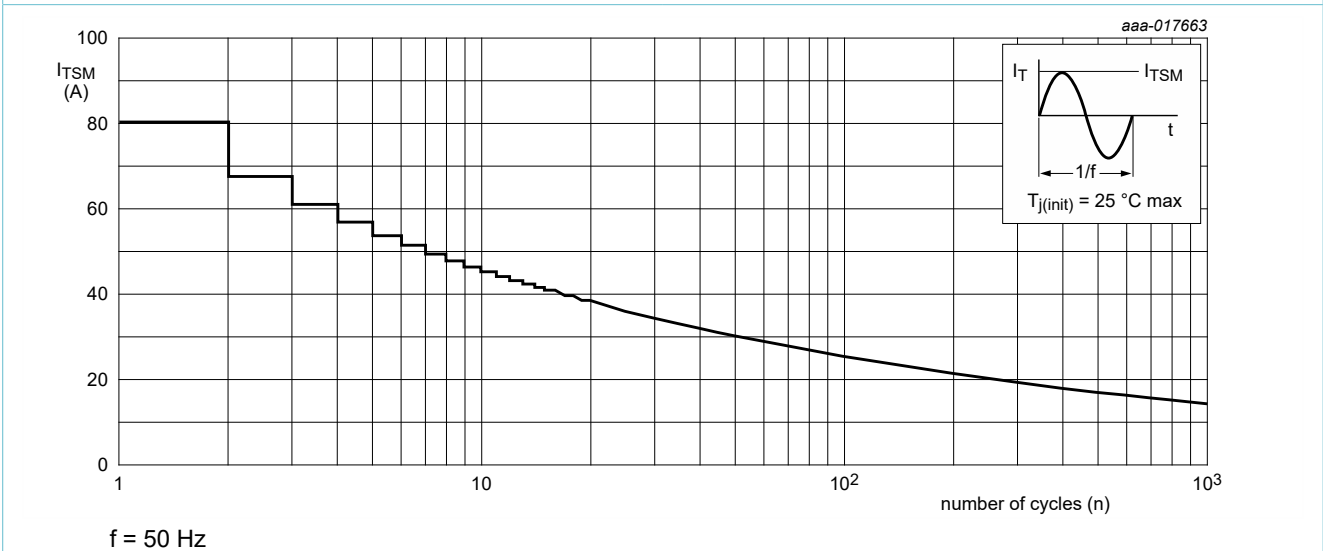


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

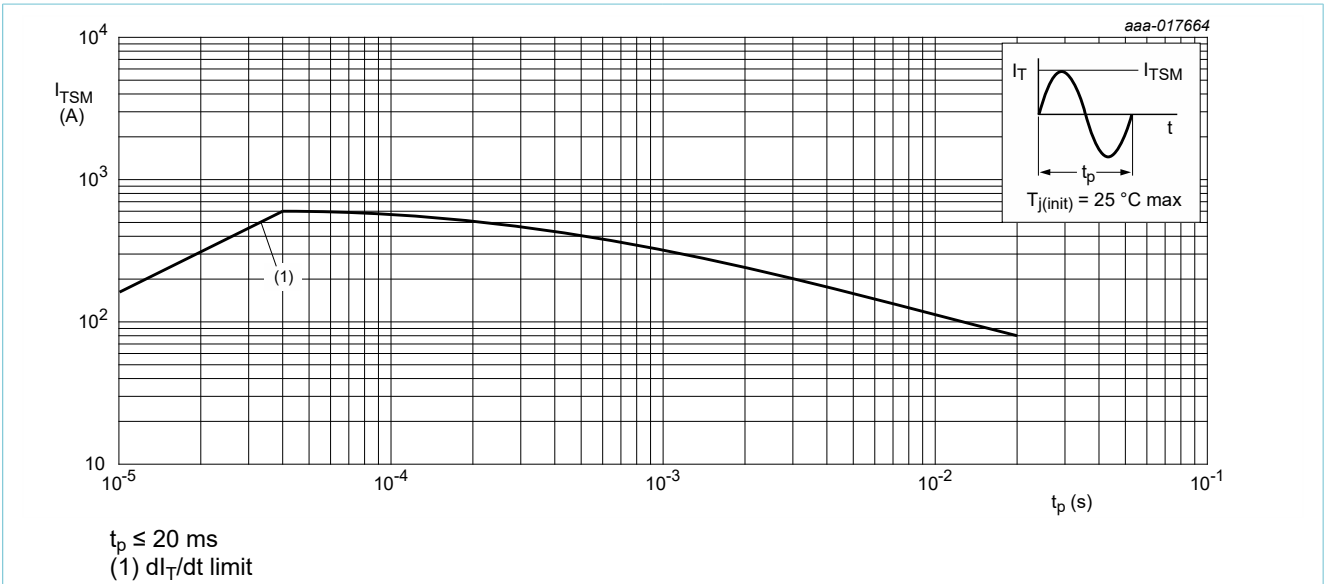


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

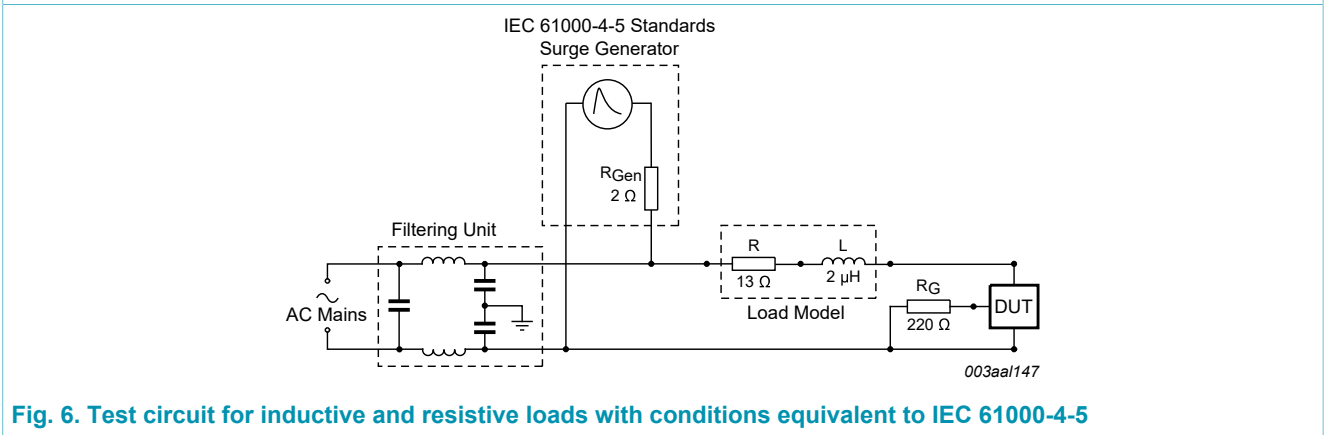
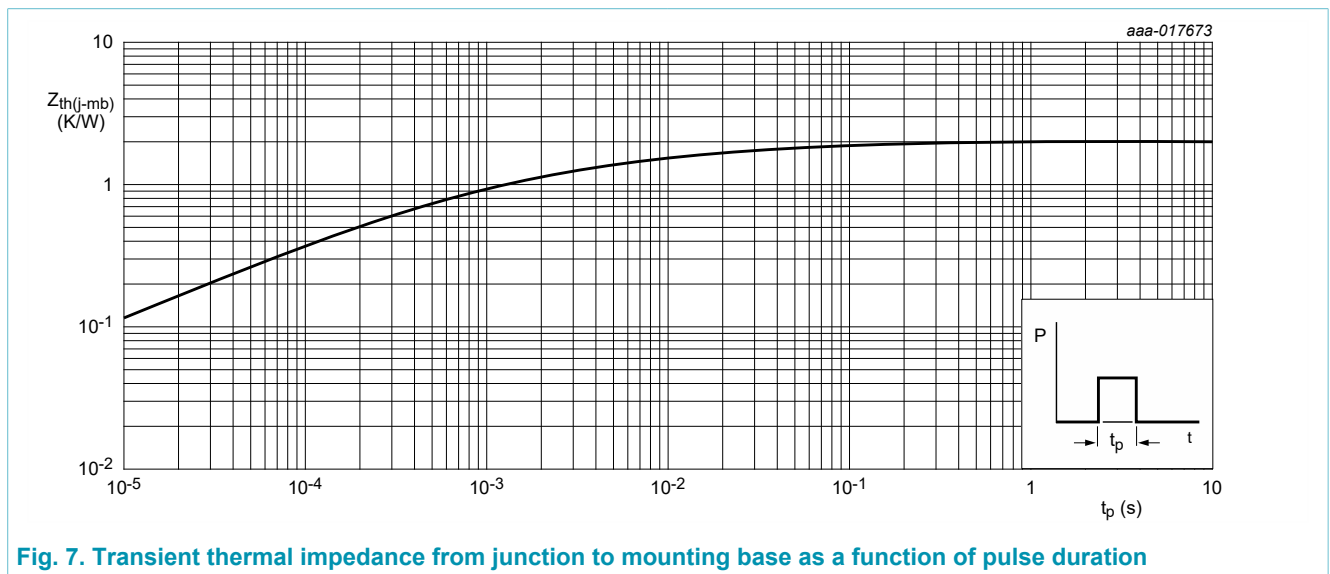


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

### 9. Thermal characteristics

Table 6. Thermal characteristics

| Symbol                | Parameter  | Conditions                                       | Min | Typ | Max | Unit |
|-----------------------|--|--|-----|-----|-----|------|
| R <sub>th(j-mb)</sub> | thermal resistance from junction to mounting base    | full cycle; <a href="#">Fig. 7</a>               | -   | -   | 2   | K/W  |
|                       |  | half cycle                                       | -   | -   | 2.4 | K/W  |
| R <sub>th(j-a)</sub>  | thermal resistance from junction to ambient free air | in free air; printed circuit board (FR4) mounted | -   | 55  | -   | K/W  |



## 10. Characteristics

Table 7. Characteristics

| Symbol                         | Parameter                             | Conditions  | Min  | Typ  | Max | Unit             |
|--------------------------------|---------------------------------------|---|------|------|-----|------------------|
| <b>Static characteristics</b>  |                                       |   |      |      |     |                  |
| $I_{GT}$                       | gate trigger current                  | $V_D = 12\text{ V}$ ; $I_T = 100\text{ mA}$ ; LD+ G+;<br>$T_j = 25\text{ °C}$ ; <a href="#">Fig. 8</a>  | 5    | -    | 35  | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 100\text{ mA}$ ; LD+ G-;<br>$T_j = 25\text{ °C}$ ; <a href="#">Fig. 8</a>  | 5    | -    | 35  | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_T = 100\text{ mA}$ ; LD- G-;<br>$T_j = 25\text{ °C}$ ; <a href="#">Fig. 8</a>  | 5    | -    | 35  | mA               |
| $I_L$                          | latching current                      | $V_D = 12\text{ V}$ ; $I_G = 100\text{ mA}$ ; LD+ G+;<br>$T_j = 25\text{ °C}$ ; <a href="#">Fig. 9</a>  | -    | -    | 50  | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 100\text{ mA}$ ; LD+ G-;<br>$T_j = 25\text{ °C}$ ; <a href="#">Fig. 9</a>  | -    | -    | 60  | mA               |
|                                |                                       | $V_D = 12\text{ V}$ ; $I_G = 100\text{ mA}$ ; LD- G-;<br>$T_j = 25\text{ °C}$ ; <a href="#">Fig. 9</a>  | -    | -    | 50  | mA               |
| $I_H$                          | holding current                       | $V_D = 12\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 10</a>  | -    | -    | 40  | mA               |
| $V_T$                          | on-state voltage                      | $I_T = 10\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 11</a>  | -    | -    | 1.5 | V                |
| $V_{GT}$                       | gate trigger voltage                  | $V_D = 12\text{ V}$ ; $I_T = 100\text{ mA}$ ; $T_j = 25\text{ °C}$ ;<br><a href="#">Fig. 12</a>   | -    | 0.8  | 1   | V                |
|                                |                                       | $V_D = 400\text{ V}$ ; $I_T = 100\text{ mA}$ ; $T_j = 150\text{ °C}$ ;<br><a href="#">Fig. 12</a>   | 0.2  | 0.45 | -   | V                |
| $I_D$                          | off-state current                     | $V_D = 800\text{ V}$ ; $T_j = 25\text{ °C}$   | -    | -    | 10  | $\mu\text{A}$    |
|                                |                                       | $V_D = 800\text{ V}$ ; $T_j = 150\text{ °C}$  | -    | -    | 2   | mA               |
| $V_{CL}$                       | clamping voltage                      | $I_{CL} = 0.1\text{ mA}$ ; $t_p = 1\text{ ms}$ ; $T_j = 25\text{ °C}$   | 850  | -    | -   | V                |
| <b>Dynamic characteristics</b> |                                       |   |      |      |     |                  |
| $dV_D/dt$                      | rate of rise of off-state voltage     | $V_{DM} = 536\text{ V}$ ; $T_j = 125\text{ °C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit                                   | 4000 | -    | -   | V/ $\mu\text{s}$ |
|                                |                                       | $V_{DM} = 536\text{ V}$ ; $T_j = 150\text{ °C}$ ; exponential waveform; gate open circuit   | 2000 | -    | -   | V/ $\mu\text{s}$ |
| $di_{com}/dt$                  | rate of change of commutating current | $V_D = 400\text{ V}$ ; $T_j = 150\text{ °C}$ ; $I_{T(RMS)} = 8\text{ A}$ ; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$ ; gate open circuit; snubberless condition | 12   | -    | -   | A/ms             |
|                                |                                       | $V_D = 400\text{ V}$ ; $T_j = 150\text{ °C}$ ; $I_{T(RMS)} = 8\text{ A}$ ; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$ ; gate open circuit                        | 15   | -    | -   | A/ms             |
|                                |                                       | $V_D = 400\text{ V}$ ; $T_j = 150\text{ °C}$ ; $I_{T(RMS)} = 8\text{ A}$ ; $dV_{com}/dt = 1\text{ V}/\mu\text{s}$ ; gate open circuit                         | 20   | -    | -   | A/ms             |



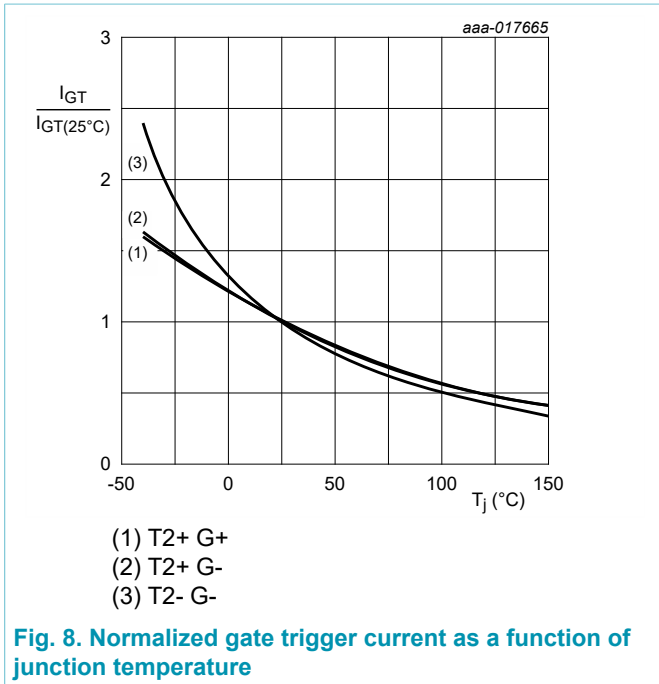


Fig. 8. Normalized gate trigger current as a function of junction temperature

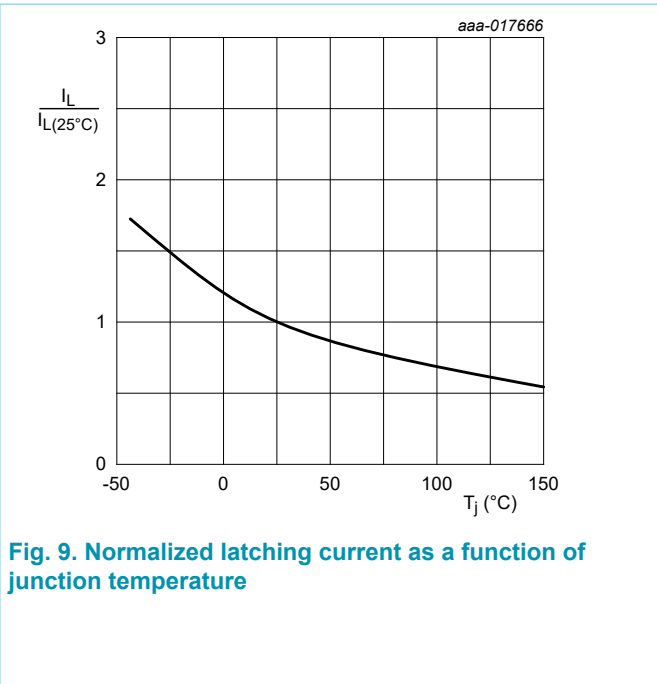


Fig. 9. Normalized latching current as a function of junction temperature

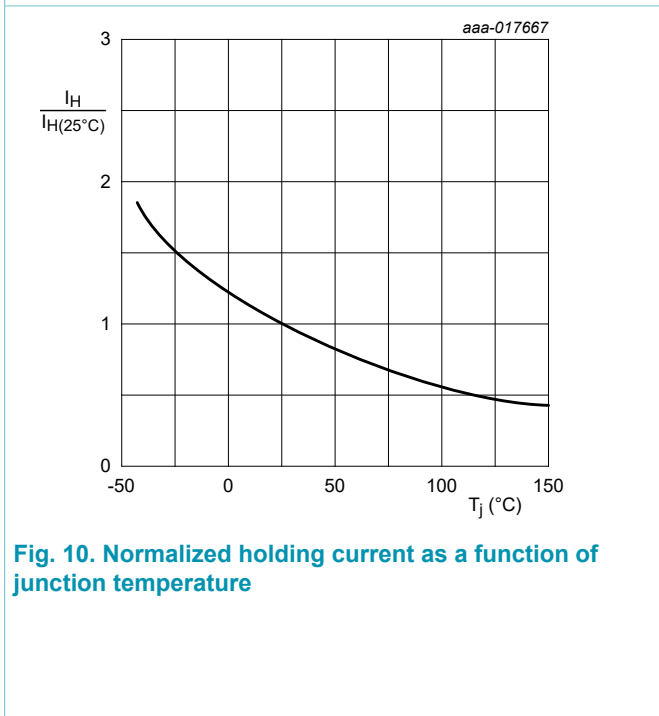


Fig. 10. Normalized holding current as a function of junction temperature

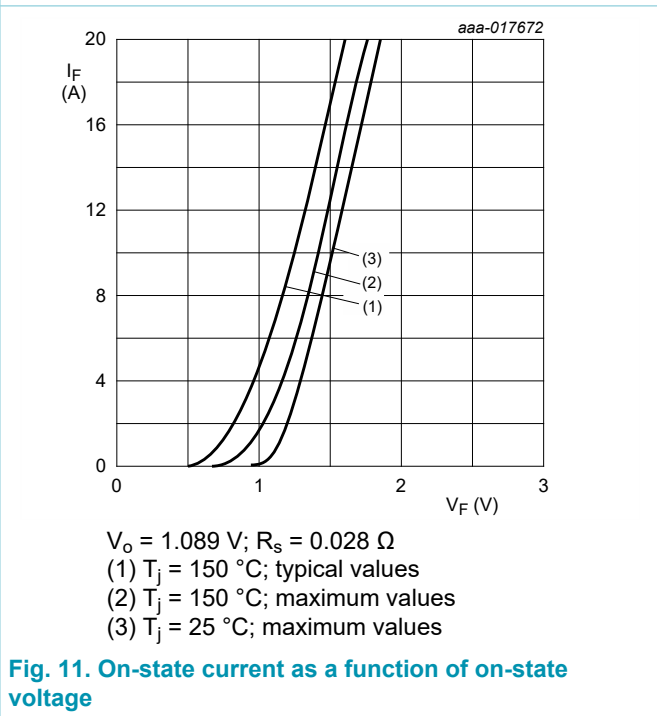


Fig. 11. On-state current as a function of on-state voltage

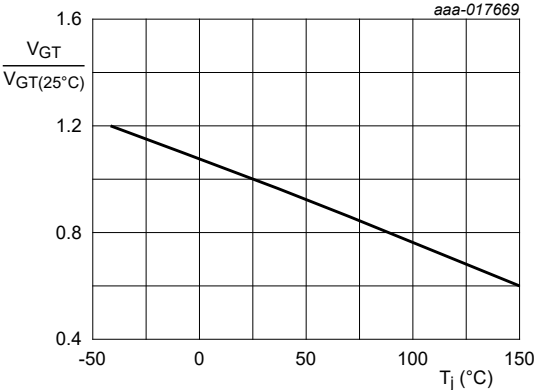


Fig. 12. Normalized gate trigger voltage as a function of junction temperature

### 11. Package outline

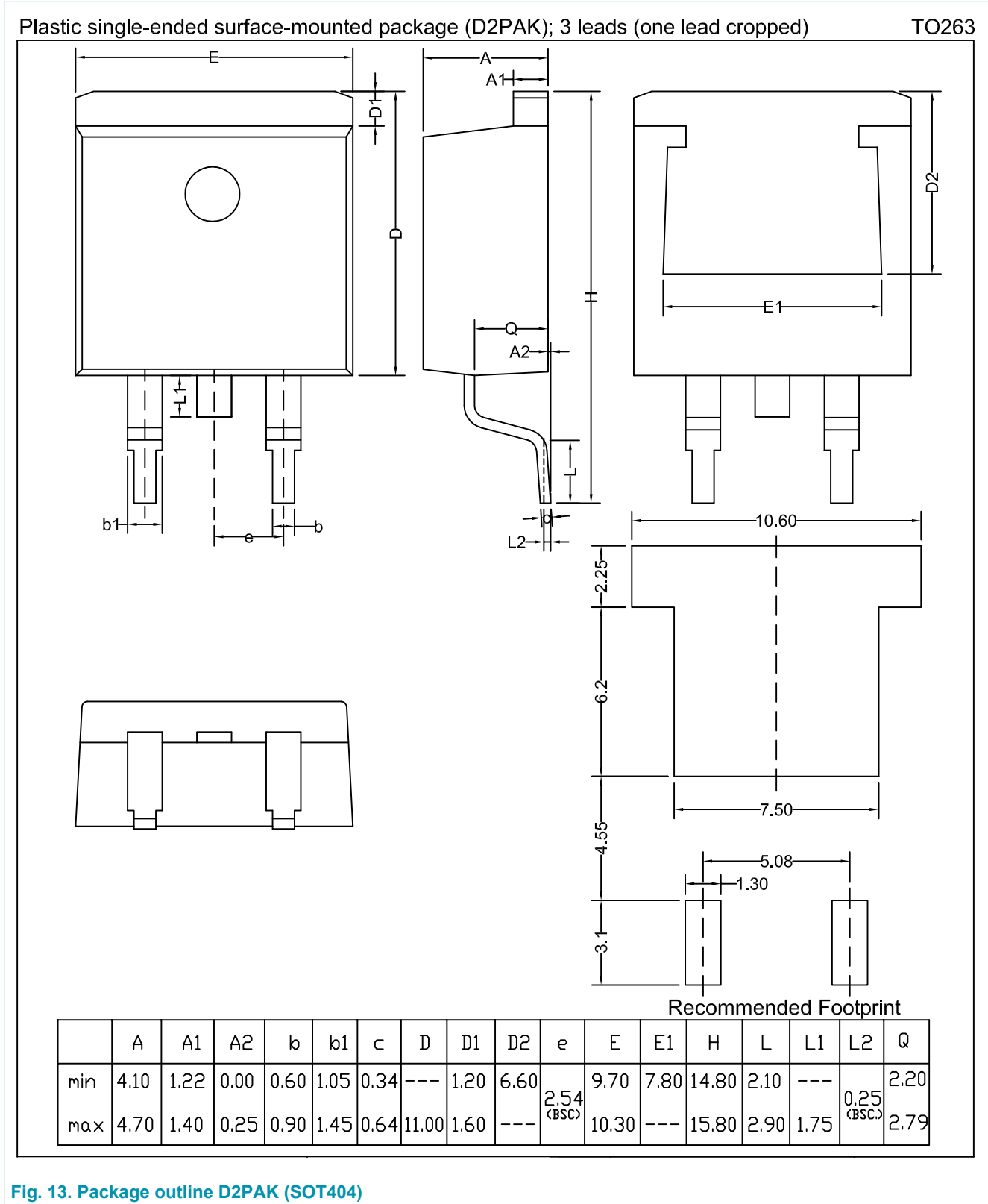


Fig. 13. Package outline D2PAK (SOT404)

## 12. Soldering

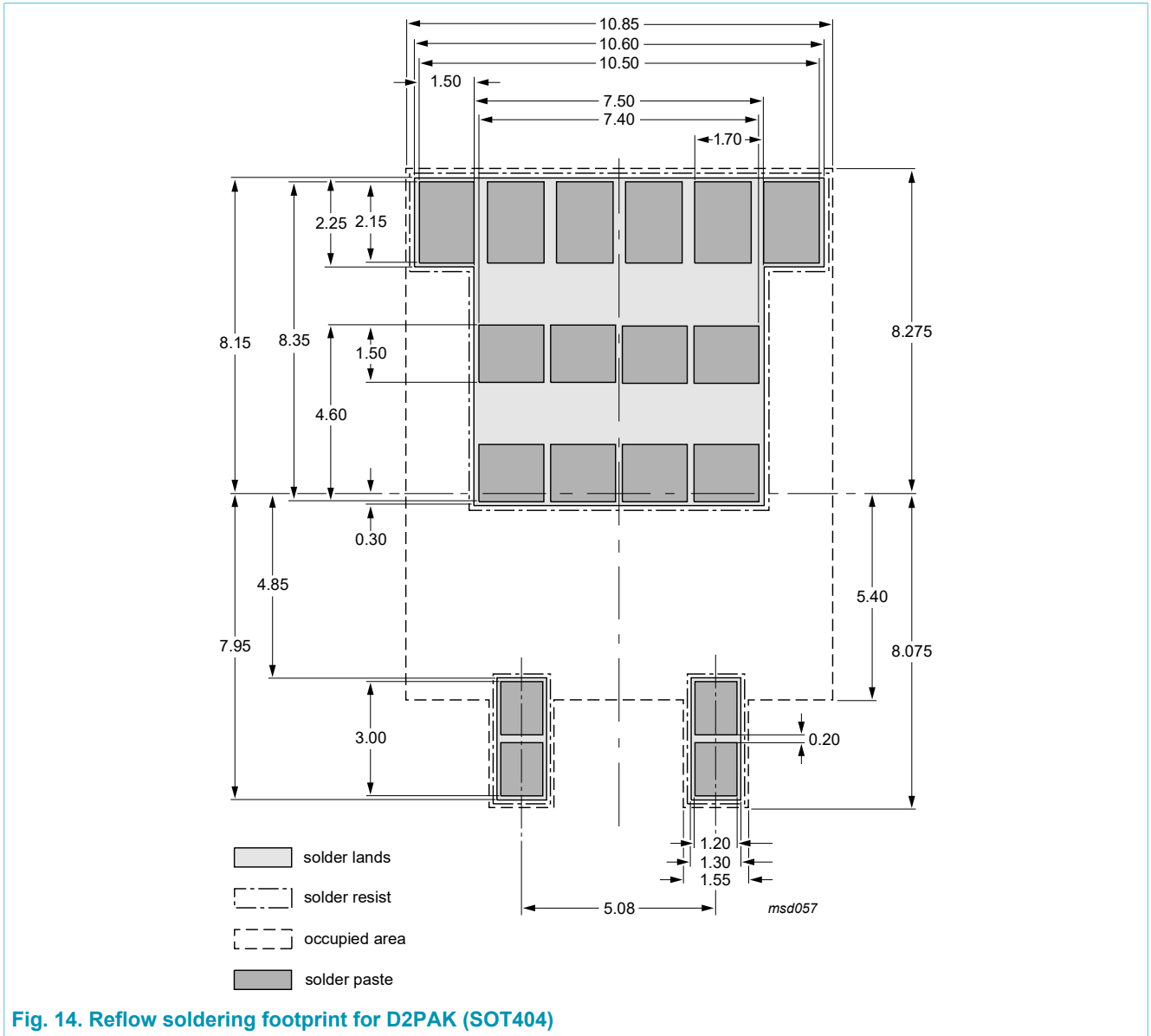


Fig. 14. Reflow soldering footprint for D2PAK (SOT404)

## 13. Legal information

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| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
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