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April 2014



FDA8440

N-Channel Logic Level PowerTrench[®] MOSFET

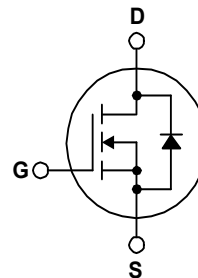
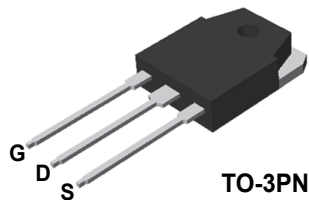
40 V, 100 A, 2.1 mΩ

Features

- $R_{DS(on)} = 1.46 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 80 \text{ A}$
- $Q_{G(tot)} = 345 \text{ nC}$ (Typ.) @ $V_{GS} = 10 \text{ V}$
- Low Miller Charge
- Low Q_{rr} Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- 160 A Guarantee for 2 sec
- RoHS Compliant

Application

- Power tools
- Motor drives and Uninterruptible Power Supplies
- Synchronous Rectification
- Battery Protection Circuit



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDA8440	Unit
V_{DSS}	Drain to Source Voltage	40	V
V_{GSS}	Gate to Source Voltage	± 20	V
I_D	Drain Current - Continuous ($T_C = 155^\circ\text{C}$)	100	A
	- Continuous ($T_A = 25^\circ\text{C}$, $V_{GS} = 10 \text{ V}$, $R_{\theta JA} = 40^\circ\text{C/W}$)	30	A
	- Pulsed	500	A
E_{AS}	Single Pulsed Avalanche Energy (Note 1)	1682	mJ
P_D	Power dissipation	306	W
	Derate above 25°C	2.04	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to +175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.49	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 2)	40	$^\circ\text{C/W}$

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDA8440	FDA8440	TO-3PN	Tube	N/A	N/A	30 units

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	40	--	--	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 32 V	--	--	1	μA
		V _{GS} = 0 V, T _C = 150°C	--	--	250	μA
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±20 V	--	--	±100	nA
On Characteristics						
V _{GS(th)}	Gate to Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1	--	3	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 4.5 V, I _D = 80 A	--	1.56	2.2	mΩ
		V _{GS} = 10 V, I _D = 80 A	--	1.46	2.1	
		V _{GS} = 10 V, I _D = 80 A, T _C = 175°C	--	2.82	4.1	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	--	18600	24740	pF
C _{oss}	Output Capacitance		--	1840	2450	pF
C _{rss}	Reverse Transfer Capacitance		--	1400	2100	pF
R _G	Gate Resistance	V _{GS} = 0.5 V, f = 1 MHz	--	1.1	--	Ω
Q _{g(tot)}	Total Gate Charge at 10V	V _{GS} = 0 V to 10 V	--	345	450	nC
Q _{g(2)}	Threshold Gate Charge	V _{GS} = 0 V to 2 V	--	32.5	--	nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 20 V I _D = 80 A I _g = 1.0 mA	--	49	--	nC
Q _{gs2}	Gate Charge Threshold to Plateau		--	16.5	--	nC
Q _{gd}	Gate to Drain "Miller" Charge		--	74	--	nC
Switching Characteristics						
t _{ON}	Turn-On Time	V _{DD} = 20 V, I _D = 80 A V _{GS} = 10 V, R _{GEN} = 7 Ω	--	175	360	ns
t _{d(on)}	Turn-On Delay Time		--	43	95	ns
t _r	Rise Time		--	130	275	ns
t _{d(off)}	Turn-Off Delay Time		--	435	875	ns
t _f	Fall Time		--	290	590	ns
t _{OFF}	Turn-Off Time		--	730	1470	ns
Drain-Source Diode Characteristics and Maximum Ratings						
V _{SD}	Source to Drain Diode Voltage	I _{SD} = 80 A	--	--	1.25	V
		I _{SD} = 40 A	--	--	1.0	V
t _{rr}	Reverse Recovery Time	I _{SD} = 75 A, dI _{SD} /dt = 100 A/μs	--	59	--	ns
Q _{RR}	Reverse Recovery Charge	I _{SD} = 75 A, dI _{SD} /dt = 100 A/μs	--	77	--	nC

NOTES:

- Starting T_J = 25°C, L = 1 mH, I_{AS} = 58 A, V_{DD} = 36 V, V_{GS} = 10 V.
- Pulse width = 100 s.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

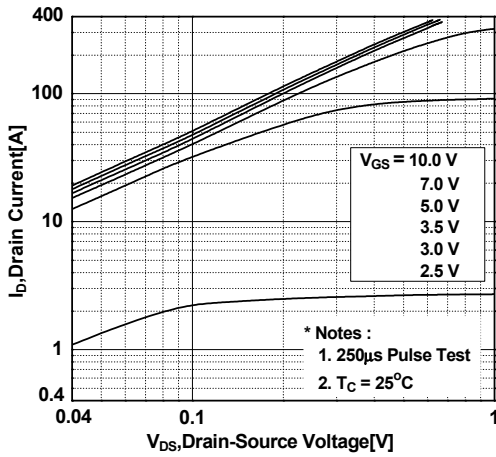


Figure 2. Transfer Characteristics

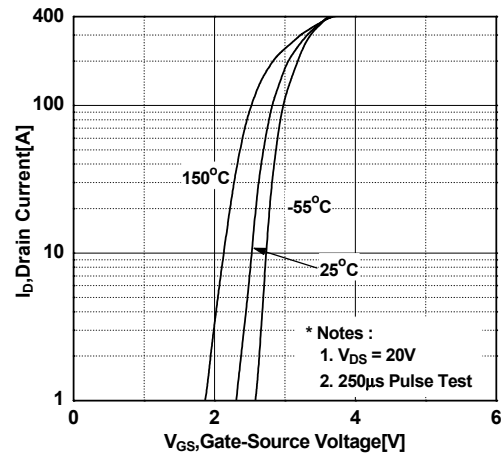


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

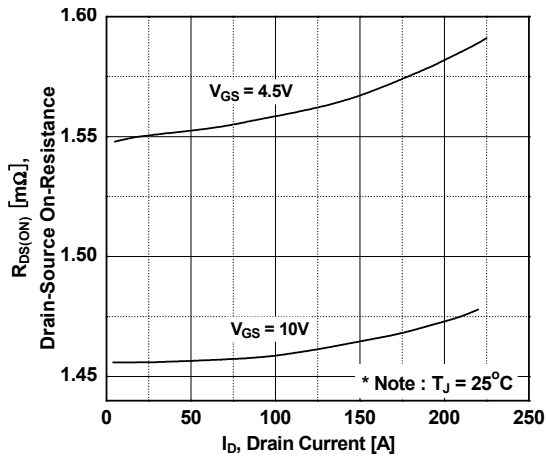


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

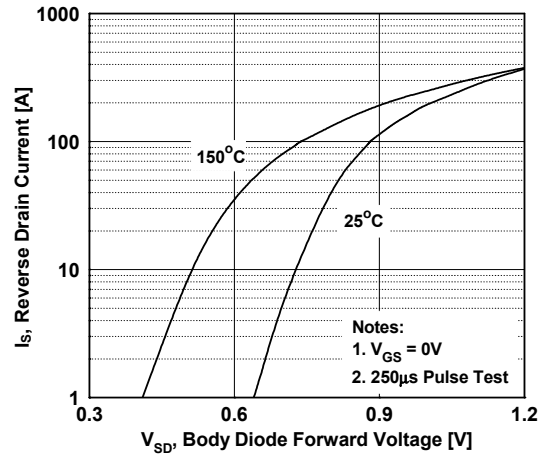


Figure 5. Capacitance Characteristics

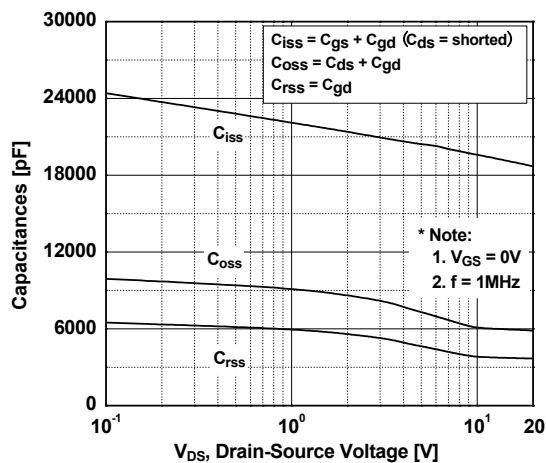
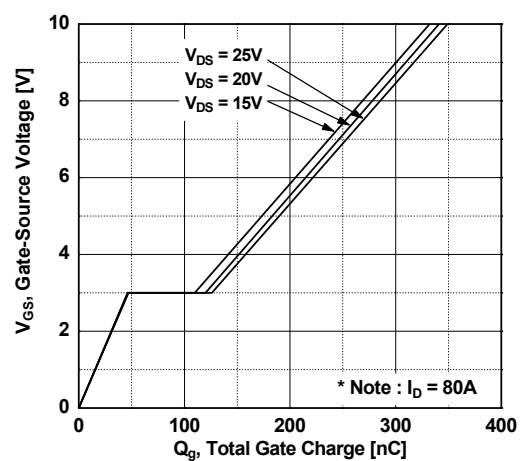


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

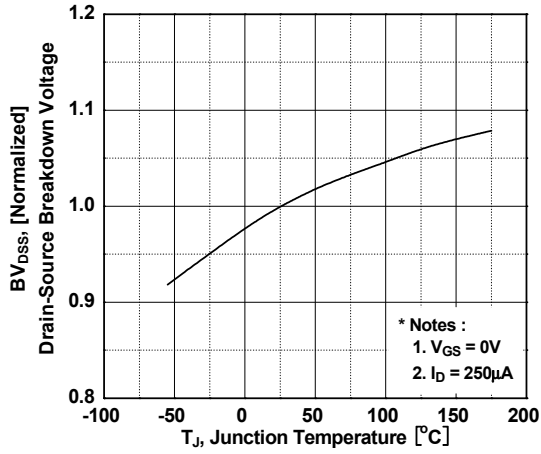


Figure 8. On-Resistance Variation vs. Temperature

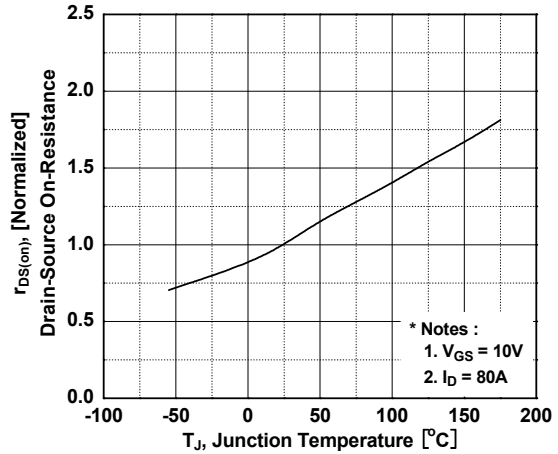


Figure 9. Unclamped Inductive Switching Capability

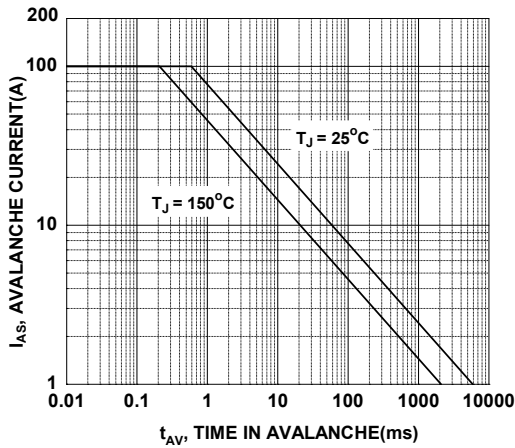


Figure 10. Safe Operating Area

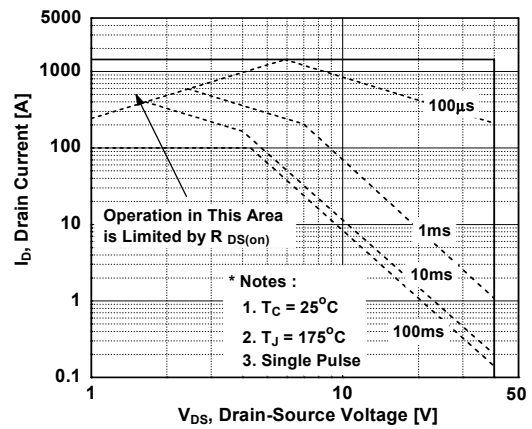
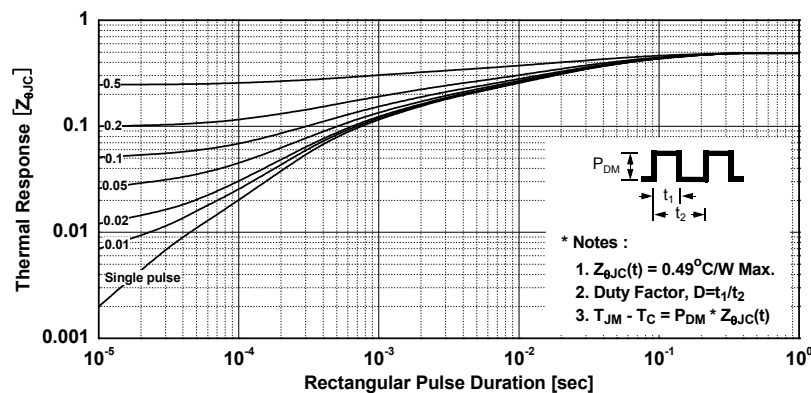


Figure 11. Transient Thermal Response Curve



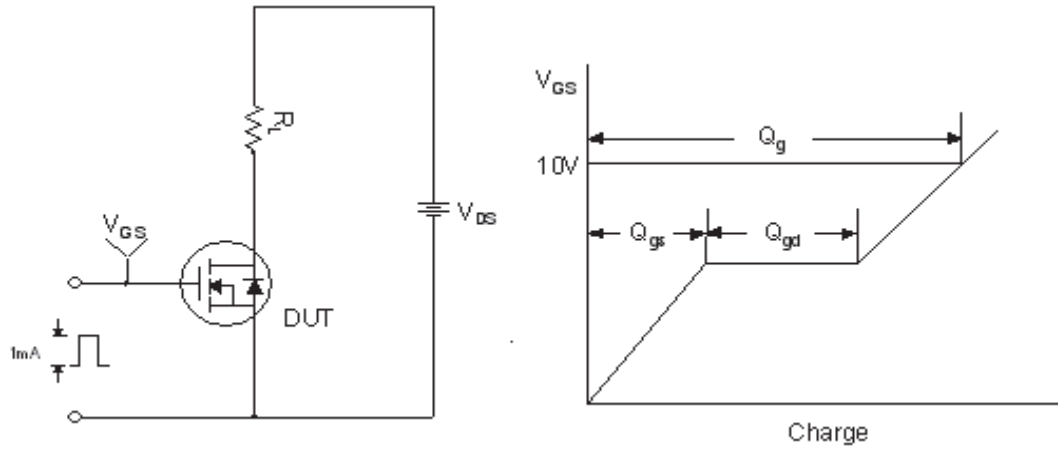


Figure 12. Gate Charge Test Circuit & Waveform

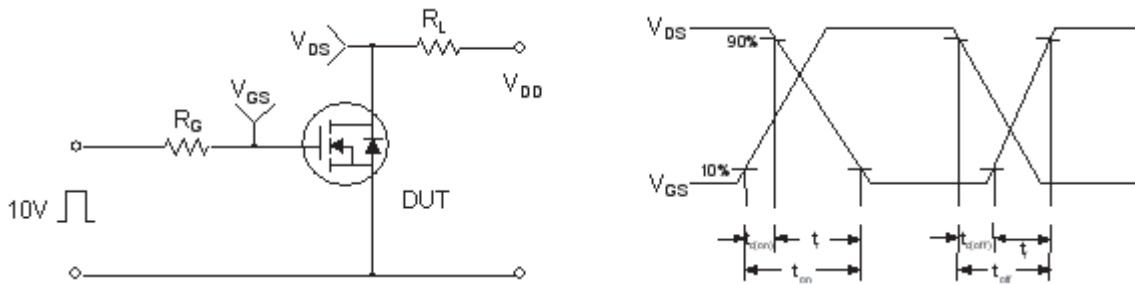


Figure 13. Resistive Switching Test Circuit & Waveforms

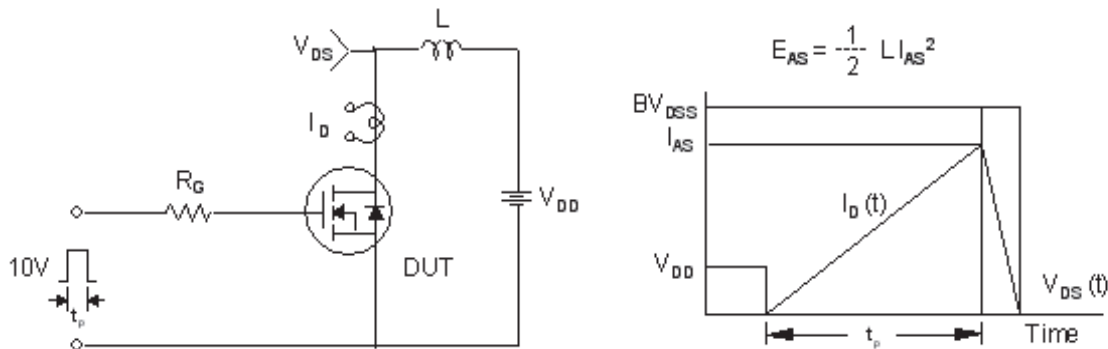


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

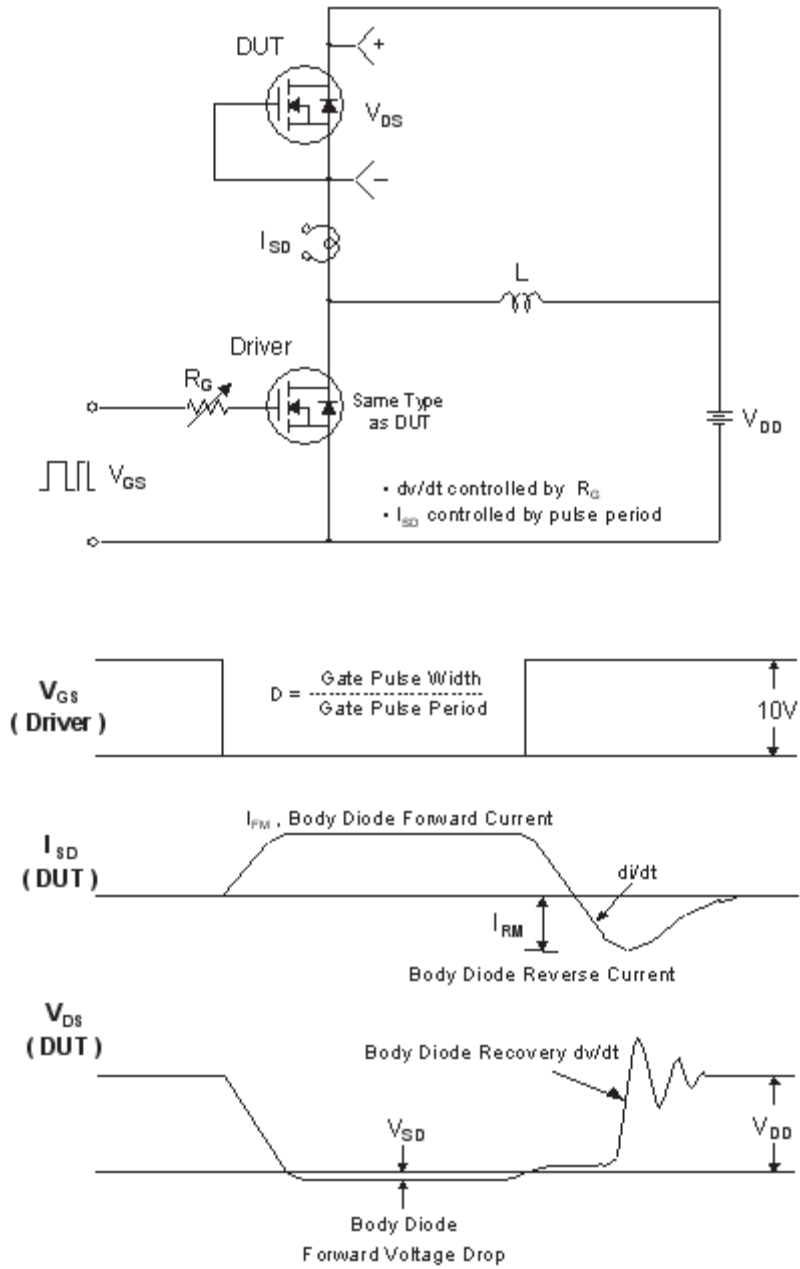



Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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